Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE 3110
Course Title: Digital System Design Lab

Experiment Number: 01

Name of the Experiment: Designing a 4-bit ALU (Arithmetic and Logic Unit)

Group Number: 04

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Introduction:

In this experiment, we made a 4-bit Arithmetic Logic Unit (ALU) using a 4-bit full adder and basic gates. In this experiment, if S2 = 0 then the ALU will perform the arithmetic operation, and if the S2 = 1 then the ALU will perform the logical operation. So, depending on the value of S2 the ALU will perform a logical or arithmetic operation.

Problem Statement:

S2	S1	S0	Output	Function
0	0	0	Ai + 1 + 1	Transfer A with carry
0	0	1	Ai – Bi -1	Subtraction with borrow
0	1	0	Ai -1	Decrement A
0	1	1	Ai + Bi	Add
1	0	X	Ai **.** Bi	AND
1	1	X	Ai | Bi	OR

Function Generation:

S2	S1	S0	Z	X	Y	Output	Function
0	0	0	1	Ai	All 1	Ai + 1 + 1	Transfer A with carry
0	0	1	0	Ai	$\overline{Bi}$	Ai – Bi -1	Subtraction with borrow
0	1	0	0	Ai	All 1	Ai -1	Decrement A
0	1	1	0	Ai	Bi	Ai + Bi	Add
1	0	X	0	Ai . Bi	0	Ai **.** Bi	AND
1	1	X	0	Ai + Bi	0	Ai | Bi	OR

$$X = \overline{S2}\,Ai + S2\,\overline{S1}\,Ai\,Bi + S2\,S1\,(Ai + Bi)$$

$$= \overline{S2}\,Ai + S2\,\overline{S1}\,Ai\,Bi + S2\,S1\,Ai + S2\,S1\,Bi$$

$$= \overline{S2}\,Ai + S2\,Ai\,(\overline{S1}\,Bi + S1) + S2\,S1\,Bi$$

$$= \overline{S2}\,Ai + S2\,Ai\,(\overline{S1} + S1)\,(Bi + S1) + S2\,S1\,Bi$$

$$= \overline{S2}\,Ai + S2\,Ai\,(Bi + S1) + S2\,S1\,Bi$$

$$= \overline{S2}\,Ai + S2\,Ai\,Bi + S2\,S1\,Ai + S2\,S1\,Bi$$

$= Ai\ (\overline{S2} + S2\ S1\ ) + S2\ Ai\ Bi + S2\ S1\ Bi$

$= Ai\ (\overline{S2} + S2\ )\ (\overline{S2} + S1\ ) + S2\ Ai\ Bi + S2\ S1\ Bi$

$= Ai\ (\overline{S2} + S1\ ) + S2\ Ai\ Bi + S2\ S1\ Bi$

$= Ai\ \overline{S2} + Ai\ S1 + S2\ Ai\ Bi + S2\ S1\ Bi$

$= Ai\ (\overline{S2} + S2\ Bi\ ) + Ai\ S1 + S2\ S1\ Bi$

$= Ai\ (\overline{S2} + S2\ )\ \left(\overline{S2} + Bi\ \right) + Ai\ S1 + S2\ S1\ Bi$

$= Ai\ \left(\overline{S2} + Bi\ \right) + Ai\ S1 + S2\ S1\ Bi$

$= Ai\ (\overline{S2} + S1 + Bi\ ) + S2\ S1\ Bi$

$Y = \overline{S2}\ \overline{S1}\ \overline{S0} + \overline{S2}\ \overline{S1}\ S0\ \overline{Bi} + \overline{S2}\ S1\ \overline{S0} + \overline{S2}\ S1\ S0\ Bi$

$= \overline{S2}\ \overline{S0}\ (\overline{S1} + S1\ ) + \overline{S2}\ S0\ (\overline{S1}\ \overline{Bi} + S1\ Bi)$

$= \overline{S2}\ \overline{S0} + \overline{S2}\ S0\ (\overline{S1}\ \overline{Bi} + S1\ Bi)$

$= \overline{S2}\ \overline{S0} + \overline{S2}\ S0\ (\overline{S1 \oplus Bi}\ )$

$= \overline{S2}\ (\overline{S0} + S0\ (\overline{S1 \oplus Bi}\ ))$

$= \overline{S2}\ (\overline{S0} + S0\ )\ (\overline{S0} + \left(\overline{S1 \oplus Bi}\right)\ )$

$= \overline{S2}\ (\overline{S0} + \overline{S1 \oplus Bi}\ )$

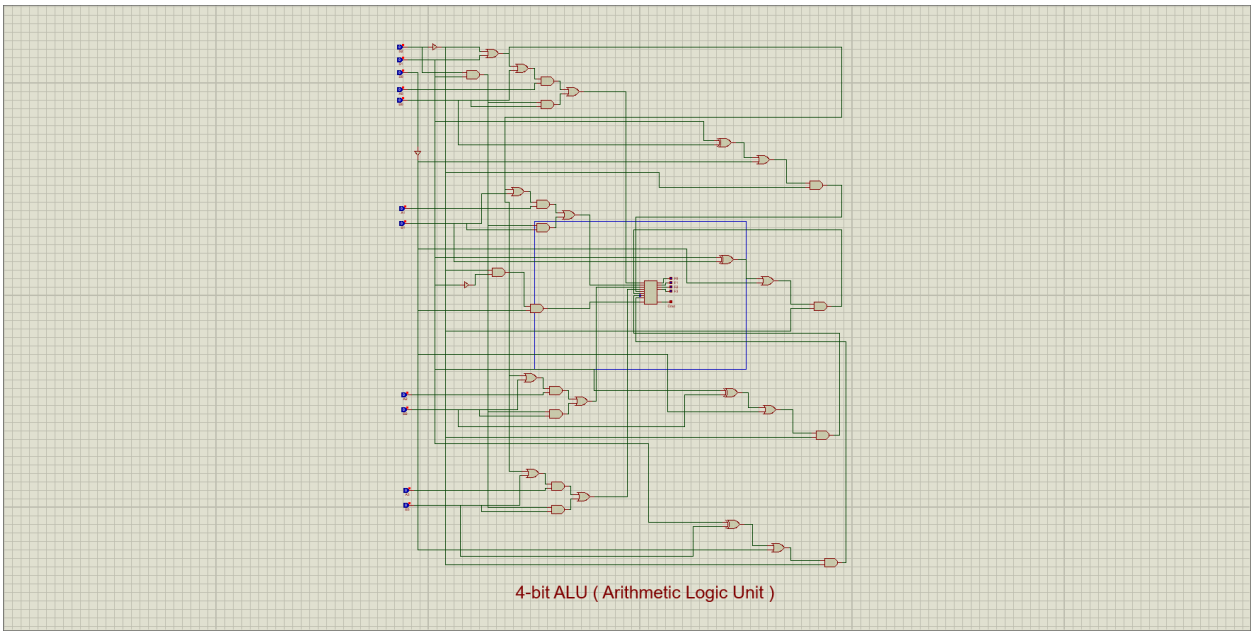
$Z = \overline{S2}\ \overline{S1}\ \overline{S0}$

Equipment and Budget:

Gate Name	IC	Amount	Price per IC (tk)	Price(tk)
AND	7408	4	30	120
OR	7432	4	29	116

NOT	7404	1	25	25
XNOR	4077	1	26	26
4-bit full adder	4008	1	40	40
Total Cost = 327				

Simulation:



Result:

For Transfer A with Carry operation,

Input											Output				
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0
			0	1	1	0					1	0	1	1	0
			1	1	1	1					1	1	1	1	1

For Subtraction with Borrow operation,

Input											Output				
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
0	0	1	0	0	1	0	0	1	1	0	0	1	0	1	1
			0	0	0	0	1	1	0	0	0	0	0	1	1
			0	1	1	1	0	0	0	0	1	0	1	1	0

For Decrement A operation,

Input											Output				
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0
			1	0	0	1					1	1	0	0	0
			0	1	0	1					1	0	1	0	0

For Addition operation,

Input											Output				
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	1	1	1	1	1	1	1	1	1	1	1	0
			1	0	1	0	1	0	0	1	1	0	0	1	1

For AND operation,

Input											Output				
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
1	0	X	0	1	0	1	1	0	0	1	0	0	0	0	1
			1	0	1	1	1	1	0	1	0	1	0	0	1
			0	0	1	0	0	1	1	1	0	0	0	1	0

For OR operation,

Input											Output				
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
1	1	X	0	1	1	1	0	0	1	0	0	0	1	1	1
			1	0	0	1	0	1	0	1	0	1	1	0	1
			1	1	1	1	0	0	1	0	0	1	1	1	1

Conclusion:

There were some errors while working with Dual carry save full adder (IC 74LS183). While working with IC74LS183 the proteus software was showing some errors such as (No model specified, Simulation Failed due to partition analysis error). But even after fixing these errors the circuit was not showing any output. After that, we used a 4-bit Binary full adder with fast carry (IC4008). After using this IC, the circuit worked perfectly and there was no error during simulation. All operations worked without generating any error.