Ahsanullah University of Science and Technology (AUST)

Department of Computer Science and Engineering

LAB REPORT

Course No. : CSE 3110

Course Title: Digital System Design Lab

Experiment Number: 02

Name of the Experiment: Designing a 5-bit Booth

Group Number: 04

Group Members:

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Introduction:

In this experiment, we made a 5-bit Booth Multiplier using Adder, Flip-Flops, and Basie gates. Booths multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. In this experiment, we will input multiplicand (m) and multiplier (r), both are 5-bit values and get the value of (m X r) as result. Booths multiplication algorithm can be implemented by repeatedly adding one of two predetermined values A and S to a product P, then performing a right ward arithmetic shift on P. Here -

A= M (5 bits) 0 (6 bits)

S = -M (5 bits) 0 (6 bits)

P = 0 (5 bits) R (5 bits) 0 (1 bit)

Problem Statement:

Design a 5-bit Booth Multiplier.

Operations:

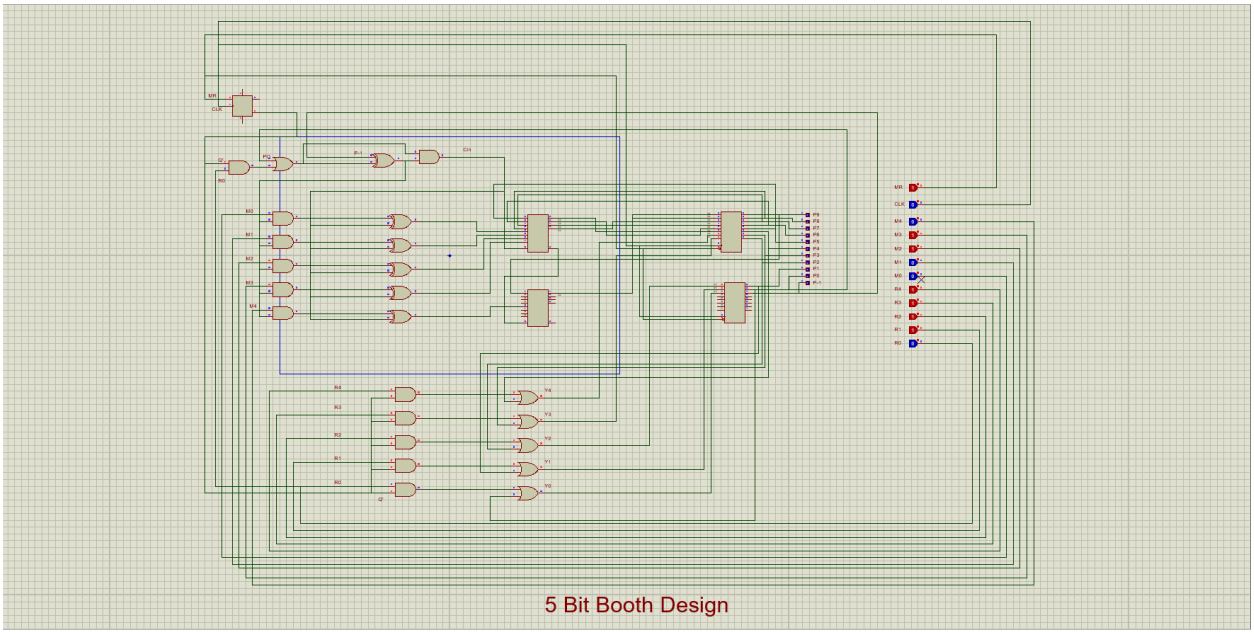
P_0	P_{-1}	Operation
0	0	P + 0
0	1	P + A
1	0	P + S
1	1	P + 0

After executing the required operation, the algorithm right shifts P by 1 bit after each iteration.

Equipment and Budget:

Gate Name	IC	Amount	Price per IC	Price (Taka)
AND	7408	3	30	90
OR	7432	2	29	58
D Flip Flop	74273	2	40	80
XOR	4077	2	26	52
D Flip Flop	4013	1	17	17
4-bit Full Adder	4008	2	40	80
				Full Price - 377 Taka

Simulation:



Result:

M	R	Clock Pulse	P
01111	01111	CLK 1	11000101111
		CLK 2	11100010111
		CLK 3	11110001011
		CLK 4	11111000101
		CLK 5	00111000010

M	R	Clock Pulse	P
01100	11110	CLK 1	00000011110
		CLK 2	11010001111
		CLK 3	11101000111
		CLK 4	11110100011
		CLK 5	11111010001

M	R	Clock Pulse	P
01110	11011	CLK 1	11001011011
		CLK 2	11100101101
		CLK 3	00101010110
		CLK 4	11011101011
		CLK 5	11101110101

Conclusion:

While using the shift Register IC (7496) for the right shift operation, the values were not being loaded to the IC after a few clock pulses. So, we have manually performed the right shift operation using the D flip flop IC (4013). One extra clock pulse is needed to load the value of P in the D flip Flop and to compare the 2 least significant bits of P initially. To avoid the situation, we have used a few extra gates so that the 2 least significant bits of P get compared and the required operation is performed before the first clock pulse is given. The total number of required addition/subtraction operations is not fixed which resulted in difficulties during testing the results. The complexity of the circuit was another disadvantage.