GATE SOLVED PAPER
Computer Science Engineering
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GATE SOLVED PAPER - CS

COMPUTER ORGANIZATION & ARCHITECTURE

Q. 1   More than one word are put in one cache block to
(A) Exploit the temporal locality of reference in a program

(B) Exploit the spatial locality of reference in a program

(C) Reduce the miss penalty

(D) None of the above

Q. 2   A low memory can be connected to 8085 by using
(A) INTER   (B) $\overline{\text{RESET IN}}$
(C) HOLD   (D) READY

Q. 3   Suppose a processor does not have any stack pointer register. Which of the following statements is true ?
(A) It cannot have subroutine call instruction

(B) It can have subroutine call instruction, but no nested subroutine calls.

(C) Nested subroutine calls are possible, but interrupts are not.

(D) All sequences of subroutine calls and also interrupts are possible

Q. 4   A processor needs software interrupt to
(A) Test the interrupt system of the processor.

(B) Implement co-routines.

(C) Obtain system services which need execution of privileged instructions.

(D) Return from subroutine.

Q. 5   A CPU has two modes-privileged and non-privileged. In order to change the mode from privileged to non-privileged.
(A) A hardware interrupt is needed.

(B) A software interrupt is needed.

(C) A privileged instruction (which does not generate an interrupt) is needed.

(D) A non-privileged instruction (Which does not generate an interrupt) is needed.

Q. 6   The process of assigning load addresses to the various parts of the program and adjusting the code and date in the program to reflect the assigned addresses is called
(A) Assembly   (B) Parsing
(C) Relocation   (D) Symbol resolution

Q. 7   Which of the following requires a device driver ?
(A) Register   (B) Cache
(C) Main memory   (D) Disk

Q. 8　　Which is the most appropriate match for the items in the first column with the items in the second column

(X.) Indirect Addressing　　　　　　(I.) Array implementation

(Y.) Indexed Addressing　　　　　　(II.) Writing re-locatable code

(Z.) Base Register Addressing　　　　(III.) Passing array as parameter

(A) (X, III) (Y, I) (Z, II)　　　　　(B) (X, II) (Y, III) (Z, I)

(C) (X, III) (Y, II) (Z, I)　　　　　(D) (X, I) (Y, III) (Z, II)

Q. 9　　Consider the following data path of a simple non-pilelined CPU. The registers A, B, A_1, A_2, MDR the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size $8 \times (2{:}1)$ and the DEMUX is of size $8 \times (1{:}2)$. Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.
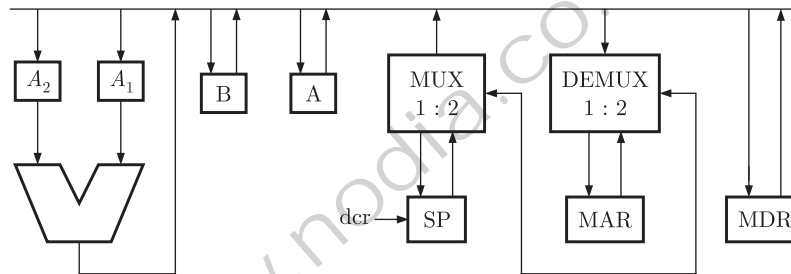
The CPU instruction "push r", where = A or B, has the specification

$$M[SP] \leftarrow r$$
$$SP \leftarrow SP - 1$$

How many CPU clock cycles are needed to execute the "push r" instruction ?

(A) 2　　　　　　　　　　　　　　(B) 3

(C) 4　　　　　　　　　　　　　　(D) 5

Q. 10　　Which of the following does not interrupt a running process ?

(A) A device　　　　　　　　　　(B) Timer

(C) Scheduler process　　　　　　(D) Power failure

YEAR 2002

Q. 11　　A device employing INTR line for device interrupt puts the CALL instruction on the data bus while

(A) $\overline{INTA}$ is active　　　　　　(B) HOLD is active

(C) READY is active　　　　　　　(D) None of the above

Q. 12　　In 8085 which of the following modifies the program counter ?

(A) Only PCHL instruction　　　　(B) Only ADD instructions

(C) Only JMP and CALL instructions　(D) All instructions

Q. 13   In serial data transmission, every byte of data is padded with a '0' in the beginning and one or two '1's at the end of byte because
(A) Receiver is to be synchronized for byte reception
(B) Receiver recovers lost '0's and '1' from these padded bits
(C) Padded bits are useful in parity computation.
(D) None of the above

Q. 14   Which of the following is not a form of memory ?
(A) Instruction cache   (B) Instruction register
(C) Instruction opcode   (D) Translation-a-side buffer

Q. 15   In the C language
(A) At most one activation record exists between the current activation record and the activation record for the main.
(B) The number of activation records between the current activation record and the activation record for the main depends on the actual function calling sequence.
(C) The visibility of global variables depends on the actual function calling sequence.
(D) Recursion requires the activation record for the recursive function to be saved on a different stack before the recursive fraction can be called.

Q. 16   In the absolute the addressing mode
(A) The operand is inside the instruction
(B) The address of the operand is inside the instruction
(C) The register containing the address of the operand is specified inside the instruction
(D) The location of the operand is implicit

Q. 17   The performance of a pipelined processor suffers if
(A) The pipelined stages have different delays
(B) Consecutive instructions are dependent on each other
(C) The pipeline stages share hardware resources
(D) All the above

Q. 18   Horizontal microprogramming
(A) Does not require use of signal decoders
(B) Results in larger sized microinstructions than vertical microprogramming
(C) Uses one bit for each control signal
(D) All of the above

Q. 19   For a pipelined CPU with a single ALU, consider the following situations
1. The $j+1-st$ instruction uses the result of $j-th$ instruction as an operand
2. The execution of a conditional jump instruction
3. The $j-th$ and $j+1-st$ instructions require the ALU at the same time
Which of the above can cause a hazard?
(A) 1 and 2 only   (B) 2 and 3 only
(C) 3 only   (D) All the three

Q. 20   Consider an array multiplier for multiplying two n bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is
(A) $\Theta(1)$ (B) $\Theta(\log n)$
(C) $\Theta(n)$ (D) $\Theta(n^2)$

Q. 21   Consider the ALU shown below
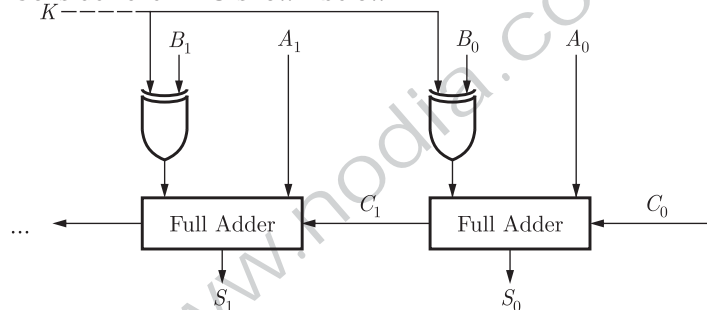
If the operands are in 2's complement representation, which of the following operations can be performed by suitably setting the control lines K and C_0 only (+ and - denote addition and subtraction respectively)?
(A) $A+B$, and $A-B$, but not $A+1$ (B) $A+B$, and $A+1$, but not $A-B$
(C) $A+B$, but not $A-B$, or $A+1$ (D) $A+B$, and $A-B$, and $A+1$

Common Data For Q. 22 & 23

Consider the following assembly language program for a hypothetical processor. A,B and C are 8 bit registers. The meanings of various instructions are shown as comments.

```
       MOV B, # 0      ; B←0
       MOV C, # 8      ; C←8
Z:     CMP C, # 0      ; compare C with 0
       JZX             ; jump to X if zero flag is set
       SUB C, # 1      ; C←C−1
       RRC A, # 1      ; right rotate A through carry
                       ; by one bit. Thus: if the
                       ; initial values of A and the
                       ; carry flag are a₇.......a₀ and c₀
                       ; respectively, their values
                       ; after the execution of this
                    ; instruction will be c₀a₇.....a₁
```

```
                                ; and a₀ respectively.
            JCY                 ;jump to Y if carry flag is set
            JMP Z               ; jump to Z
    Y:      ADD B, # 1          ; B←B+1
            JMP Z               ; jump to Z
    X:
```

Q. 22   If the initial value of register A is A_0, the value of register B after the program execution will be

(A) the number of 0 bits in A_0 (B) the number of 1 bits in A_0

(C) A_0 (D) 8

Q. 23   Which of the following instructions when inserted at location X will ensure that the value of register A after program execution is the same as its initial value?

(A) $RRC\ A, \#\ 1$

(B) NOP ;   no operation

(C) $LRC\ A, \#\ 1$;   left rotate A through carry flag by one bit

(D) $ADD\ A, \#\ 1$

Q. 24   Which of the following addressing modes are suitable for program relocation at run time?

1. Absolute addressing
2. Based addressing
3. Relative addressing
4. Indirect addressing

(A) 1 and 4   (B) 1 and 2

(C) 2 and 3   (D) 1,2 and 4

Q. 25   Consider a multiplexer with X and Y as data inputs and Z as control input. $Z = 0$ selects input X, and $Z=1$ selects input Y. What are the connection required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?

(A) R to X, 1 to Y, T to Z   (B) T to X, R to Y, T to Z

(C) T to X, R to Y, 0 to Z   (D) R to X, 0 to Y, T to Z

Common Data For Q. 26 & 27

Consider the following program segment for a hypothetical CPU having three user registers R1,R2 and R3.

Instruction	Operation	Instruction Size (in words)
MOV R1,5000	;R1←Memory[5000]	2
MOV R2,R3	;R2←R2+R3	1
ADD R2,R3	;R2←R2+R3	1
MOV 6000,R2	;Memory[6000]←R2	2
HALT	;Machine halts	1

Q. 26   Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be
(A) 1007   (B) 1020
(C) 1024   (D) 1028

Q. 27   Let the clock cycles required for various operations be as follows:
Register to/from memory transfer: 3 clock cycles
ADD with both operands in register: 1 clock cycle
Instruction fetch and decode: 2 clock cycles per word
The total number of clock cycles required to execute the program is
(A) 29   (B) 24
(C) 23   (D) 20

Q. 28   Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12,0, 12,8
(A) 2   (B) 3
(C) 4   (D) 5

Q. 29   The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.
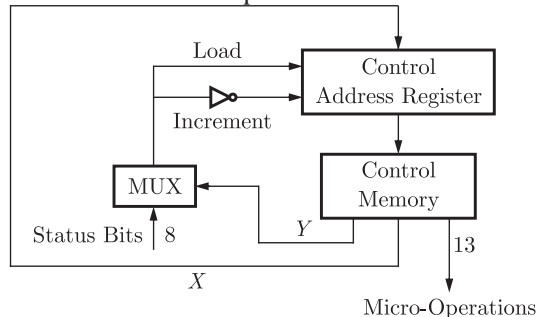
How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?
(A) 10, 3, 1024   (B) 8, 5, 256
(C) 5, 8, 2048   (D) 10, 3, 512

Q. 30   A hard disk with a transfer rate of 10 M bytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz. and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?
(A) 5.0%   (B) 1.0%
(C) 0.5%   (D) 0.1%

Q. 31   A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be
(A) 120.4 microseconds   (B) 160.5 microseconds
(C) 165.5 microseconds   (D) 590.0 microseconds

YEAR 2005   **ONE MARK**

Q. 32   Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?
(A) Neither vectored interrupt nor multiple interrupting devices are possible
(B) Vectored interrupts are not possible but multiple interrupting devices are possible
(C) vectored interrupts and multiple interrupting devices are both possible
(D) vectored interrupt is possible but multiple interrupting devices are not possible

Q. 33   Normally user programs are prevented from handing I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instructions privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?
(A) I/O protection is ensured by operating system routine(s)
(B) I/O protection is ensured by a hardware trap
(C) I/O protection is ensured during system configuration
(D) I/O protection is not possible

Q. 34   What is the swap apace in the disk used for?
(A) Saving temporary html pages   (B) Saving process data
(C) Storing the super-block   (D) Storing device drivers

Q. 35   Increasing the RAM of a computer typically improves performance because
(A) Virtual memory increases   (B) Larger RAMs are faster
(C) Fewer page faults occur   (D) Fewer segmentation faults occur

Q. 36   Consider a three word machine instruction

$$ADD\ A[R_0],@B$$

The first operand (destination) "$A[R0]$" uses indexed addressing mode with $R0$ as the index register. The second operand (source) "$@B$" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand). The number of memory cycles needed during the execution cycle of the instruction is

(A) 3   (B) 4

(C) 5   (D) 6

Q. 37   Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	List-II
A. $A[1] = B[j]$;	**1.** Indirect addressing
B. while [* $A++$];	**2.** Indexed addressing
C. int temp=*x;	**3.** Auto increment

Codes:

	A	B	C
(A)	3	2	1
(B)	1	3	2
(C)	2	3	1
(D)	1	2	3

Q. 38   Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively

(A) 10,17   (B) 10,22

(C) 15,17   (D) 5,17

Q. 39   A 5 stage pipelined CPU has the following sequence of stages

IF-Instruction fetch from instruction memory.

RD-Instruction decode and register read,

EX- Execute:ALU operation for data and address computation,

MA-Data memory access-for write access the register read at

RD stage it used,

WB-register write back.

Consider the following sequence of instruction:

$$I_1 : LR0, \text{Locl};\ R0 <= M[\text{Locl}]$$

$$I_2\ \ AR0, R0;\ R0 <= R0 + R0$$

$$I_3\ \ AR2, R0;\ R2 <= R2 - R0$$

Let each stage take one clock cycle.

What is the number of clock cycles taken to complete the above sequence of instruction starting from the fetch of I_1?

(A) 8   (B) 10

(C) 12   (D) 15

Q. 40   A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 μsec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

(A) 15   (B) 25

(C) 35   (D) 45

Q. 41   Consider a disk drive with the following specification
16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 *rpm*. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 *n*sec . The maximum percentage of time that the CPU gets blocked during DMA operation is

(A) 10   (B) 25

(C) 40   (D) 50

Common Data For Q. 42 & 43

Consider the following data path of a CPU
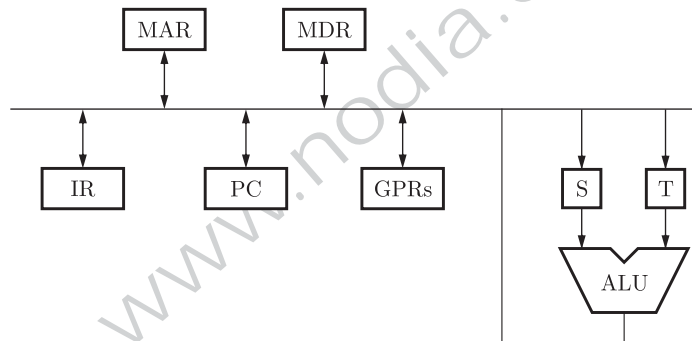
The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycle are needed for memory read operation-the first one for loading data from the memory but into the MDR.

Q. 42   The instruction "add $R0, R1$" has the register transfer in terpretation $R0 <= R0 + R1$. The minimum number of clock cycles needed for execution cycle of this instruction is

(A) 2   (B) 3

(C) 4   (D) 5

Q. 43   The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is $Rn <= PC = 1;$, $PC <= M[PC];$. The minimum number of CPU clock cycles needed during the execution cycle of this instruction is

(A) 2   (B) 3

(C) 4   (D) 5

Q. 44   A CPU has 24-bit instructions. A program starts at address 300(in decimal). Which one of the following is a legal program counter (all values in decimal)?

(A) 400   (B) 500

(C) 600   (D) 700

YEAR 2006   **TWO MARKS**

Q. 45   A CPU has a cache with block size 64 bytes. The main memory has k banks, each bank being c bytes wide. Consecutive c-bute chunks are mapped on consecutive banks with warp-around. All the k banks can be accessed in parallel, but two accesses to the same bank must be serialized. A cache block access may involve multiple iterations of parallel bank accesses depending on the amount of data obtained by accessing all the k banks in parallel. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes $k/2$ ns. The latency of one bank access is 80 ns. If $c = 2$ and $k = 24$, then latency of retrieving a cache block starting at address zero from main memory is

(A) 92 ns (B) 104 ns

(C) 172 ns (D) 184 ns

Q. 46   A CPU has five-stages pipeline and runs at $1GHz$ frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, then total execution time of the program is

(A) 1.0 second   (B) 1.2 seconds

(C) 1.4 seconds   (D) 11.6 seconds

Q. 47   Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction "bbs reg, pos, labbel" jumps to label if bit in position pos of register operand reg is one. a register is 32 bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

temp←reg and mask

Branch to label if temp is non-zero

The variable temp is a temporary register. For correct emulation the variable mask must be generated by

(A) mask← $0x1 << pos$ (B) musk← $0x$ $ffffffff >> pos$

(C) mask← pos (D) msdk← $0xf$

Common Data For Q. 48 & 49

Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-bytes block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases A2-to-1 multiplexes has latency of 0.6 ns where a k-bit comparator has a latency of $k/10ns$. The hit latency of the set associative organization is h_1 while that of the direct mapped one is h_2.

Q. 48   The value of h_1 is
            (A) $2.4ns$ (B) $2.3ns$
            (C) $1.8ns$ (D) $1.7ns$

Q. 49   The value of h_2 is
            (A) $2.4ns$ (B) $2.3ns$
            (C) $1.8ns$ (D) $1.7ns$

Common Data For Q. 50 & 51

A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, P_1 and P_2,

```
P1 : for (i=0;i<512;i++)
{
      for (j=0;j<512;j++)
{
            x+=A[i][j];
      }
}
P2 : for (i=0;i<512;i++) {
            for (j=0;j<512;j++) {
      {x+=A[j][i];}
      }
}
```

P1 and P2are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by P1 be M_1 and that for P2 be M_2.

Q. 50   The value of M_1 is
            (A) 0   (B) 2048
            (C) 16384   (D) 262144

Q. 51   The value of the ratio M_1/M_2 is
            (A) 0   (B) 1/16
            (C) 1/8   (D) -16

YEAR 2007   **ONE MARK**

Q. 52   Consider a 4-way set associative cache consisting of 120 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively
            (A) 9,6,5   (B) 7,7,6
            (C) 7,5,8   (D) 9,5,6

Q. 53   Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively

(A) 256 Mbytes, 19 bits   (B) 256 Mbyte, 28 bits

(C) 512 Mbytes, 20 bits   (D) 64 Gbyte, 28 bits

YEAR 2007   **TWO MARKS**

Q. 54   Consider a pipelined processor with the following four stages
```
IF: Instruction Fetch
ID: Instruction Decode and Operand Fetch
EX: Execute
WB: Write Bank
```

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD	R2,	R1,	R0	R2←R1+R0
MUL	R4,	R3,	R2	R4←R3*R2
SUB	R6,	R5,	R4	R6←R5−R4

(A) 7   (B) 8

(C) 10   (D) 14

Common Data For Q. 55, 56 & 57

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

Instruction	Operation	Instruction size (no. of words)
MOV R1,(3000)	R1←M[3000]	2
LOOP:		
MOV R2,R1	R2←M[R3]	1
ADD R2,R1	R2←R1+R2	1
MOV (R3),R2	M(R3]←R2	1
INC R3	R3←R3+1	1
DEC R1	R1←R1−1	1
BNZ LOOP	Branch on not zero	2
HALT	Stop	

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 100. All the numbers are in decided.

Q. 55   Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

(A) 10   (B) 11

(C) 20   (D) 21

Q. 56   Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is

(A) 100   (B) 101

(C) 102   (D) 110

Q. 57   Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack?

(A) 1005   (B) 1020

(C) 1024   (D) 1040

Common Data For Q. 58 & 59

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50×50 two-dimensional array of bytes is stored in the main memory stating from memory location 1100H.Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Q. 58   How many data cache misses will occur in total?

(A) 48   (B) 50

(C) 56   (D) 59

Q. 59   Which of the following lines of the data cache will be replaced by new blocks in accessing the array

(A) line 4 to line 11   (B) line 4 to line 12

(C) line 0 to line 7   (D) line 0 to line 8

YEAR 2008   **TWO MARKS**

Q. 60   For a magnetic disk with concentric circular track, the latency is not linearly proportional to the seek distance due to

(A) non-uniform distribution of requests

(B) arm starting and stopping inertia

(C) higher capacity of tracks on the periphery of the platter

(D) use of unfair arm scheduling policies.

Q. 61   Which of the following is/are true of the auto increment addressing mode?

1. It is useful in creating self relocating code

2. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation

3. The amount of increment depends on the size of the data item accessed.

(A) 1 only   (B) 2 only

(C) 3 only   (D) 2 and 3 only

Q. 62   Which of the following must be true for the RFE (Return from Expectation) instruction on a general purpose processor.
1. It must be a trap instruction
2. It must be a privileged instruction
3. An exception can not be allowed to occur during execution of an RFE instruction.
(A) 1 only   (B) 2 only
(C) 1 and 2 only   (D) 1, 2 and 3 only

Q. 63   For inclusion to hold between two cache level L1 and L2 in a multilevel cache hierarchy, which of the following are necessary?
1. L1 must be a write-through cache
2. L2 must be write-through cache
3. The associativity of L2 must be greater that of L1
4. The L2 cache must be at least as large as the L1 cache
(A) 4 only   (B) 1 and 2 only
(C) 1, 2 and 4 only   (D) 1, 2, 3 and 4

Q. 64   Which of the following are NOT true in a pipe lined processor?
1. Bypassing can handle alll Raw hazards.
2. Register renaming can eliminate all register carried WAR hazards.
3. Control hazard penalties can be eliminated by dynamic branch prediction.
(A) 1 and 2 only   (B) 1 and 3 only
(C) 2 and 3 only   (D) 1,2 and 3

Q. 65   The use of multiple register windows with overlap causes a reduction in the number of memory accesses for
1. Function locals and parameters
2. Register saves and restores
3. Instruction fetches
(A) 1 only   (B) 2 only
(C) 3 only   (D) 1,2 and 3

Q. 66   In an instruction execution pipeline, the earliest that the data TLB (Translation Look aside Buffer) can be accessed is
(A) before effective address calculation has started
(B) during effective address calculation
(C) after effective address calculation has completed
(D) after data cache lookup has completed

Common Data For Q. 67, 68 & 69

Consider a machine a 2-way set associative data cache of size 64 kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addressed and the page size is 4 kbytes. A program to be run on this machine begins as follows:
```
Double APR[1024]]1024]
int i,j;
/*Initalize array APR to 0.0*/
for  (i = 0;i < 1024;i ++)
for    (j = 0;k < 1024;j ++)
APR[i][j] = 0.0;
```

The size of double 8 bytes. Array APR is in memory stating at the beginning of virtual page $0 \times FF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array APR.

Q. 67   The total size of the tags in the cache directory is
(A) 32 kbits   (B) 34 kbits
(C) 64 kbits   (D) 68 kbits

Q. 68   Which of the following array elements has the same cache index as APR [0][0]?
(A) APR[0][4]   (B) APR[4][0]
(C) APR[0][5]   (D) APR[5][0]

Q. 69   The cache hit ratio for this initialization loop is
(A) 0%   (B) 25%
(C) 50%   (D) 75%

Common Data For Q. 70 & 71

Delayed branching can help in the handling of control hazardous

Q. 70   For all delayed conditional branch instruction, irrespective of weather the condition evato true or false, A
(A) the instruction following the conditional branch instruction in memory is executed
(B) the first instruction in the fall through path is executed
(C) the first instruction in the taken path is executed
(D) the branch takes longer to execute that any other instruction

Q. 71   The following code is to run on a pipe lined processor with one branch delay slot
```
11: ADD   R2 ← R7+R8
12: SUB   R4 ← R5− R6
13: ADD R1 ← R2+ R3
14: STORE Memory [R4] ←  R1
BRANCH to Label if R1==0
```
Which of the instruction 11,12,13 or 14 can legitimately occupy the delay slot without any other program modification?
(A) 11   (B) 12
(C) 13   (D) 14

Q. 72   How many 32K×1 RAM chips are needed to provide a memory capacity of 356-bytes ?
(A) 8   (B) 32
(C) 64   (D) 128

Q. 73   A CPU generally handles are interrupt by executing an interrupt service routine
         (A) As soon as an interrupt is raised
         (B) By checking the interrupt register at the end of fetch cycle
         (C) By checking the interrupt register after finishing the execution of the
             current instruction
         (D) By checking the interrupt register at fixed time intervals

Q. 74   Consider a 4 stage pipeline processor. The number of cycles needed by the four
         instructions 11, 12, 13, 14 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	2	3	2	2
I3	2	1	1	3
I4	1	2	2	2

         What is the number of cycles needed to execute the following loop?
                   for ($i = 1\ to\ 2$){I1; I2; I3; I4;}
         (A) 16   (B) 23
         (C) 28   (D) 30

Q. 75   Consider a 4 way set associative cache (initially empty) with total 16 cache
         blocks. The main memory consists of 256 blocks and the request for memory
         blocks is in the following order :
         0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155
         Which one of the following memory block will NOT be in the cache if LRU
         replacement policy is used ?
         (A) 3   (B) 8
         (C) 129   (D) 216

Common Data For Q. 76 & 77

         A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces
         and 1000 cylinders. The address of a sector is given as a triple $\langle c, h, s \rangle$, where c is
         the cylinder number, h is the surface number and s is the sector number. Thus,
         the 0th sector is addressed as $\langle 0, 0, 0 \rangle$, the 1st sector as $\langle 0, 0, 1 \rangle$, and so on.

Q. 76   The address $\langle 400, 16, 29 \rangle$, corresponds to sector number:
         (A) 505035   (B) 505036
         (C) 505037   (D) 505038

Q. 77   The address of 1039th sector is
         (A) $\langle 0, 15, 31 \rangle$ (B) $\langle 0, 16, 30 \rangle$
         (C) $\langle 0, 16, 31 \rangle$ (D) $\langle 0, 17, 31 \rangle$

Q. 78   A main memory unit with a capacity of 4 megabytes is build using $1M \times 1 -$ bit DRAM chips. Each DRAM chip has 1K rows of cells with 1 K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

(A) 100 nanoseconds   (B) $100*2^{10}$ nanoseconds

(C) $100*2^{20}$ nanoseconds   (D) $3200*2^{20}$ nanoseconds

Q. 79   A-5 stage pipelined processor has Instruction Fetch. (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instruction. The PO stage takes 1 stake clock cycle for ADD and SUB instructions 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions ?

Instruction Meaning of instruction

I_0: MUL R_2, R_0, R_1 $R_2 \leftarrow R_0 * R_1$

I_1: DIV R_5, R_3, R_4 $R_5 \leftarrow R_3 / R_4$

I_2: ADD R_2, R_5, R_2 $R_2 \leftarrow R_5 + R_2$

I_3: SUB R_5, R_2, R_6 $R_5 \leftarrow R_2 - R_6$

(A) 13   (B) 15

(C) 17   (D) 19

Q. 80   The program below uses six temporary variables a, b, c, d, e, f

$a = 1$ $b = 10$ $c = 20$

$d = a + b$ $e = c + d$ $f = c + e$

$b = c + e$ $e = b + f$ $d = 5 + e$

Assuming that all operations take their operands from register, what is the minimum number of registers needed to execute this program without spilling ?

(A) 2   (B) 3

(C) 4   (D) 6

Common Data For Q. 81 & 82

A computer system has an L1 and L2 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size is L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unity respectively.
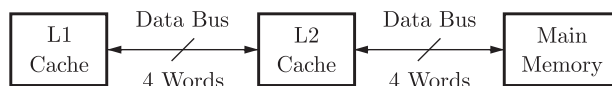
Q. 81   When there is a miss in L1 cache and a hit in L2 cache, a block is transferred form L2 cache to L1 cache. What is the time taken for this transfer ?
(A) 2 nanoseconds   (B) 20 nanoseconds
(C) 22 nanoseconds   (D) 88 nanoseconds

Q. 82   When there is a miss in both L1 cache and L2 cache, first a block is transferred from memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers ?
(A) 222 nanoseconds   (B) 888 nanoseconds
(C) 902 nanoseconds   (D) 968 nanoseconds

YEAR 2011   **ONE MARK**

Q. 83   Consider a hypothetical processor with a instruction of type LWR1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?
(A) Immediate Addressing
(B) Register Addressing
(C) Register Indirect Scaled Addressing
(D) Base Indexed Addressing

YEAR 2011   **TWO MARKS**

Q. 84   On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.
```
Initialize the address register
Initialize the count to 500 LOOP:Load a byte from device
Store in memory at address given by address register
Increment the address register
Decrement the court
If count! = 0 go to LOOP
```
Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.
The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overhead. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from interrupt driven program based input-output?
(A) 3.4   (B) 4.4
(C) 5.1   (D) 6.7

Q. 85   Consider evaluating the following expression tree on a machine with loadstore architecture in which memory can be accessed only through load and store instructions. The variables a, b, c, d and e are initially stored in memory. The binary operators used in this expression tree can be evaluated by the machine only when the operands are in registers. The instructions produce result only in a register. If no intermediate results can be stored in memory, what is the minimum number of registers needed to evaluate this expression?

(A) 2   (B) 9
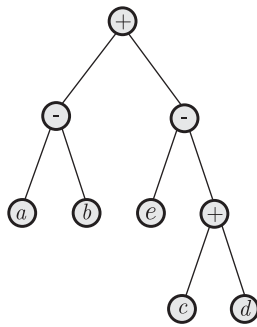
(C) 5   (D) 3

Q. 86   Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure.
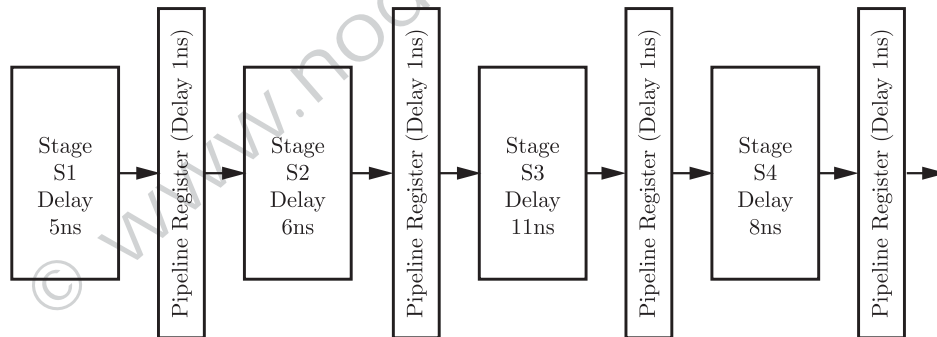
What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

(A) 4.0   (B) 2.5

(C) 1.1   (D) 3.0

Q. 87   An 8 KB direct-mapped write back cache is organized as multiple blocks, each of size 32 bytes. The processor generates 32 bit addresses. The cache controller maintains the tag information for each cache block comprising of the following.

1 Valid bit   1 Modified bit

As many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

(A) 4864 bits   (B) 6144 bits

(C) 6656 bits   (D) 5376 bits

Q. 88   The decimal value 0.5 in IEEE single precision floating point representation has
(A) fraction bits of 000 ... 000 and exponent value of 0

(B) fraction bits of 000 ... 000 and exponent value of –1

(C) fraction bits of 100 ... 000 and exponent value of 0

(D) no exact representation

Q. 89   The amount of ROM needed to implement at 4 bit multiplier is
(A) 64 bits   (B) 128 bits

(C) 1 K bits   (D) 2 K bits

Q. 90   Register renaming is done in pipelined processors
(A) as an alternative to register allocation at compile time

(B) for efficient access to function parameters and local variables

(C) to handle certain kinds of hazards

(D) as part of address translation

Statement For Linked Q. 91 and 92 :

A computer has a 256 Kbyte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 2 replacement bit.

Q. 91   The number of bits in the tag field of an address is
(A) 11   (B) 14

(C) 16   (D) 27

Q. 92   The size of the cache tag directory is
(A) 160 Kbits   (B) 136 Kbits

(C) 40 Kbits   (D) 32 Kbits

****

ANSWER KEY

Computer Organization & Architecture									
1	2	3	4	5	6	7	8	9	10
(A)	(D)	(A)	(C)	(B)	(C)	(D)	(A)	(B)	(C)
11	12	13	14	15	16	17	18	19	20
(A)	(D)	(A)	(C)	(A)	(D)	(D)	(C)	(D)	(C)
21	22	23	24	25	26	27	28	29	30
(D)	(A)	(A)	(C)	(A)	(C)	(B)	(C)	(A)	(D)
31	32	33	34	35	36	37	38	39	40
(C)	(B)	(A)	(B)	(C)	(D)	(C)	(A)	(B)	(B)
41	42	43	44	45	46	47	48	49	50
(B)	(B)	(B)	(C)	(D)	(C)	(A)	(A)	(B)	(A)
51	52	53	54	55	56	57	58	59	60
(B)	(B)	(A)	(B)	(D)	(A)	(A)	(C)	(A)	(C)
61	62	63	64	65	66	67	68	69	70
(C)	(D)	(A)	(D)	(C)	(B)	(B)	(B)	(C)	(B)
71	72	73	74	75	76	77	78	79	80
(B)	(C)	(C)	(B)	(D)	(C)	(C)	(D)	(C)	(B)
81	82	83	84	85	86	87	88	89	90
(D)	(D)	(D)	(A)	(D)	(B)	(D)	(C)	(D)	(C)
91	92								
(C)	(A)								