GATE SOLVED PAPER
Computer Science Engineering
Digital Logic

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GATE SOLVED PAPER - CS

DIGITAL LOGIC

YEAR 2001

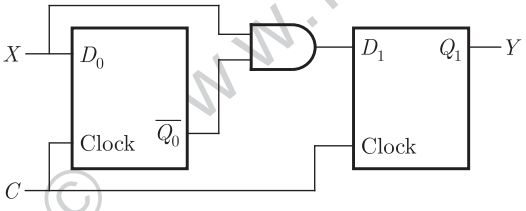
Q. 1 Given the following Karnaugh map, which one of the following represents the minimal sum-of-Products of the map ?

yz \ wx	00	01	11	10
00	0	×	0	×
01	×	1	×	1
11	0	×	1	0
10	0	1	1	×

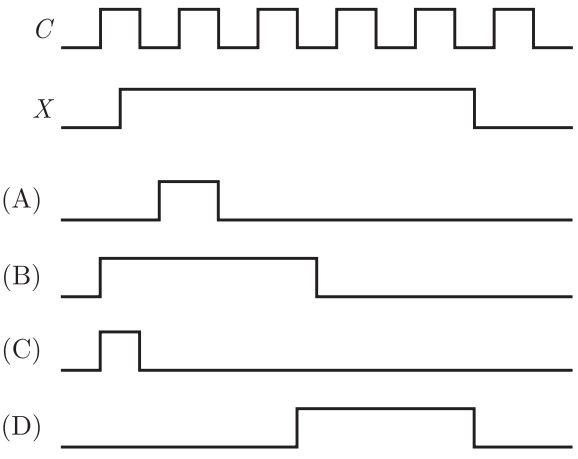
(A) $xy + y'z$ (B) $wx'y' + xy + xz$

(C) $w'x + y'z + xy$ (D) $xz + y$

Q. 2 Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



Consider the following timing diagrams of X and C; the clock of $C \geq 40$ nanosecond. Which one is the correct plot of Y

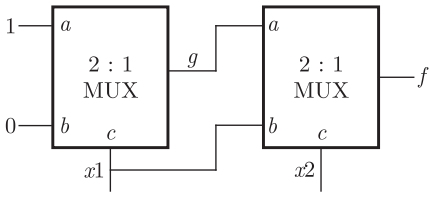


Q. 3 The 2's complement representation of $(-539)_{10}$ is hexadecimal is

(A) ABE (B) DBC

(C) DE5 (D) 9E7

Q. 4 Consider the circuit shown below. The output of a 2:1 Mux is given by the function $(ac' + bc)$.

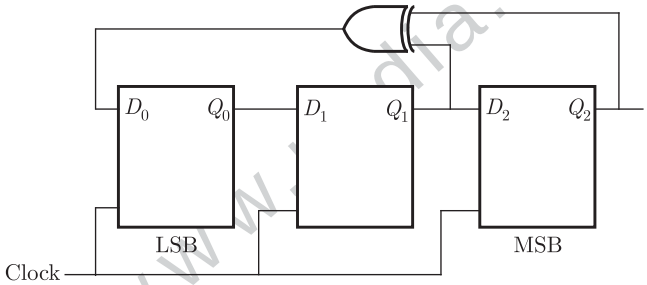


Which of the following is true ?

(A) $f = x1' + x2$ (B) $f = x1'x2 + x1x2'$

(C) $f = x1x2 + x1'x2'$ (D) $f = x1 + x2$

Q. 5 Consider the circuit given below the initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$



Which one of the following is the correct state sequence of the circuit ?

(A) 1, 3, 4, 6, 7, 5, 2 (B) 1, 2, 5, 3, 7, 6, 4

(C) 1, 2, 7, 3, 5, 6, 4 (D) 1, 6, 5, 7, 2, 3, 5

YEAR 2002

Q. 6 Minimum sum of product expression for $f(w,x,y,z)$ shown in Karnaugh-map below is

yz \ wx	00	01	11	10
00	0	1	1	0
01	×	0	0	1
11	×	0	0	1
10	0	1	1	×

(A) $xz + y'z$ (B) $xz' + zx'$

(C) $x'y + zx'$ (D) None of the above

Q. 7 The decimal value of 0.25

(A) is equivalent to the binary value 0.1

(B) is equivalent to the binary value 0.01

(C) is equivalent to the binary value 0.00111.....

(D) cannot be represented precisely in binary.

Q. 8 The 2's complement represent representation of the decimal value -15 is

(A) 1111 (B) 11111

(C) 111111 (D) 10001

Q. 9 Sign extension is a step in

(A) floating point multiplication

(B) signed 16 bit integer addition

(C) arithmetic left shift

(D) converting a signed integer from one size to another.

Q. 10 In 2's complement addition, overflow

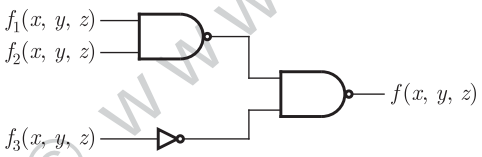
(A) Relational algebra is more powerful than relational calculus

(B) Relational algebra has the same power as relational calculus.

(C) Relational algebra has the same power as safe relational calculus.

(D) None of the above.

Q. 11 Consider the following logic circuit whose inputs are functions f_1, f_2, f_3 and output is f



Given that

$$f_1(x,y,z) = \Sigma(0,1,3,5)$$

$$f_2(x,y,z) = \Sigma(6,7), \text{ and}$$

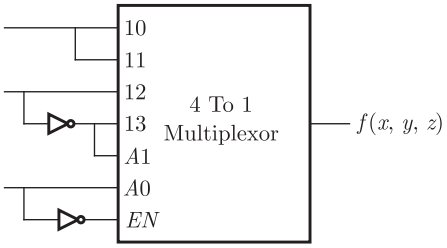
$$f(x,y,z) = \Sigma(1,4,5)$$

f_3 is

(A) $\Sigma(1,4,5)$ (B) $\Sigma(6,7)$

(C) $\Sigma(0,1,3,5)$ (D) None of the above

Q. 12 Consider the following multiplexor where 10, 11, 12, 13 are four data input lines selected by two address line combinations $A1A0 = 00, 01, 10, 11$ respectively and f is the output of the multiplexor. EN is the Enable input.



The function $f(x,y,z)$ implemented by the above circuit is

(A) xyz' (B) $xy+z$

(C) $x+y$ (D) None of the above

Q. 13 Let $f(A,B)=A'+B$. Simplified expression for function $f(f(x+y,y),z)$ is

(A) $x'+z$ (B) xyz

(C) $xy'+z$ (D) None of the above

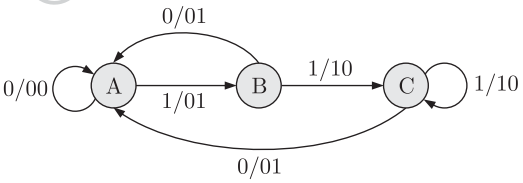
Q. 14 What are the states of the Auxiliary Carry (AC) and Carry Flag (CY) after executing the following 8085 program ?

```
MIV  H,   5DH
MIV  L,   6BH
MOV  A,   H
ADD  L
```

(A) $AC=0$ and $CY=0$ (B) $AC=1$ and $CY=1$

(C) $AC=1$ and $CY=0$ (D) $AC=0$ and $CY=1$

Q. 15 The finite state machine described by the following state diagram with A as starting state, where an arc label is $\frac{x}{y}$ and x stands for 1-bit input and y stands for 2-bit output.



(A) Outputs the sum of the present and the previous bits of the input.

(B) Outputs 01 whenever the input sequence contains 11

(C) Outputs 00 whenever the input sequence contains 10

(D) None of the above.

YEAR 2003 ONE MARK

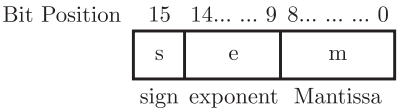
Q. 16 Assuming all numbers are in 2's complement representation, which of the following number is divisible by 11111011?

(A) 11100111 (B) 11100100

(C) 11010111 (D) 11011011

YEAR 2003 TWO MARKS

Q. 17 The following is a scheme for floating point number representation using 16 bits.



Let s, c and m be the number represented in binary in the sign, exponent, and mantissa fields respectively. Then the flouting point number represented id

$$\begin{cases}(-1)^2(1+m\times 2^{-9})2^{e-31}, \text{ if the exponent } 111111\\ 0 \text{ otherwise}\end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

(A) 2^{-40} (B) 2^{-9}

(C) 2^{22} (D) 2^{31}

Q. 18 A 1-input, 2-output synchronous sequential circuit behaves as follows.
Let z_k, n_k denote the number of 0's and 1's respectively in initial k bits of the input ($z_k + n_k = k$). The circuit outputs 00 until one of the following conditions holds.
1. $n_k - n_k = 2$. In this case, the output at the k-th and all subsequency clock ticks is 10.
2. $n_k - z_k = 2$. In this case, the output at the k-th and all subsequent clock ticks is 01.
What in the minimum number of states required in the state transition graph of the above circuit?

(A) 5 (B) 6

(C) 7 (D) 8

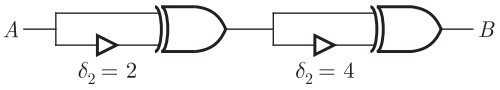
Q. 19 The literal count of a boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of $(xy + xz)$ is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following karnaugh map?
Here, × denotes "don't care"

xy \ zw	00	01	11	10
00	×	1	0	1
01	0	1	×	0
11	1	×	×	0
10	×	0	0	×

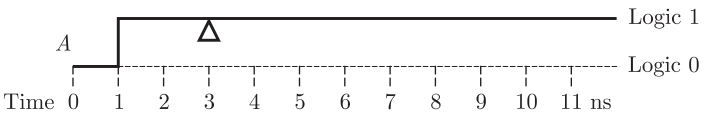
(A) (11,9) (B) (9,13)

(C) (9,10) (D) (11,11)

Q. 20 Consider the following circuit composed of XOR gates and non-inverting buffers.



The non-inverting buffers have delays $\delta_1 = 2ns$ and $\delta_2 = 4ns$ as shown in the figure. both XOR gates and al wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0. If the following waveform is applied at input. A, how many transition (s) (change of logic levels) occur (s) at B during the interval from 0 to 10 *ns*?



(A) 1 (B) 2

(C) 3 (D) 4

YEAR 2004 ONE MARK

Q. 21 The Boolean function $x'y' + xy + x'y$ is equivalent to

(A) $x' + y'$ (B) $x + y$

(C) $x + y'$ (D) $x' + y$

Q. 22 In an *SR* latch made by cross-coupling two NAND gates, if both *S* and *R* inputs are set to 0, then it will result in

(A) $Q = 0, Q' = 1$ (B) $Q = 1, Q' = 0$

(C) $Q = 1, Q' = 1$ (D) Indeterminate states

Q. 23 If 73_x (in base-x number system) is equal to 54, (in base-y number system), the possible values of x and y are

(A) 8, 16 (B) 10, 12

(C) 9, 13 (D) 8, 11

Q. 24 What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

$(113. + -111.) + 7.51$

$113. + (-111. + 7.51)$

(A) 9.51 and 10.0 respectively (B) 10.0 and 9.51 respectively

(C) 9.51 and 9.51 respectively (D) 10.0 and 10.0 respectively

YEAR 2004 TWO MARKS

Q. 25 A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001,...9 by 1001. A combinational circuit is to be diesigned which takes these 4 bits as input and outputs 1 if the digit ≥ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

(A) 2 (B) 3

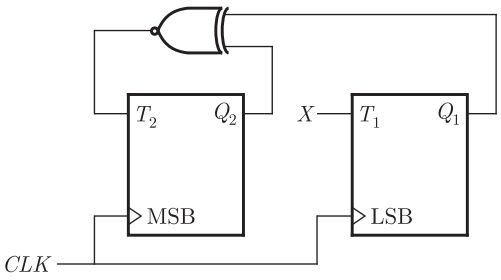
(C) 4 (D) 5

Q. 26 Which are the essential prime implicates of the following Boolean function?
$f(a,b,c) = a'c + ac' + b'c$

(A) $a'c$ and ac' (B) $a'c$ and $b'c$

(C) $a'c$ only (D) ac' and bc'

Q. 27 Consider the partial implementation fo a 2-bit counter using T flip flops following the sequence 0-2-3-1-0, as shown below



To complete the circuit, the input X should be

(A) Q_2' (B) $Q_2 + Q_1$

(C) $(Q_1 \oplus Q_2)'$ (D) $Q_1 \oplus Q_2$

Q. 28 A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncompensated forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

(A) 4 time units (B) 6 time units

(C) 10 time units (D) 12 time units

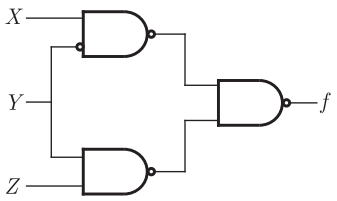
Q. 29 Let $A = 11111010$ and B 0000 1010 be two 8-bit 2's complement numbers. Their product in 2's complement is

(A) 1100 0100 (B) 1001 1100

(C) 1010 0101 (D) 1101 0101

YEAR 2005 ONE MARK

Q. 30 Consider the following circuit.



Which one of the following is TRUE?

(A) f is independent of X (B) f is independent of Y

(C) f is independent of Z (D) None of X, Y, Z is redundant

Q. 31 The range of integers that can be represented by an a bit 2's complement number system is

(A) -2^{n-1} to $(2^{n-1}-1)$ (B) $-(2^{n-1}-1)$ to $(2^{n-1}-1)$

(C) -2^{n-1} to 2^{n-1} (D) $-(2^{n-1}+1)$ to $(2^{n-1}-1)$

Q. 32 The hexadecimal representation of 657_8 is

(A) 1AF (B) D78

(C) D71 (D) 32F

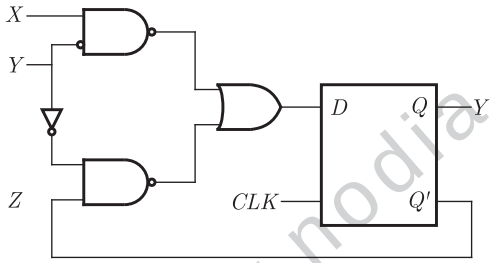
Q. 33 The switching expression corresponding to $f(A,B,C,D) = \sum(1,4,5,9,11,12)$ is

(A) $BC'D' + A'C'D + AB'D$ (B) $ABC' + ACF + B'C'D$

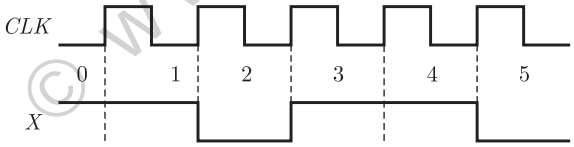
(C) $ACD' + A'BC' + AC'D'$ (D) $A'BD + ACD' + BCD'$

YEAR 2005 TWO MARKS

Q. 34 Consider the following circuit involving a positive edge triggered D-FF.



Consider the following timing diagram. Let Ai represent the logic level on the line A in the $i-th$ clock period.

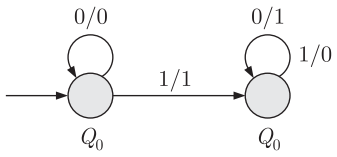


Let A represent the complement of A. The correct output sequence on Y over the clock perids 1 through 5 is

(A) $A_0A_1A_1'A_3A_4$ (B) $A_0A_1A_2'A_3A_4$

(C) $A_1A_2A_2'A_3A_4$ (D) $A_1A_2'A_3A_4A_5$

Q. 35 The following diagram represents a finite state machine which takes as input a binary number from the least significant bit



Which one of the following is TRUE?

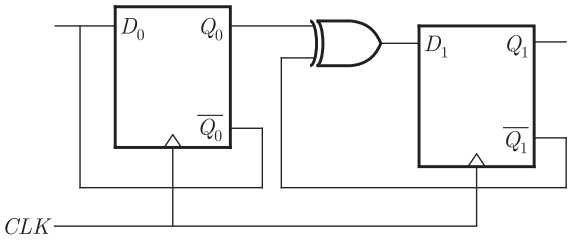
(A) It computes 1's complement of the input number

(B) It computes 2's complement of the input number

(C) It increments the input number

(D) It decrements the input number

Q. 36 Consider the following circuit



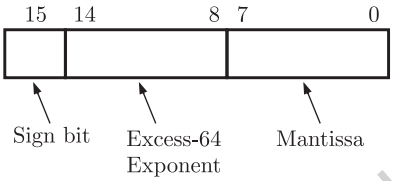
The flip-flops are positive edge triggered $DFFs$. Each state is designated as a two bit string Q_0, Q_1. Let the initial state be 00. The state transition sequence is

(A) $\underline{00 \rightarrow 11 \rightarrow 01}$ (B) $\underline{00 \rightarrow 11}$

(C) $\underline{00 \rightarrow 10 \rightarrow 01 \rightarrow 11}$ (D) $\underline{00 \rightarrow 11 \rightarrow 01 \rightarrow 10}$

Common Data For Q. 37 & 38

Solve the problems and choose the correct answers.
Consider the following floating point format



Mantissa is a pure fraction is sign-magnitude form.

Q. 37 The decimal number 0.239×2^{13} has the following hexadecimal representation without normalization and rounding off

(A) 0*D* 24 (B) 0*D* 4*D*

(C) 4*D* 0*D* (D) 4*D* 3*D*

Q. 38 The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field. The normalized representation of the above number (0.239×2^{13}) is

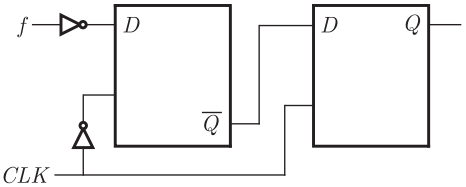
(A) 0*A* 20 (B) 11 34

(C) 4*D* *D*0 (D) 4*A* *E*8

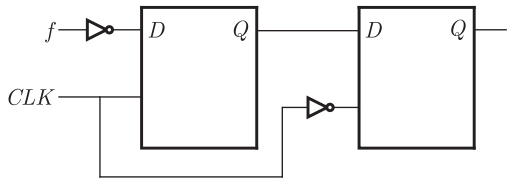
YEAR 2006 ONE MARK

Q. 39 You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip flops) will delay the phase of f by 180° ?

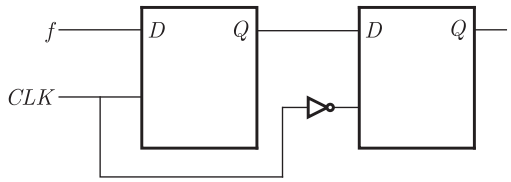
(A)



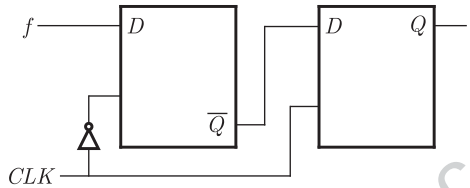
(B)



(C)

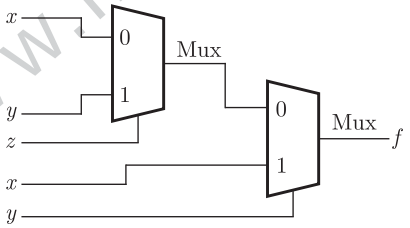


(D)



YEAR 2006 TWO MARKS

Q. 40 Consider the circuit below. Which one of the following options correctly represents $f(x,y,z)$?



(A) $x\bar{z}+xy+\bar{y}z$ (B) $x\bar{z}+xy+y\bar{z}$

(C) $xz+xy+\bar{y}\bar{z}$ (D) $xz+x\bar{y}+\bar{y}z$

Q. 41 Given two three bit numbers $a_2a_1a_0$ and $b_2b_1b_0$ and c, the carry in, the function that represents the carry generate function when these two numbers are added is

(A) $a_2b_2+a_1a_1b_1+a_2a_1a_0b_0+a_2a_0b_1b_0+a_1b_2b_1+a_1a_0b_2b_0+a_0b_2b_1b_0$

(B) $a_2b_2+a_2b_1b_0+a_2a_1b_1b_0+a_1a_0b_{21}b_1+a_1a_0b_2+a_1a_0b_2b_0+a_2a_0b_1b_0$

(C) $a_2+b_2+(a_2\oplus b_2)[a_1+b_1+(a_1\oplus b_1)(a_0+b_0)]$

(D) $a_2b_2+\overline{a_2}a_1b_1+\overline{a_2a_1}a_0b_0+\overline{a_2}a_0\overline{b_1}b_0+a_1\overline{b_2}b_1\overline{a_1}a_0\overline{b_2}b_0+a_0\overline{b_2b_1}b_0$

Q. 42 Consider a boolean function $f(w,x,y,z)$. Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors $i_1+<w_1,x_1,y_1,x_1>$ and $i_2+<w_2,x_2,y_2,z_2>$, we would like the function to remain true as the input changes from i_1 to i_2(i_1 and i_2 differ in exactly one bit position), without becoming false momentarily. Let $f(w,x,y,z)=\sum(5,,711,12,13,15)$. Which of the following cube covers of f will ensure that the required property is satisfied?

(A) $\bar{w}xz,wx\bar{y},x\bar{y}z,xyz,wyz$ (B) $wxy,\bar{w}xz,wyz$

(C) $wx\bar{y}\bar{z},xz,w\bar{x}yz$ (D) $wzy,wyz,wxz,\bar{w}\bar{w}xz,x\bar{y}z,xyz$

Q. 43 We consider addition of two 2's complement numbers $b_{n-1}b_{n-2}.....b_0$ and $a_{n-1}a_{n-2}....a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}....c_0$ and the carryout by c_{out}. Which one of the following options correctly identifies the overflow condition?

(A) $c_{out}\overline{(a_{n-1} \oplus b_{n-1})}$ (B) $a_{n-1}b_{n-1}\overline{c_{n-1}} + \overline{a_{n-1}b_{n-1}c_{n-1}}$

(C) $c_{out} \oplus c_{n-1}$ (D) $a_{n-1} \oplus b_{n-1} \oplus c_{n-1}$

Q. 44 Consider number represented in 4-bit gray code. Let $h_3h_2h_1h_0$ be the gray code representation of a number n and let $g_3g_2g_1g_0$ be the gray code of $(n+1)$ (modulo 16) value of the number. Which one of the following functions is correct?

(A) $g_0(h_1h_2h_1h_0) = \sum(1,2,3,6,10,13,14,15)$

(B) $g_1(h_1h_2h_1h_0) = \sum(4,9,10,11,12,,13,14,15)$

(C) $g_2(h_1h_2h_1h_0) = \sum(2,4,5,6,7,12,,13,15)$

(D) $g_3(h_1h_2h_1h_0) = \sum(0,1,6,7,10,11,12,,13,)$

YEAR 2007 ONE MARK

Q. 45 What is the maximum number of different Boolean functions involving n Boolean variables?

(A) n^2 (B) 2^n

(C) 2^{2^n} (D) 2^{n^2}

Q. 46 How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

(A) 7 (B) 8

(C) 9 (D) 10

Q. 47 Consider the following Boolean function of four variables

$f(w,x,,y,z) = \sum(1,3,4,6,9,11,12,14)$

The function is

(A) independent of one variable (B) independent of two variables

(C) independent of three variables (D) dependent on all the variables

YEAR 2007 TWO MARKS

Q. 48 Let $f(w,x,y,z) = \sum(0,4,5,7,8,9,13,15)$. Which of the following expressions are NOT equivalent to f?

(A) $x'y'z + w'xy' + wy'z + xz$ (B) $w'y'x' + wx'y' + xz$

(C) $w'y'z' + wx'y' + xyz + xy'z$ (D) $x'y'z + wx'y' + w'y$

Q. 49 Define the connective* for the boolean variable X and Y as: $X * Y = XY + X'Y'$

Let $Z = X * Z$

Consider the following expression P, Q and R.

$P: X = Y * ZQ: Y = X * Z$

$R: X * Y * Z = 1$

Which of the following is TRUE?

(A) only P and Q are valid (B) Only Q and R are valid

(C) Only P and R are valid (D) All P, Q, R are valid

Q. 50 Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

(A) 2^n line to 1 line (B) 2^{n+1} line to 1 line

(C) 2^{n-1} line to 1 line (D) 2^{n-2} line to 1 line

Q. 51 In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs, A_i and B_i are given by $P_i = A_i \oplus B_i$ and $G_i = A_i B_i$ The expressions for the sum bit S and carry bit C_{i+1} of the look ahead carry adder are given by

$S_i + P_i \oplus C_i$ and $C_{i+1} G_i + P_i C_i$, Where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator.. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively

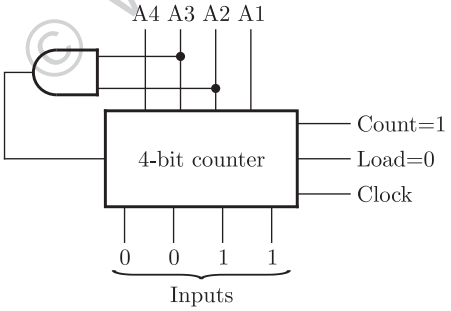
(A) 6,3 (B) 10,4

(C) 6,4 (D) 10,5

Q. 52 The control signal functions of 4-bit binary counter are given below (where X is "don't care")

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

The counter is connected as follows



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence

(A) 0,3,4 (B) 0,3,4,5

(C) 0,1,2,3,4 (D) 0,1,2,3,4,5

YEAR 2008 ONE MARK

Q. 53 In the IEEE floating point representation the hexadecimal value 0x00000000 corresponds to

(A) the normalized value 2^{-127} (B) the normalized value 2^{-126}

(C) the normalized value $+0$ (D) the special value $+0$

Q. 54 In the karnaugh map shown below, X denoted a don't care term. What is the nominal form of the function represented by the karnaugh map

cd \ ab	00	01	11	10
00	I	I		I
01	×			
11	×			
10	I	I		×

(A) $\bar{b}.\bar{d} + \bar{a}.\bar{d}$ (B) $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.\bar{b}.\bar{d}$

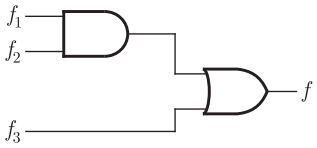
(C) $\bar{b}.\bar{d} + \bar{a}.\bar{b}.\bar{d}$ (D) $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.\bar{d}$

Q. 55 Let a denote number system radix. The only value(s) of r that satisfy the equation $\sqrt{121} + 11$, is/are

(A) decimal 10 (B) decimal 11

(C) decimal 10 and 11 (D) any value> 2

Q. 56 Give f_1, f_3 and f in canonical sum of products form (in decimal) for the circuit



$$f_1 = \sum m(4,5,6,7,8)$$
$$f_3 = \sum m(1,6,15)$$
$$f = \sum m(1,6,8,15)$$

Then f_2 is

(A) $\sum m(4,6)$ (B) $\sum m(4,8)$

(C) $\sum m(6,8)$ (D) $\sum m(4,6,8)$

YEAR 2008 TWO MARKS

Q. 57 If P, Q, R are Boolean variables, $(P + \bar{Q})\ (P.\bar{Q} + P.R)\ (\bar{P}.\bar{R} + \bar{Q})$simplifies to

(A) $P.\bar{Q}$ (B) $P.\bar{R}$

(C) $P.\bar{Q} + R$ (D) $P.\bar{R} + Q$

YEAR 2009 ONE MARK

Q. 58 $(1217)_8$ is equivalent to

(A) $(1217)_{16}$ (B) $(028F)_{16}$

(C) $(2297)_{10}$ (D) $(0B17)_{16}$

Q. 59 What is the minimum number of gates required to implement the Boolean function $(AB + C)$ if we have to use only 2-input NOR gates ?

(A) 2 (B) 3

(C) 4 (D) 5

YEAR 2010 ONE MARK

Q. 60 The minterm expansion of $f(P,Q,R) = PQ + Q\overline{R} + P\overline{R}$ is

(A) $m_2 + m_4 + m_6 + m_1$ (B) $m_0 + m_1 + m_3 + m_5$

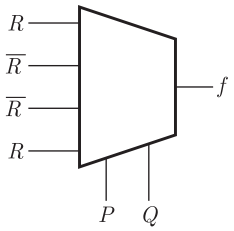
(C) $m_0 + m_1 + m_6 + m_1$ (D) $m_2 + m_3 + m_4 + m_5$

Q. 61 P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. The 2's complement representation of 8^*P is

(A) $(C3D8)_{16}$ (B) $(187B)_{16}$

(C) $(F878)_{16}$ (D) $(987B)_{16}$

Q. 62 The Boolean expression for the output f of the multiplexer shown below is

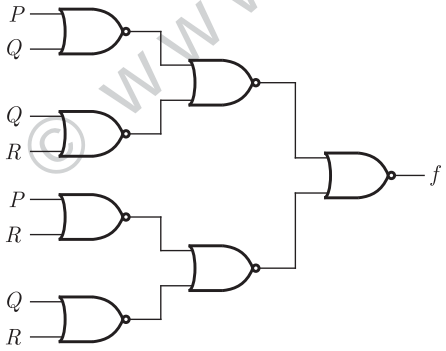


(A) $\overline{P \oplus Q \oplus R}$ (B) $P \oplus Q \oplus R$

(C) $P + Q + R$ (D) $\overline{P + Q + R}$

YEAR 2010 TWO MARKS

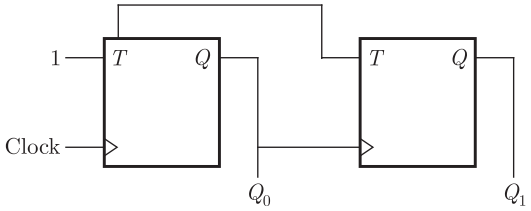
Q. 63 What is the boolean expression for the output f of the combinational logic circuit of NOR gates given below ?



(A) $\overline{Q + R}$ (B) $\overline{P + Q}$

(C) $\overline{P + R}$ (D) $\overline{P + Q + R}$

Q. 64 In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00, what are the next four values of Q_1Q_0 ?

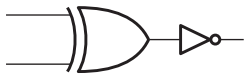


(A) 11, 10, 01, 00 (B) 10, 11, 01, 00

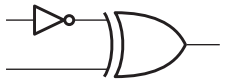
(C) 10, 00, 01, 11 (D) 11, 10, 00, 01

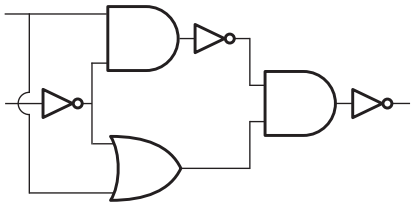
YEAR 2011 ONE MARK

Q. 65 Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate?

(A) 

(B) 

(C) 

(D) 

Q. 66 The minimum number of D flip-flops needed to design a mod-258 counter is

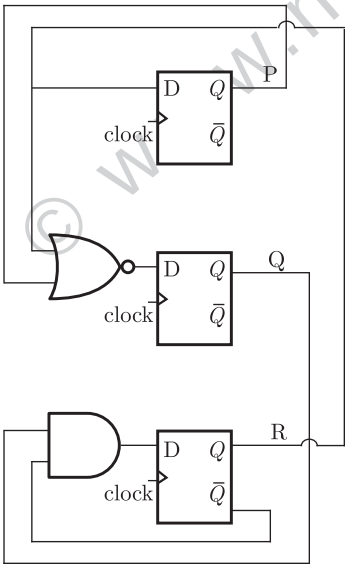
(A) 9 (B) 8

(C) 512 (D) 258

YEAR 2011 TWO MARKS

Common Data For Q. 67 and 68 :

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration



Q. 67 If a some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

(A) 000 (B) 001

(C) 010 (D) 011

Q. 68 If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

(A) 3 (B) 4

(C) 5 (D) 6

YEAR 2012 ONE MARK

Q. 69 The truth table

X	Y	$f(X, Y)$
0	0	0
0	1	0
1	0	1
1	1	1

represents the Boolean function

(A) X (B) $X + Y$

(C) $X \oplus Y$ (D) Y

YEAR 2012 TWO MARKS

Q. 70 What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term.

ab / cd	00	01	11	10
00	**1**	**X**	**X**	**1**
01	**X**			**1**
11				
10	**1**			**X**

(A) $\overline{bd}$ (B) $\overline{bd} + \overline{b}\overline{c}$

(C) $\overline{bd} + a\overline{b}\overline{c}d$ (D) $\overline{bd} + \overline{b}\overline{c} + \overline{c}\overline{d}$

****

ANSWER KEY

Digital Logic									
1	2	3	4	5	6	7	8	9	10
(A)	(A)	(C)	(C)	(B)	(B)	(B)	(D)	(A)	(B)
11	12	13	14	15	16	17	18	19	20
(A)	(A)	(C)	(C)	(A)	(A)	(C)	(C)	(C)	(C)
21	22	23	24	25	26	27	28	29	30
(D)	(D)	(D)	(A)	(B)	(A)	(D)	(B)	(A)	(D)
31	32	33	34	35	36	37	38	39	40
(A)	(A)	(A)	(A)	(B)	(D)	(D)	(D)	(B)	(A)
41	42	43	44	45	46	47	48	49	50
(D)	(A)	(C)	(C)	(C)	(B)	(B)	(D)	(D)	(C)
51	52	53	54	55	56	57	58	59	60
(B)	(C)	(D)	(A)	(D)	(C)	(A)	(B)	(B)	(A)
61	62	63	64	65	66	67	68	69	70
(A)	(B)	(A)	(A)	(D)	(A)	(D)	(B)	(A)	(B)