Practical-6

Design and verify the operation of flip-flops using logic gates.

Aim : To design and construct the operation of flip-flops circuits and verify the truth table using logic gates.

Theory :

S-R Flip Flop

- It us basically S-R latch using NAND gates with an additional enable input.
- It is also called as level triggered SR-FF. For this circuit in output will take place if and only if the enable input (E) is made active.
- In short this circuit will operate as an S-R latch, if E=1 but there is no change in the output if E=0.

JK Flip Flop

- Master slave JK FF is a cascade of two S-R FF with feedback from the output of second to input of first Master is positive level triggered.

But due to the presence of the inverter in the clock line, the slave will respond to the negative level. Hence when the clock = 1 (positive level) the master is active and slave is inactive.

- Whereas when clock=0 (low level) the slave is active and master is inactive.

Delay Flip Flop / D Flip Flop

- Delay Flip Flop or D flip flop is the simple gated S-R latch with a NAND inverter connected between S and R inputs.
- It has only one input. The input data is appearing at output after same time. Due to this data delay between i/p and o/p, it is called delay flip flop.
- S and R will be the complements of each other due to NAND inverter. Hence S=R=0 or S=R=1, these input condition will never appear.
- This problem is avoided by SR = 00 and SR=11 conditions.

Toggle Flip Flop / T Flip Flop :

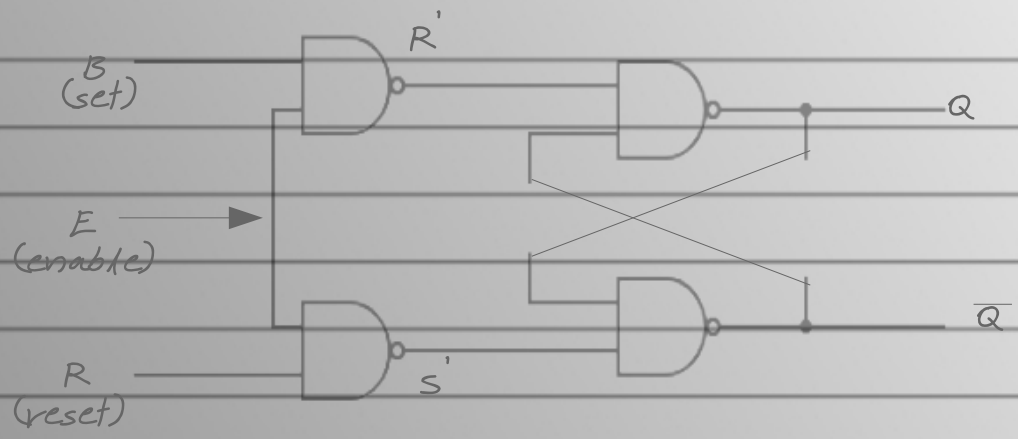
- Toggle flip flop is basically a JK flip flop with J and K terminals permanently connected

together.

- It has only input denoted by T as shown in the diagram T flipflop show in diagram.

Logic Diagram :

S-R Flip Flop

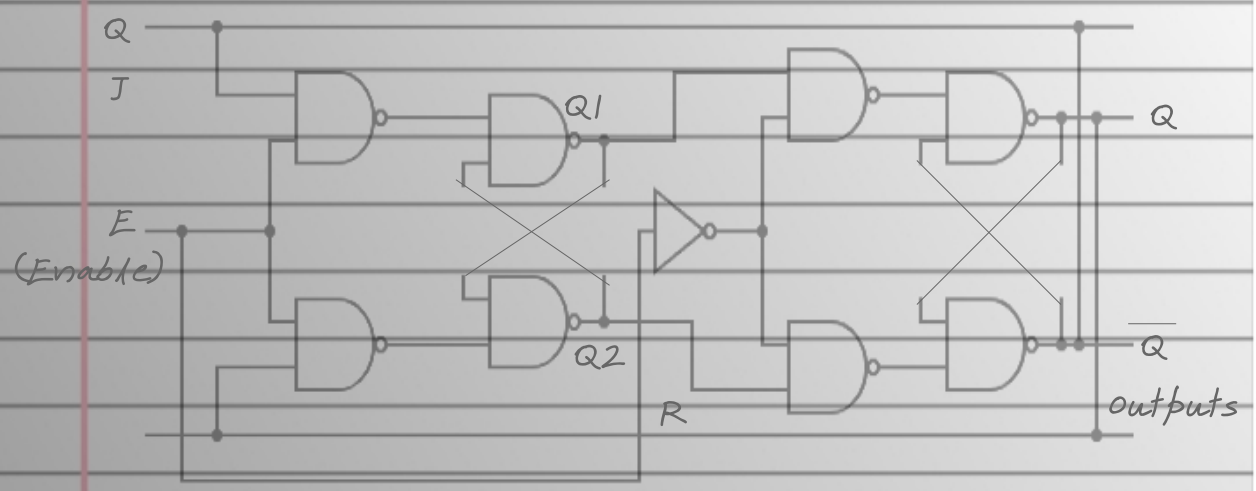


Truth Table :

F	S	R	Q	Q
1	0	0	Q	Q
1	0	1	0	1
1	1	0	1	0
1	1	1	x	x

JK Flip Flop

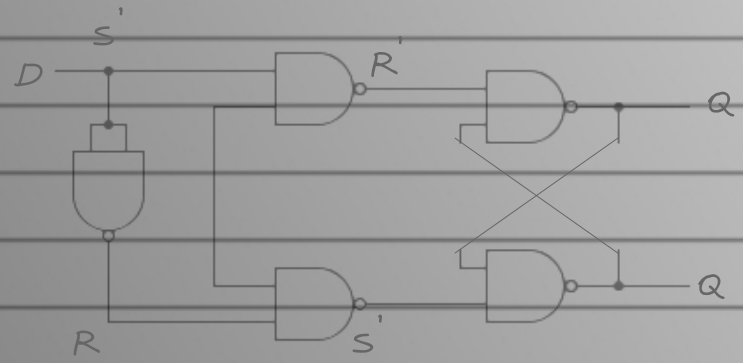
:



Truth Table :

E	J	K	Q	$\overline{Q}$
1	0	0	Q	$\overline{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\overline{Q}$	Q

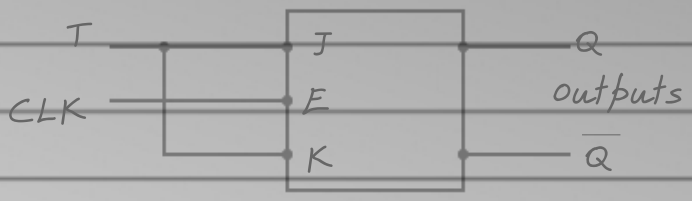
Delay Flip Flop



Truth Table :

E	D	Q	$\overline{Q}$
1	0	0	1
0	1	1	0

Toggle Flip Flop



Truth Table :

E	T	Q	$\overline{Q}$
1	0	Q	$\overline{Q}$
1	1	$\overline{Q}$	Q