Digital Logic and Circuits

Midterm Assignment-1

Submission Instructions:

*1.Submit the assignment on or before **13th August 2020***
2. Before submitting please make sure the file is in Pdf format.
3. Submit through Microsoft teams assignment section

1. Construct the XOR and XNOR gates by using basic gates.

2. If F(x, y, z) = Σ(1, 3, 6, 7) then show that F(x, y, z)= Π(0, 2, 4, 5)
3. Minimize the following Boolean expression using k-map.
   a. $\overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D} + AB\overline{C}\overline{D} + \overline{A}\overline{B}CD + A\overline{B}CD + \overline{A}\overline{B}C\overline{D} + \overline{A}BC\overline{D} + ABC\overline{D} + A\overline{B}C\overline{D}$

4. Design a 4-bit parallel adder using single bit full adder.

5. A bank has 3 locks with a key for each lock. Each key is owned by a different person. In order to open the vault door at least two people must insert their keys into the assigned locks at the same time. The trainee (i.e. person 3) can only open the vault when the manager (i.e. person 1) is present in the opening. The signal lines (A,B,C) are 1 if the key is inserted into locks 1,2,3 respectively.

   a. Determine the truth table for such a digital locking system
   b. Implement the circuit using RTL logic family
   c. Implement the circuit using CMOS technology.