به نام خدا

مشکلات پروژه :

- پیدا کردن جای مناسب برای ریختن خروجی های M , T , L (زمان درست آن جایی است که clk از صفر به یک تغییر کرده، در بقیه ی مکان ها نباید مقادیر این سیگنال ها را تغییر داد).
- پایان یافتن entity, component, architecture,... باید به چه صورت باشد (هر کدام با اسم استفاده شده تمام خواهند شد. end testsystem).
- ارور state وقتی در لیست حساسیت قرار میگرفت (داده از نوع out نمی‌تواند در لیست حساسیت قرار گیرد).
- بستن پورت entity با);
- مقادیر H و – (باید مقادیر در 7سگمنت در نظر گرفته میشد، نه مقادیر باینری ان ها).

شبیه سازی :

گزارش :

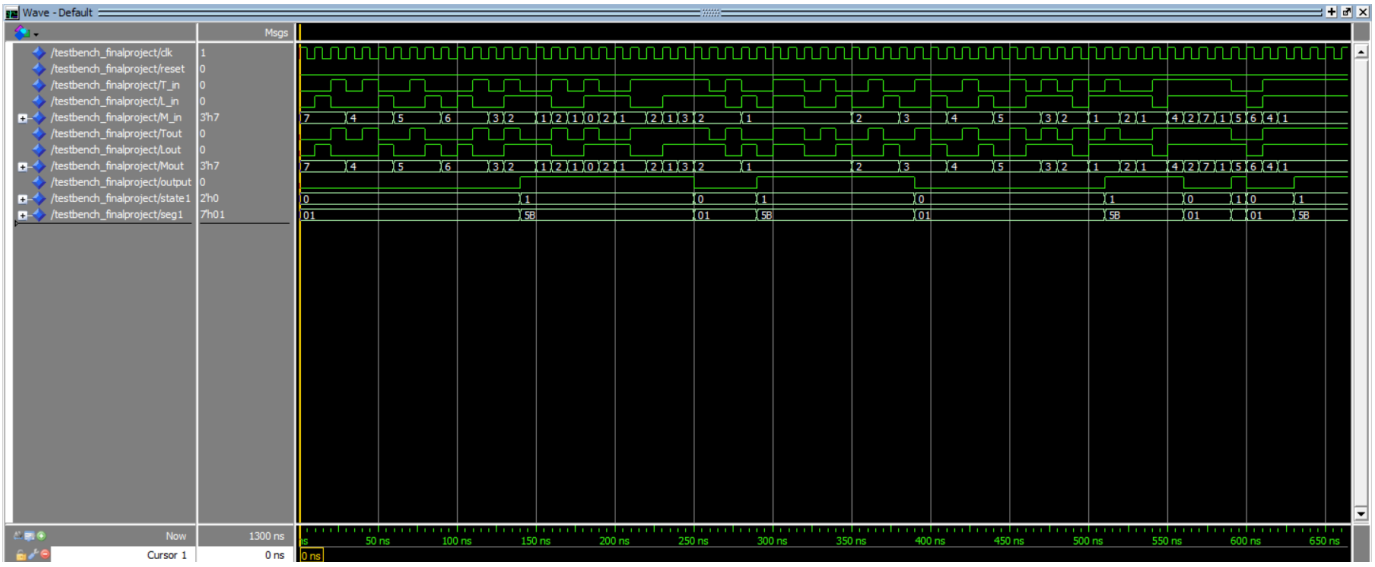
1. Reset → State = st2, st2 → st0
2. T=0, L=0, M>"011" m=7 st0 → st0
3. T= 0, L= 1, M>"011" 7 st0 → st0
4. T= 1, L= 0, M>"011" 7 st0 → st0
5. T=0, L=0, M>"011" m=4 st0 → st0
6. T= 0, L= 1, M>"011" 4 st0 → st0
7. T= 1, L= 0, M>"011” 4 st0 → st0
8. T=0, L=0, M>"011" m=5 st0 → st0
9. T=0, L=1, M>"011” 5 st0 → st0
10. T=1, L=0, M>"011” 5 st0 → st0

11. T=0, L=0, M>"011" m=6 st0 → st0
12. T=0, L=1, M>"011" 6 st0 → st0
13. T=1, L=0, M>"011" 6 st0 → st0
14. T=0 L=0 M<="011”6 st0 → st1
15. T=1 L=1 M<"011" 2 st1 →st1
16. T=1 L=1 M<"011" 1 st1→st1
17. T=1 L=1 M<"011" 2 st1→st1
18. T=1 L=1 M<"011" 1 st1→st1
19. T=1 L=1 M<"011" m=0 st1→st1
20. T=1 L=0 M<"011" m=2 st1->st1
21. T=0 L=1 M<"011" m=1 st1->st1
22. T=1 L=0 M<"011" m=1 st1->st1
23. T=0 L=1 M<"011" m=2 st1->st1
24. T=1 L=0 M<"011” m=1 st1->st1
25. T=1 L=1 M>="011” st1->st0
26. T=1 L=1 M>"001" 2 st0->st0
27. T=0 L=1 M>"001" 2 st0->st0
28. T=1 L=0 M>"001" 2 st0->st0
29. T=1 L=0 M>"011" 1 st0->st0
30. T=0 L=1 M>"011” 1 st0->st0
31. T=0 L=0 M<="111” 1 st0->st1
32. T=1 L=1 M<"011" m=1 st1->st1
33. T=1 L=1 M>="011" 3 st1->st0

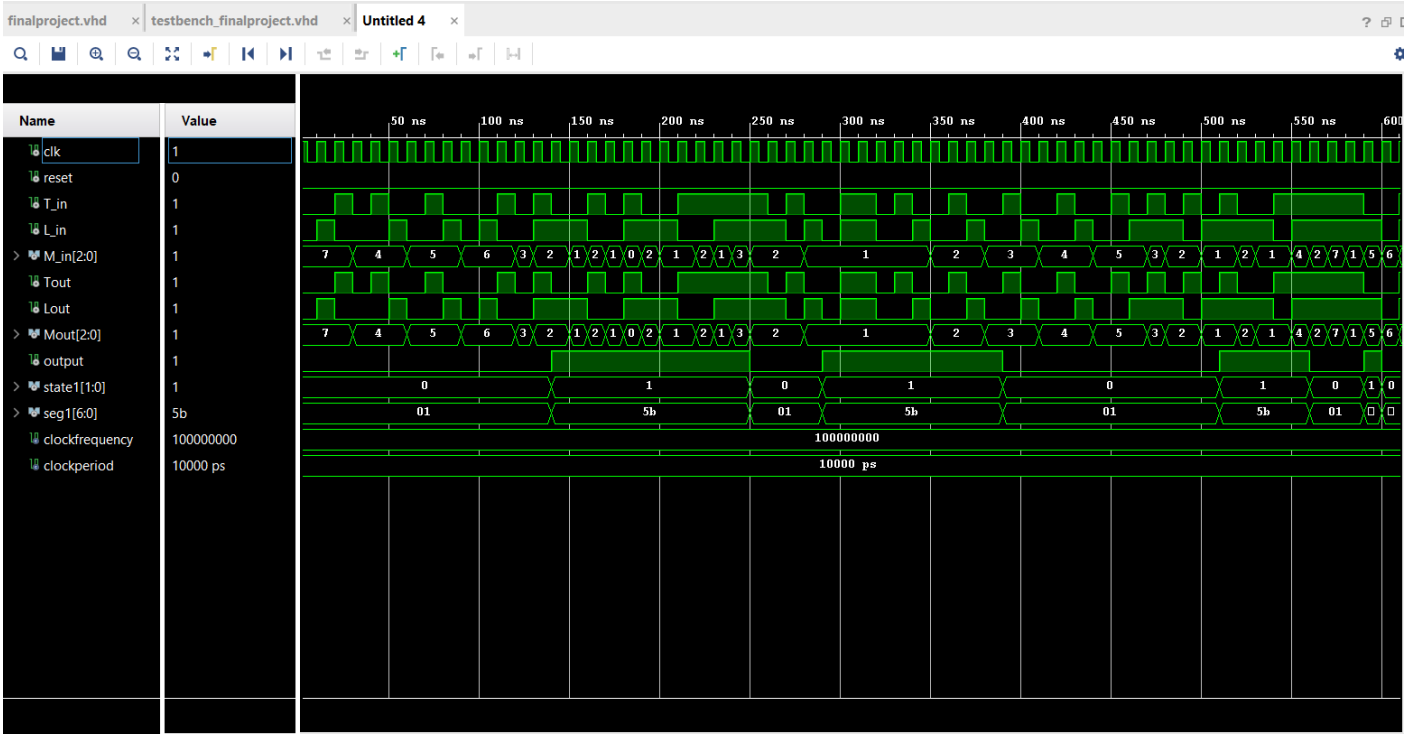
.....و

تصاویر :

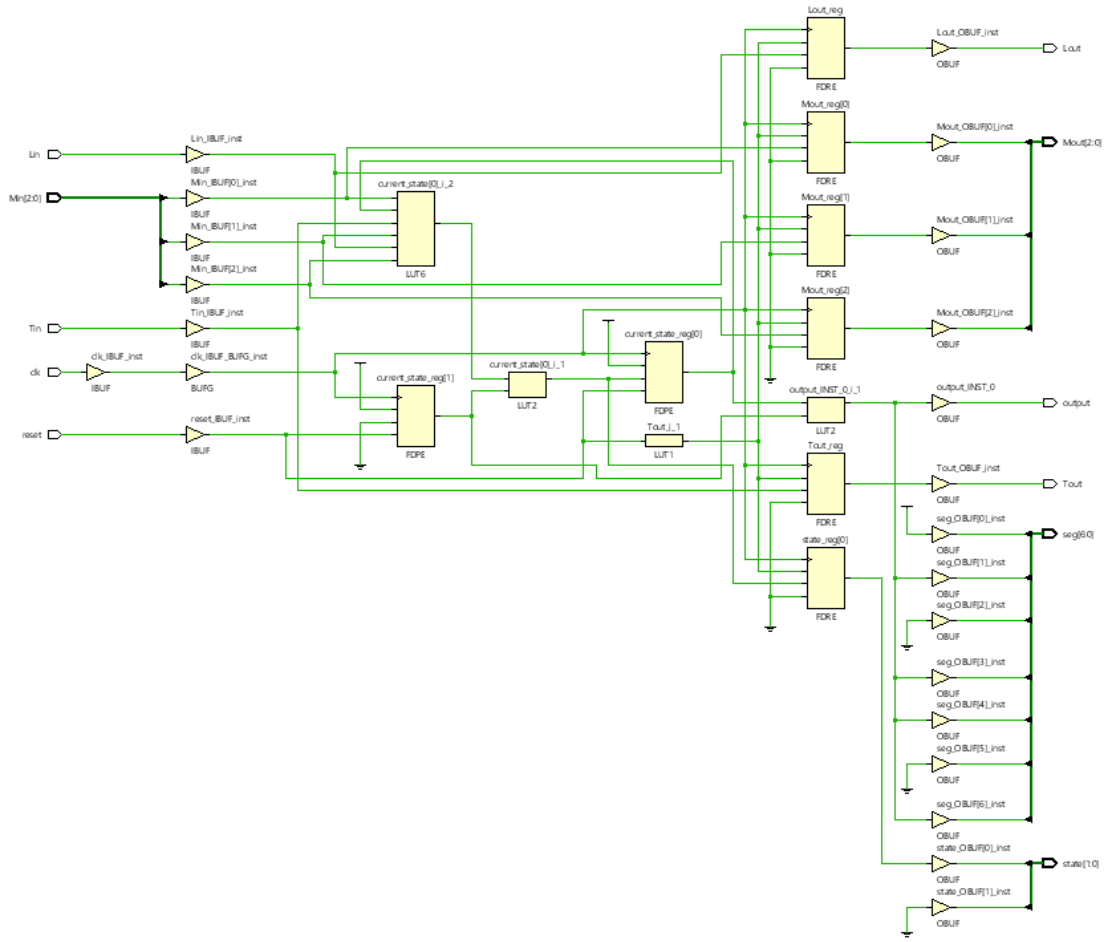
Modelsim:



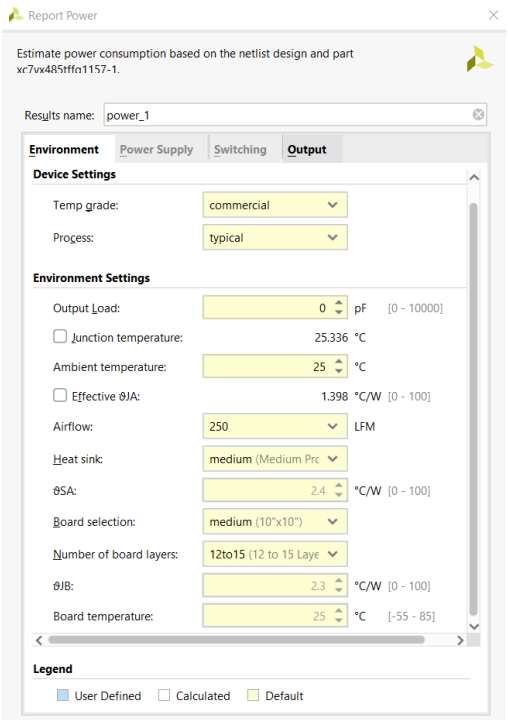
Vivado:



گزارش های خروجی سنتز:

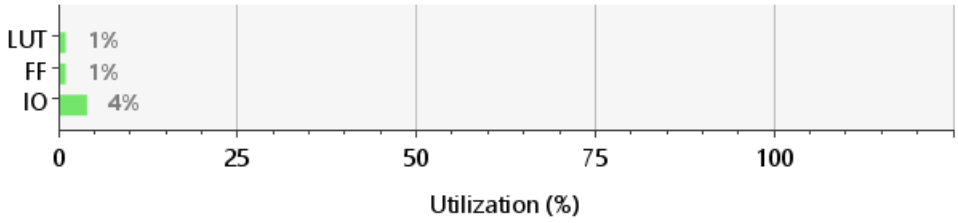


Power:



Summary

Resource	Utilization	Available	Utilization %
LUT	3	303600	0.00
FF	8	607200	0.00
IO	22	600	3.67

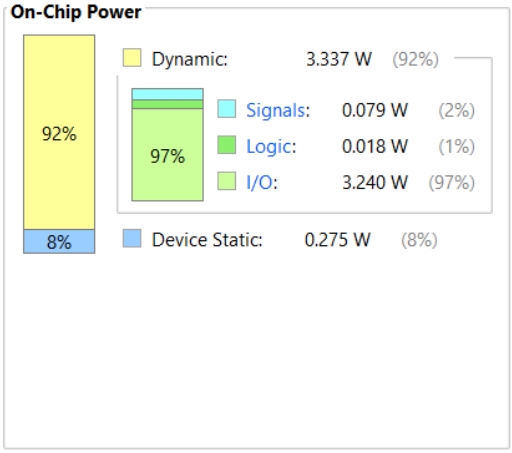


Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**3.612 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.0°C**
Thermal Margin:	55.0°C (37.8 W)
Effective ϑJA:	1.4°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Synthes Report:

```
| Tool Version : Vivado v.2019.1 (win64) Build 2552052 Fri May 24 14:49:42 MDT 2019
| Date         : Tue Jul  4 21:18:20 2023
| Host         : LAPTOP-BBTG4CFN running 64-bit major release  (build 9200)
| Command      : report_utilization -file wateringsystem_utilization_placed.rpt -pb wateringsystem_utilization_placed.pb
| Design       : wateringsystem
| Device       : 7vx485tffg1157-1
| Design State : Fully Placed
------------------------------------------------------------------------------------------------------------------------

Utilization Design Information

Table of Contents
-----------------
1. Slice Logic
1.1 Summary of Registers by Type
2. Slice Logic Distribution
3. Memory
4. DSP
5. IO and GT Specific
6. Clocking
7. Specific Feature
8. Primitives
9. Black Boxes
10. Instantiated Netlists

1. Slice Logic
--------------

+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
```

Site Type	Used	Fixed	Available	Util%
Slice LUTs	3	0	303600	<0.01
LUT as Logic	3	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	8	0	607200	<0.01
Register as Flip Flop	8	0	607200	<0.01
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

1.1 Summary of Registers by Type

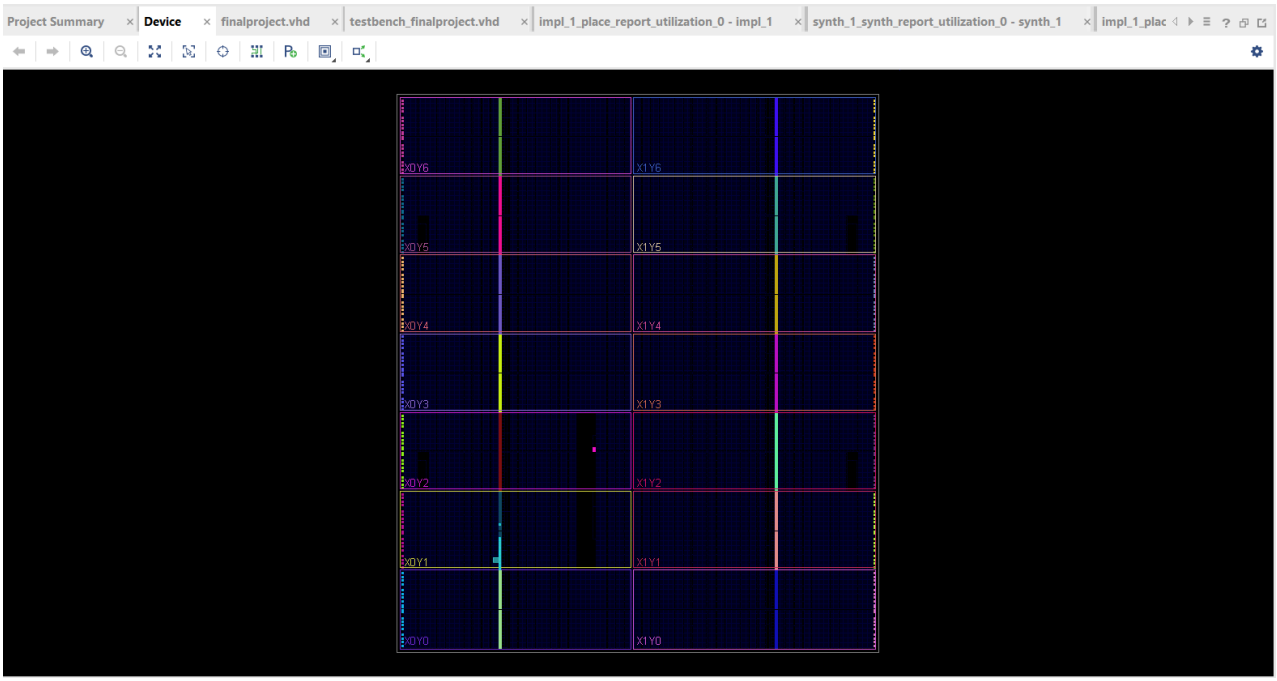
Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
2	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
6	Yes	Reset	-

Site Type	Used	Fixed	Available	Util%
Slice	2	0	75900	<0.01
SLICEL	1	0		
SLICEM	1	0		
LUT as Logic	3	0	303600	<0.01
using O5 output only	0			
using O6 output only	2			
using O5 and O6	1			
LUT as Memory	0	0	130800	0.00
LUT as Distributed RAM	0	0		
LUT as Shift Register	0	0		
Slice Registers	8	0	607200	<0.01
Register driven from within the Slice	1			
Register driven from outside the Slice	7			
LUT in front of the register is unused	4			
LUT in front of the register is used	3			
Unique Control Sets	2		75900	<0.01

* Note: Available Control Sets calculated as Slice Registers / 8, Review the Control Sets Report for more information regarding control sets.

3. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	1030	0.00
RAMB36/FIFO*	0	0	1030	0.00
RAMB18	0	0	2060	0.00



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	NA	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	NA	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA	Total Number of Endpoints:	NA	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Check Timing

Timing Check	Count
constant_clock	0
generated_clocks	0
latch_loops	0
loops	0
multiple_clock	0
no_clock	8
no_input_delay	6
no_output_delay	11
partial_input_delay	0
partial_output_delay	0
pulse_width_clock	0
unconstrained_internal_endpoints	15

نازنین اعتمادی نسب . 99213037