#### CSE 3203 CT 4 Assignment Roll No: 1803034

#### **Assignment Problem:**

**Build CPU based on following requirements:** 

- 1. Word Size of CPU = 4 bit
- 2. ALU Operations = Add, ROL, Xor
- 3. Register Number = 4
- 4. Size of RAM = 7
- 5. Word size of ISA and RAM = 15 bit
- 6. CPU Instructions = Register Mode, Immidiate Mode, Jmp, JC

#### Solution:

### **Simulator Design:**

1. ALU Circuit (Top to Bottom all circuits):

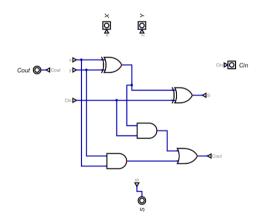


Fig: 1 bit Full Adder

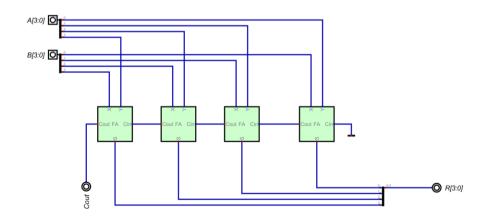


Fig: 4 bit Adder

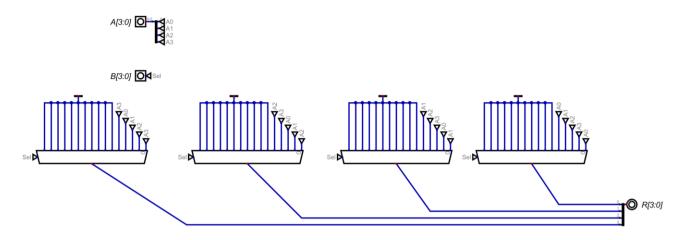
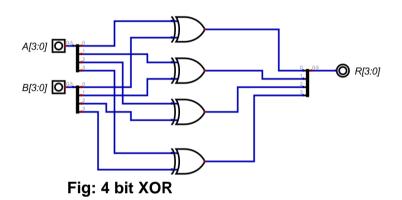


Fig: 4 bit Left Rotator



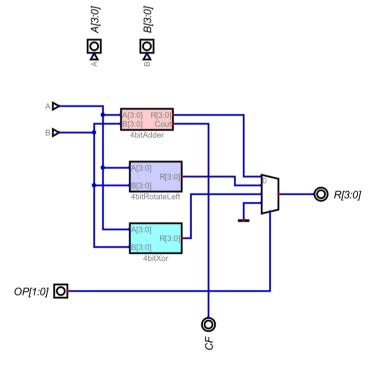


Fig: 4 bit ALU

# 2. Register Set Circuit (Top to Bottom all circuits):

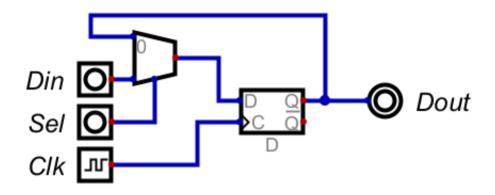


Fig: 1 bit Register

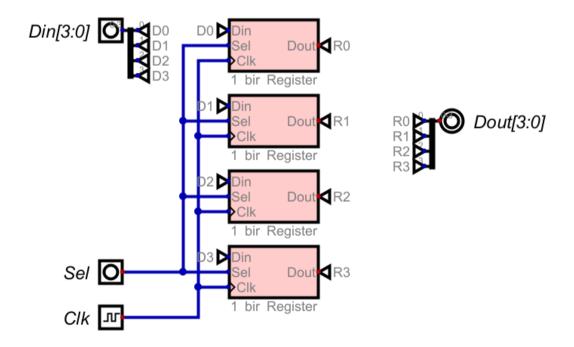


Fig: 1 x 4 Register

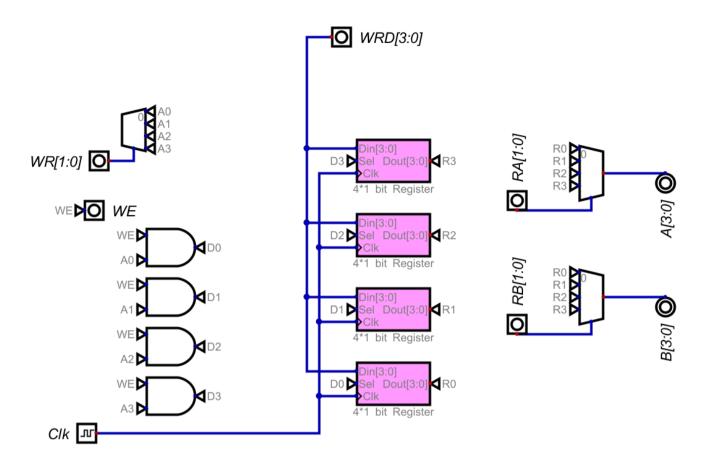


Fig: 4x4 Register Set

## 3. RAM Circuit (Top to Bottom all circuits):

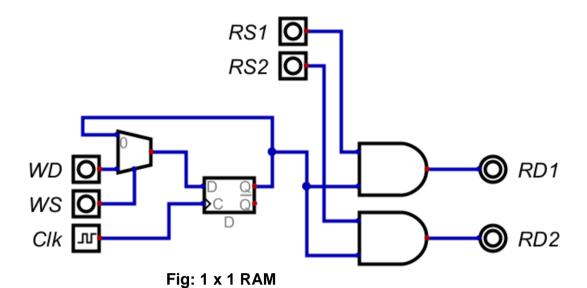


Fig: 1 x 15 RAM

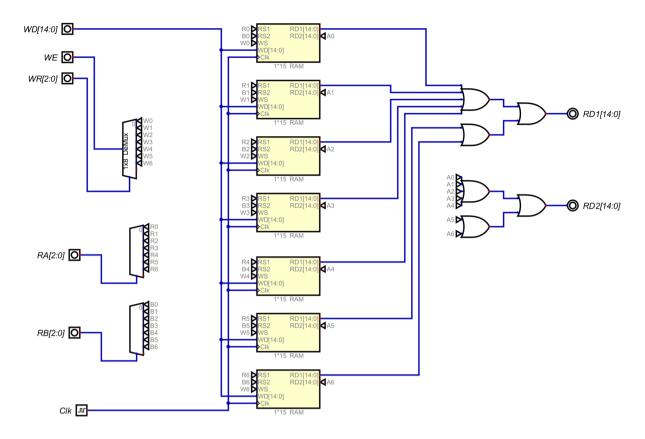


Fig: 7 x 15 RAM

# 4. ISA

1 <sup>st</sup> bit	2 <sup>nd</sup> bit	3 <sup>rd</sup> bit	4 <sup>th</sup> bit	5 <sup>th</sup> bit	6 <sup>th</sup> bit	7 <sup>th</sup> bit	8 <sup>th</sup> bit	9 <sup>th</sup> bit	10 <sup>th</sup> bit	11 <sup>th</sup> bit	12 <sup>t</sup> h bit	13 <sup>th</sup> bit	14 <sup>th</sup> bit	15 <sup>th</sup> bit
0 0 (Regular Mode)		0 0 ADD		X X Address of Register (RA)		X X Address of Register (RB)		x	X X X X X X X Don't Care (7 bit)				x	
<b>0</b> (Immidia	<b>1</b> ite Mode)	0 R	0 DD 1 OL 0	X Addr of Regi		x	X Consta (4 bi		x	Х		X t Care bit)	х	x
<b>1</b> (Jmp	<b>0</b> Mode)	<b>0</b>	<b>0</b>	Instra Poin	X ess of action ter A)	X	x	х	<b>X</b> Dor (8 I	i't Care	х	х	х	x

# 5. CPU (Top to Bottom all circuits):

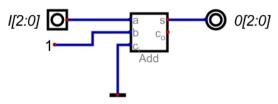


Fig: 3 bit PC Adder

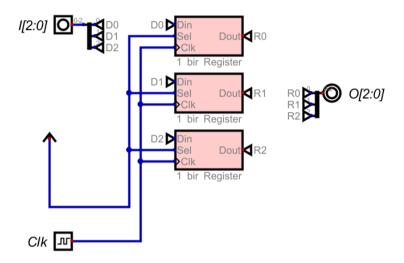


Fig: 3 bit Program Counter Register

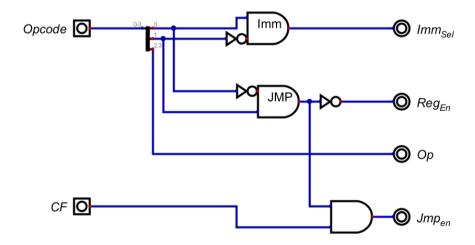


Fig: Control Unit

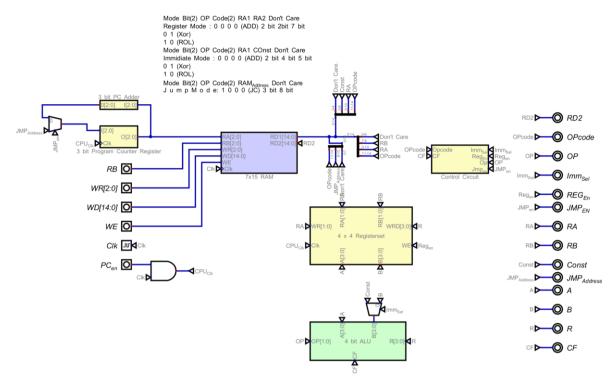


Fig: 4 bit CPU