CSE332 Lab 8

Name: Nazmul Hasan
ID: 1911742042
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Section: 3
Experiment Name: Design of a single cycle Datapath.

Discussion: In this lab our goal was to design a single cycle datapath. The datapath is an important part of a processor. It implements the fetch, decode, and execute cycle. In a datapath components include memory that stores the current instruction, program counter that stores the address of current instruction, and ALU that executes current instruction.

In pervious labs we have implemented 16 bit ALU unit and 16 bit register file. Our ALU can perform AND, OR, ADD, SUB operations. We have used overflow and zero to catch flags. We used 16 one bit ALU to form a 16 bit ALU.

To design a datapath, we need ROM as instruction memory and a RAM as accessed primary memory. ROM is a read only memory, where both read and write can be done in RAM. In Fetch unit, ROM (used to pass instruction) is connected to a PC (program counter). A PC identifies next instruction and passes it. Each time pc is incremented by 1. From ROM, we will get 16 bit output. We have used a splitter to separate RS, RT, RD and Opcode. Now it moves into the decode part. RS and RT lines are directly connected to the RS and RT inputs of our designed register file. Our designed datapath will perform both R and I type instruction. So, based on the R and I type instruction, RD and RT are connected to the RD of register file with the help of a 2x1 mux. This is how an instruction is fetched and decoded.

In execute part; we used our designed 16 bit ALU to execute operations. From our register file we get two outputs Read1 and Read2. Read1 line is directly connected to input A of ALU. Input B of ALU is depends on instruction type. If it's R type, then Read2 is connected to input B. But if it is I type instruction, then the value of RD register is converted to 16 bit and connected to the input B of ALU. We have used another 2x1 mux to select one of these two. Opcode is also given connection to ALU to select operations.

Result of ALU unit is connected to RAM to store the operation result. RAM also has some input signals like ld for load (read data form memory), str (store data into memory), and RAM enable. So, we can do both read and write here. In write back, we may need to pass the address or the ALU result to write into register based on I type and R type instruction with the help of a 2x1 multiplexer.

In this lab, we have learnt how we can use our previous designed register files and ALU unit to build a register datapath successfully. Also we have learnt how RAM and ROM works and how they can be used to design register datapath.