Lab Manual
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Experiment No: 3
Experiment Name: Design of a 4 bit Universal Shift Register

Introduction:

In this experiment you will construct a 4-bit universal shift register which will be capable of transferring data in both left and right direction. When a register is able to transfer data both in the shift-right and shift-left, along with the necessary input and output terminals for parallel transfer, then it is called a shift register with parallel load or 'universal shift register'.

Features of a universal shift register:

1. Clock input to all registers.
2. Clear control to clear the register to 0.
3. Shift right control.
4. Shift left control.
5. Parallel load control for parallel transfer.
6. N parallel output lines (4 output lines for 4 bits)
7. No change control even in presence of a clock.

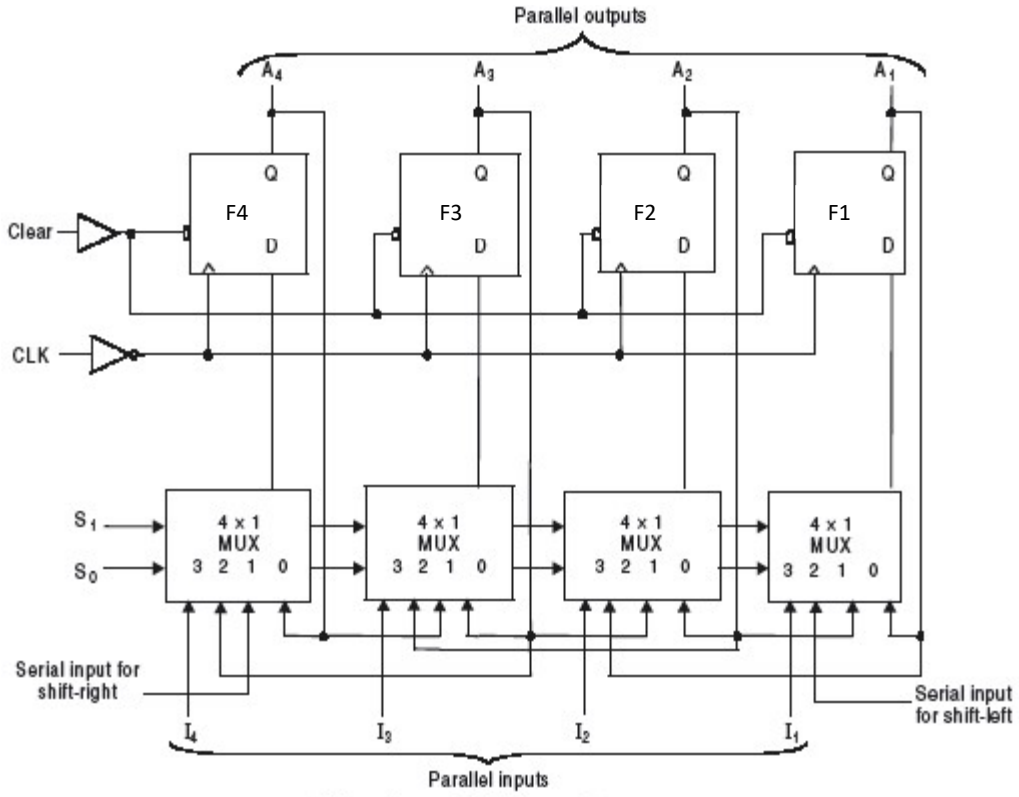
Mode Control:

S1	S0	Register Operation
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

Equipments:

- Four D Flip Flops (Two 7474 ICs)
- Four 4X1 MUX (Two 74153 ICs)
- Trainer Board
- Wires
- Power Supply

Circuit Diagram:



4-bit universal shift register.

Operational Behaviour:

1. S1 and S0 are the common select controls to the multiplexers and parallel load inputs I1, I2, I3 and I4 is connected to each of the four multiplexers.
2. When S1 and S0 are 0 0, there is no change operation. Data of F1-F4 remain unchanged.
3. When S1 and S0 are 1 1, the inputs of I1-I4 are loaded to the outputs A1-A4.
4. When S1 and S0 are 0 1, SHR operation takes place.
    - F4 goes to F3 through MUX 3.
    - F3 goes to F2 through MUX 2.
    - F2 goes to F1 through MUX 1.
    - Serial Input for shift-right goes to F4 through MUX 4.
5. When S1 and S0 are 1 0, SHL operation takes place.
    - F1 goes to F2 through MUX 2.
    - F2 goes to F3 through MUX 3.
    - F3 goes to F4 through MUX 4.
    - Serial Input for shift-left goes to F1 through MUX 1.

Function Table:

Complete the function table according to your theoretical knowledge.

S1	S0	Operation	I4	I3	I2	I1	A4	A3	A2	A1
0	0	No Change	0	1	1	0				
0	1	SHR	1	1	0	0				
1	0	SHL	1	1	0	0				
1	1	Parallel Load	1	1	0	0				

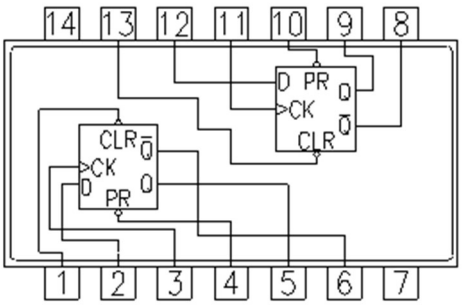
Procedure:

1) Place the ICs on the trainer board.
2) Connect V_{cc} and ground to the respective pins of IC.
3) Connect the inputs with the switches and the outputs (A1-A4) with LEDs.
4) Apply various combinations of inputs and observe the outputs.
5) Verify the experimental outputs with the Function Table.

Assignment:

1) Prepare the lab report.
2) Implement the circuit in Logisim. Take a screenshot and include it in your lab report.

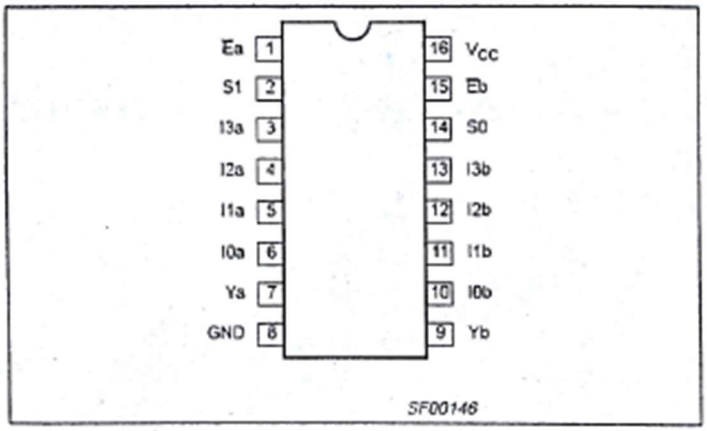
Pin configuration of ICs:



7474
Dual D Flip-Flop
with Preset and Clear

EEE336/CSE232 LAB
Dual 4x1 Multiplexer 74F153
Data Sheet

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION
I0a – I3a	Port A data inputs
I0b – I3b	Port B data inputs
S0, S1	Common Select inputs
$\overline{Ea}$	Port A Enable input (active Low)
$\overline{Eb}$	Port B Enable input (active Low)
Ya, Yb	Port A, B data outputs