CSE332 Lab 4

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Course: CSE332L
Section: 3
Experiment Name: Design of a 4 bit Universal Shift Register.

Table:

S1	S0	Operation	I4	I3	I2	I1	A4	A3	A2	A1
0	0	No Change	0	1	1	0	0	1	1	0
0	1	SHR	1	1	0	0	0	1	1	0
1	0	SHL	1	1	0	0	1	0	0	0
1	1	Parallel Load	1	1	0	0	1	1	0	0

Discussion: In our third lab class our goal was to design a 4 bit Universal Shift Register which is capable of transferring data in right and left direction. A universal shift register can transfer data both in the shift-right and shift-left with the necessary input and output terminals for parallel transfers. In the class we have seen how a register shift-right and shift-left operations are done. We can perform both shift-right and shift-left operations with the help of universal shift register.

To design a 4 bit universal shift register we need four 4x1 MUX and four D filp flops. A clock input is connected to all the registers and a clear control is used to clear the registers to 0. Selection inputs S1 and S0 are connected to all the MUX and they are used for selecting register operations. At the end we are given a task to implement the complete 4-bit universal shift register in logisim.