

Final Exam

- 1). Definition combinational Logic ?.

Ans: Combinational logic is a type of logic where the output depends only on the current inputs, not on any past inputs.

- 2) Definition sequential Logic ?.

Ans: Sequential logic is a type of logic used in electronics and computers where the output depends not only on the current inputs but also on past inputs.

3) Difference between combinational and Sequential logic?

Ans:

Combinational Logic	Sequential Logic
The output depends only on the current inputs.	The output depends on both current and past inputs.
It has no memory of past inputs.	It has memory and remembers what happened before.
Example: A calculator that gives a result based only on the numbers you enter right now.	Example: A light switch that remembers if it was on or off earlier and changes based on that memory.

*

Binary System $1+1 = 10$

Boolean Algebra $1+1 = 1$

4) Design Procedure:

- i) The problem is stated.
- ii) The number of available input variables and required output variables is determined.
- iii) The inputs and output variables are assigned letter symbols.
- iv) The truth table that defines the required relationships between inputs and outputs is derived.
- v) The simplified Boolean function for each output is obtained.
- vi) The logic diagram is drawn.

* Adders -

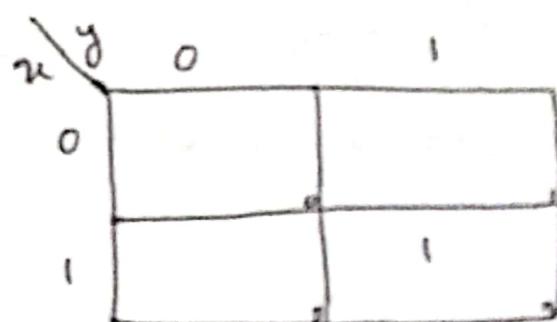
- 1) Half adder: 2 bit (sum and carry)
- 2) Full adder: 3 bit (sum and carry)

* Question: Half adder design?

Ans: This truth table is shown below:

	x	y	c_0	s
0	0	0	0	0
1	0	1	0	1
2	1	0	0	1
3	1	1	1	0

simplify -



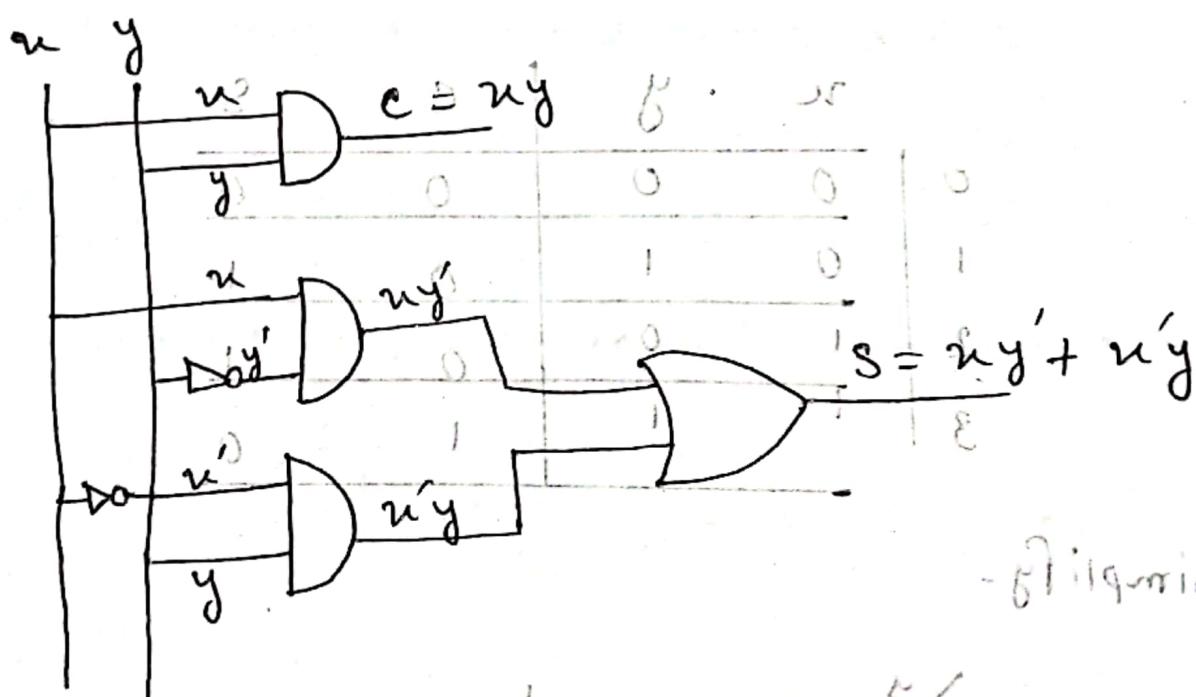
$$c = xy$$

$u \setminus y$	0	1	
(0110)	base mem) fid 2 : rabbit Flash (1)	
1	0	1	

(0110) base mem) fid 2 : rabbit Flash (1)

$$s = uy + u'y$$

Block diagram -



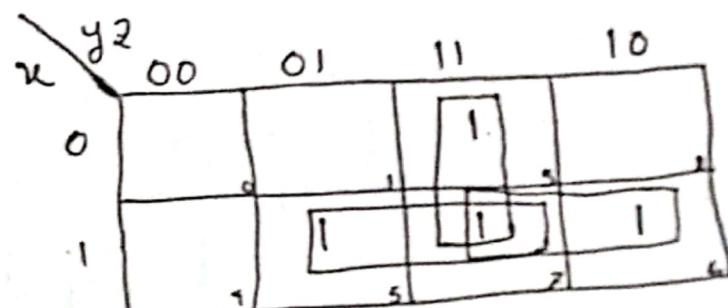
1	0	0	0
0	1	0	1
1	0	1	0
0	1	1	1

* Question: Full adder design?

Ans: This truth table is shown below:

	x	y	z	c.	s
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

Simplify -



$$C = xz + xy + yz$$

Truth table for $S = \bar{u}y'z' + \bar{u}yz + \bar{u}'y'z + \bar{u}'yz'$

u	y	z	\bar{u}	y'	z'	$\bar{u}y'z'$	$\bar{u}yz$	$\bar{u}'y'z$	$\bar{u}'yz'$	S
0	0	0	1	1	1	1	0	0	0	0
0	0	1	1	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1	0	1	1
0	1	1	1	0	0	1	1	1	1	1
1	0	0	0	1	1	0	0	0	0	0
1	0	1	0	1	0	0	0	1	0	1
1	1	0	0	0	1	0	1	0	1	1
1	1	1	0	0	0	0	1	1	1	1

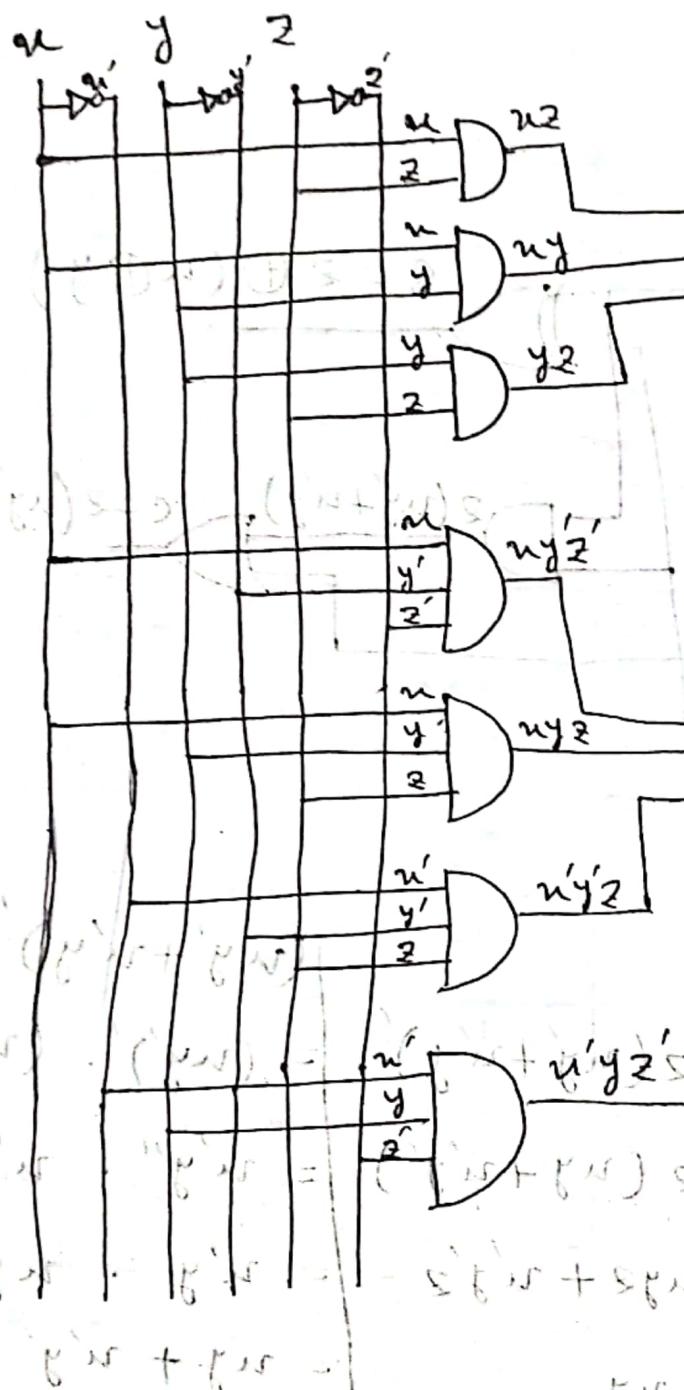
$$S = \bar{u}y'z' + \bar{u}yz + \bar{u}'y'z + \bar{u}'yz'$$

Truth table for $S = \bar{u}y'z' + \bar{u}yz + \bar{u}'y'z + \bar{u}'yz'$

u	y	z	\bar{u}	y'	z'	$\bar{u}y'z'$	$\bar{u}yz$	$\bar{u}'y'z$	$\bar{u}'yz'$	S
0	0	0	1	1	1	1	0	0	0	0
0	0	1	1	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1	0	1	1
0	1	1	1	0	0	1	1	1	1	1
1	0	0	0	1	1	0	0	0	0	0
1	0	1	0	1	0	0	0	1	0	1
1	1	0	0	0	1	0	1	0	1	1
1	1	1	0	0	0	0	1	1	1	1

$$\bar{u}y'z' + \bar{u}yz + \bar{u}'y'z + \bar{u}'yz' = 9$$

Block diagram



$$c = u_z + u_y + y_z$$

$$S = u'y_z + u'yz + u'y'z + u'y'z'$$

$$(C \oplus S) \oplus S = C$$

$$C'w + C'w' = C'w + C'w' + u'y'z' + (t_w + t_w')'s =$$

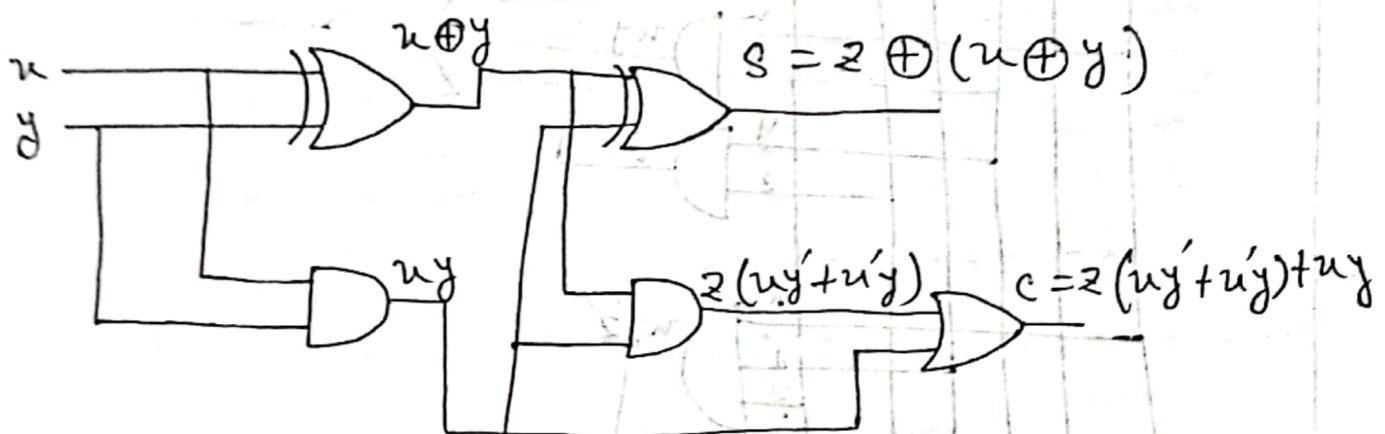
$$C'w + C'w' + u'y'z' + t_w' + t_w + s'w + s'w' + t_w' + t_w + s'w + s'w' =$$

$$t_w + t_w' + t_w + t_w + s'w + s'w' =$$

$$t_w + t_w' + s'w + s'w' =$$

* Implementation of a full adder with two half-adder and an OR gate:

Ans:



$$S = z \oplus (x \oplus y)$$

$$= z'(x'y + x'y') + z(x'y + x'y')' \quad | = (x'y)' \cdot (x'y)'$$

$$= z'(x'y + x'y') + z(x'y + x'y')' \quad | = x'y'' \cdot x''y'$$

$$= x'y'z' + x'y'z + x'yz + x'y'z \quad | = x'y \cdot x'y'$$

$$C = z(x'y + x'y') + xy$$

$$= x'y'z + x'y'z + x'yz$$

$$\begin{aligned} & (x'y + x'y')' \\ & = (x'y)' \cdot (x'y) \\ & = x'y'' \cdot x''y' \\ & = x'y \cdot x'y \\ & = xy + x'y \end{aligned}$$

* Code conversion -

Truth table for code-conversion example:

Input BCD				Output Excess-3 code				
A	B	C	D	w	u	v	y	z
0	0	0	0	0	0	0	1	1
1	0	0	1	0	1	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	0	1	1	1	0
4	0	1	0	0	1	1	1	1
5	0	1	0	1	0	1	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Raf $(A+B)8 + (C+D)8 =$

8 4 2 1	8 4 2 1
0 0 0 1	0 0 1 1
$1+3=4$	
0 1 0 0	

Simplify -

$AB \backslash CD$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	X ₁₂	X ₁₃	X ₁₅	X ₁₄
10	1 ₈	1 ₉	X ₁₁	X ₁₀

$AB \backslash CD$	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$$W = A + BD + BC$$

$$= A + BC + BD = A + B(C + D)$$

$AB \backslash CD$	00	01	11	10
00	0	1	1	1
01	1	0	5	6
11	X ₁₂	X ₁₃	X ₁₅	X ₁₄
10	1 ₈	1 ₉	X ₁₁	X ₁₀

$AB \backslash CD$	00	01	11	10
00	0	1	1	1
01	1	0	1	1
11	X	X	X	X
10	1	1	X	X

$$X = BC'D' + B'D + B'C$$

$$= B'C + B'D + BC'D'$$

$$= B'(C+D) + BC'D'$$

$$= B'(C+D) + B(C+D)$$

0010

AB	CD	00	01	11	10
00	1	0	1	1	3
01	1	1	5	1	7
11	X ₁₂	X ₁₃	X ₁₅	X ₁₄	
10	1	8	X ₁₁	X ₁₀	

AB	CD	00	01	11	10
00	1				
01	1				
11	X	X	X	X	
10	1		X	X	

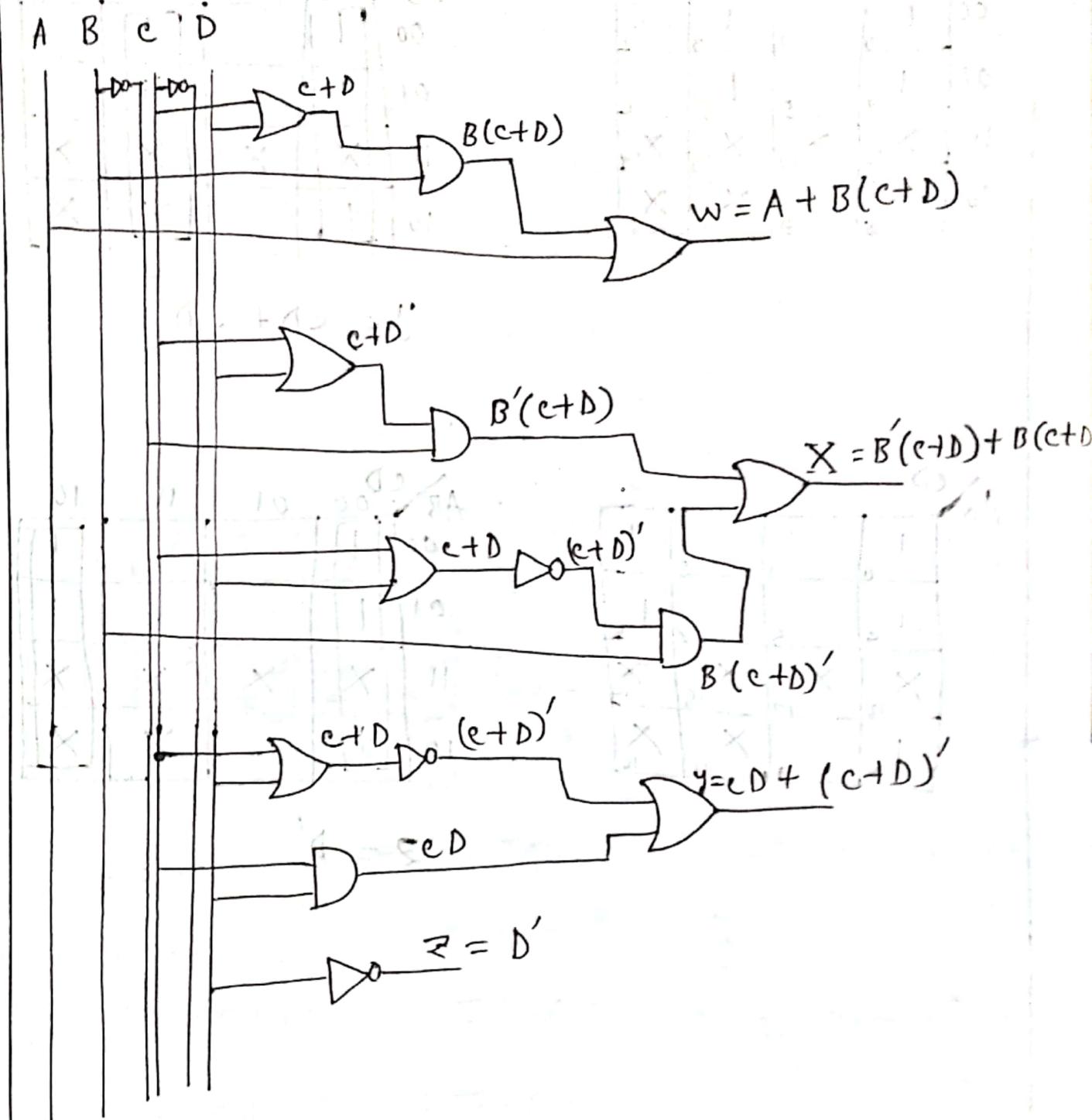
$$y = cD + c'D'$$

AB	CD	00	01	11	10
00	1	0			1
01	1	9	5	7	1
11	X ₁₂	X ₁₃	X ₁₅	X ₁₄	
10	1	8	X ₁₁	X ₁₀	

AB	CD	00	01	11	10
00	1				
01	1				
11	X	X	X	X	
10	1		*	*	X

$$z = D'$$

Block Diagram:-



Combinational Logic with MSI and LSI -

MSI = Medium Scale Integration

LSI = Large Scale Integration

Decoder -

n Input 2^n output

Truth table of a 3-to-8 line decoder -

u	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Simplify -

$$D_0 = u'y'z'$$

$$D_1 = u'yz$$

$$D_2 = u'y'z$$

$$D_3 = u'yz$$

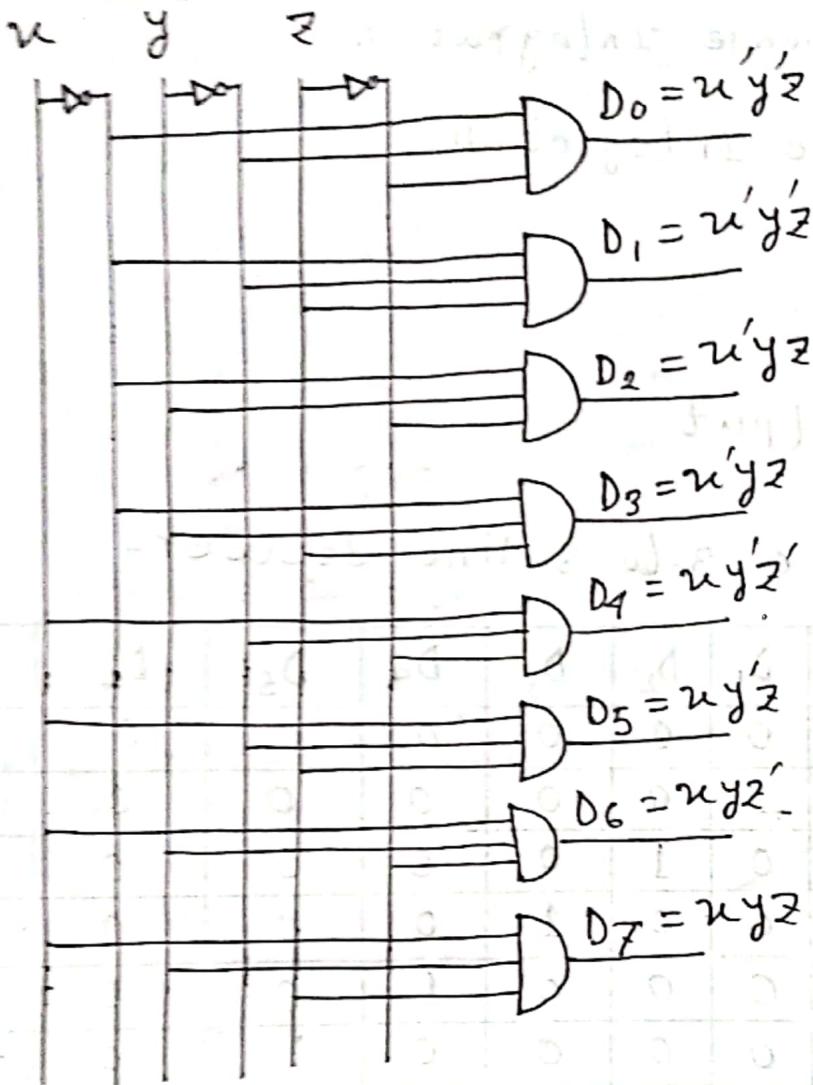
$$D_4 = uy'z'$$

$$D_5 = uy'z$$

$$D_6 = uyz$$

$$D_7 = uyz$$

Diagram-



combinational Logic Implementation -

Example-

$$S(u, y, z) = \sum(1, 2, 4, 7)$$

$$C(u, y, z) = \sum(3, 5, 6, 7)$$

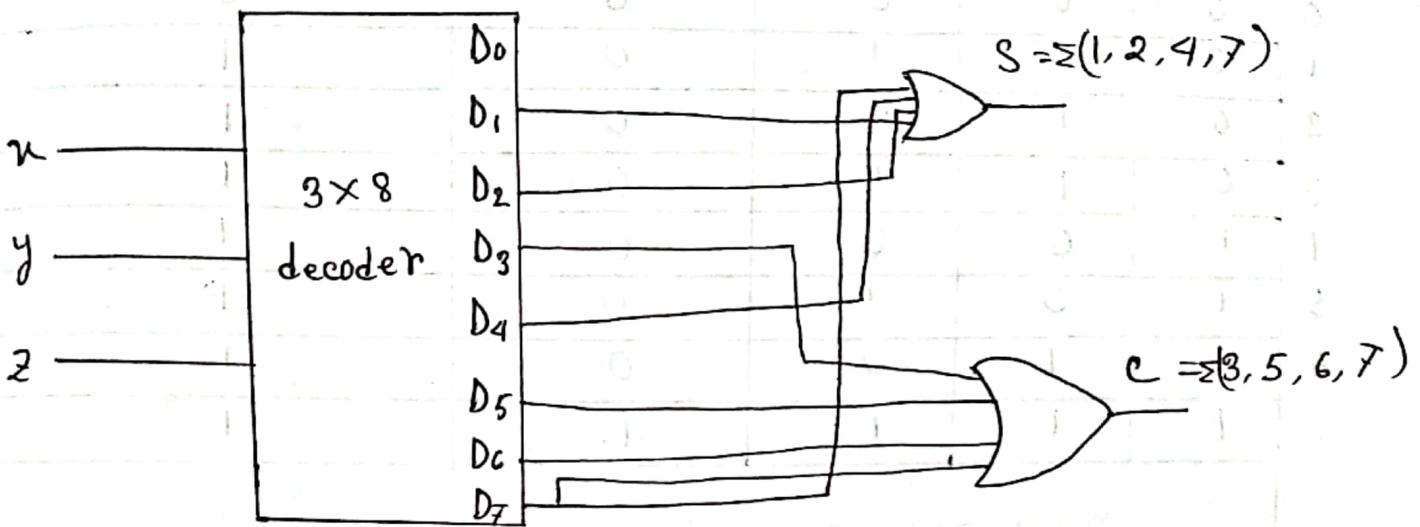
$$\Sigma P = 10$$

Σ = sum of minterms

$$\Sigma P = 10$$

$$\Sigma P = 11$$

$$\Sigma P = 10$$



Implementation of a full adder with a decoder

- * Implement the function $F(u, y, z) = uy + yz + zu$ and $H(u, y, z) = u + y + z + uyz$.

Ans:

u	y	z	uy	yz	zu	$uy + yz + zu$
0	0	0	0	0	0	0
1	0	1	0	0	0	0
2	0	1	0	0	0	0
3	0	1	0	1	0	1
4	1	0	0	0	0	0
5	1	0	1	0	1	1
6	1	1	0	0	0	1
7	1	1	1	1	1	1

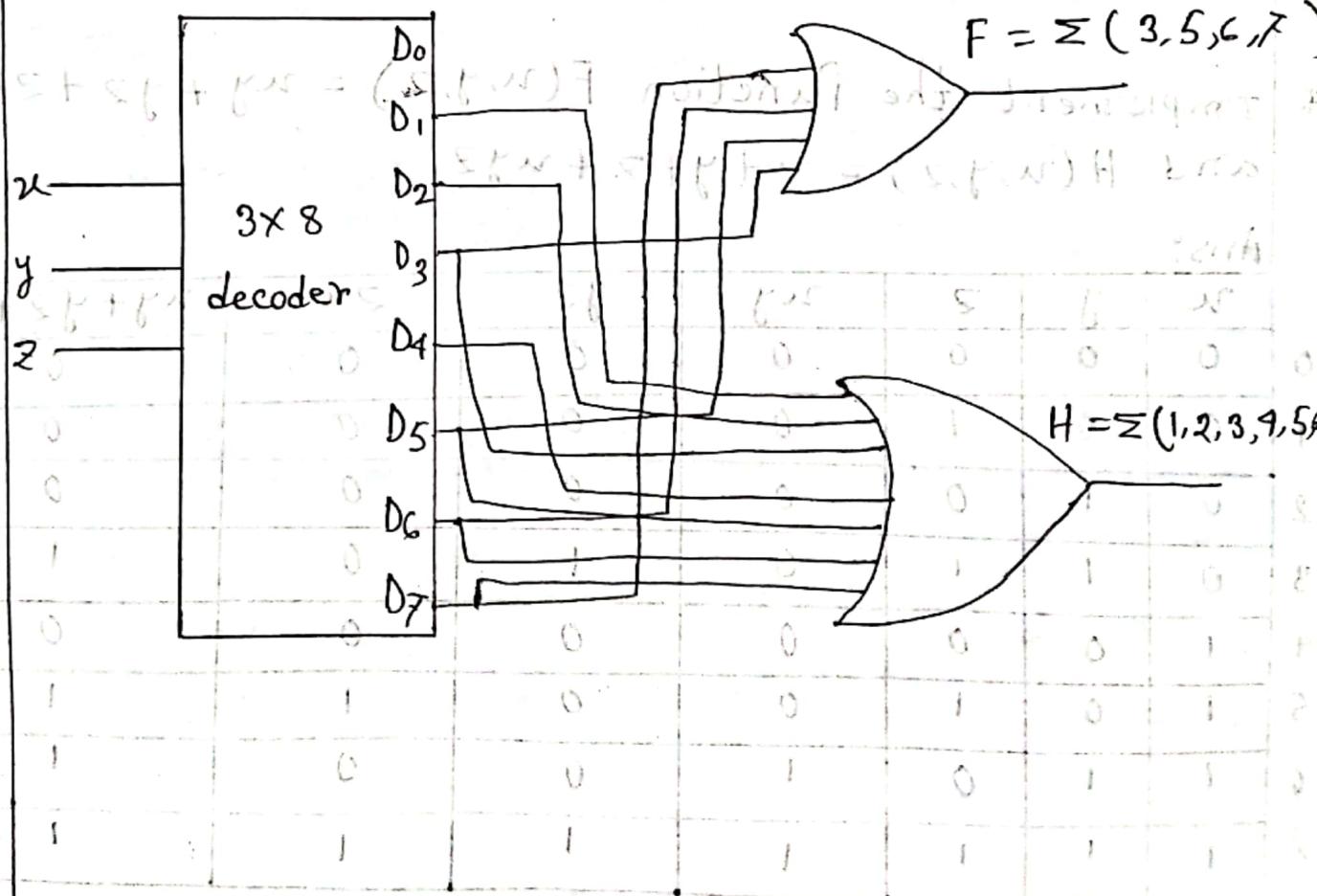
$$F = \sum(3, 5, 6, 7)$$

u	y	z	uyz	$uy + z + uyz$
0	0	0	0	0
1	0	1	0	1
2	1	0	0	1
3	0	1	0	1
4	1	0	0	1
5	1	1	0	1
6	1	0	0	1
7	1	1	1	1

$$H(u, y, z) = \sum(1, 2, 3, 4, 5, 6, 7)$$

These are the minterms of the function.

$$F = \sum(3, 5, 6, 7)$$



(S. S. S. P. L. S. T. T.)

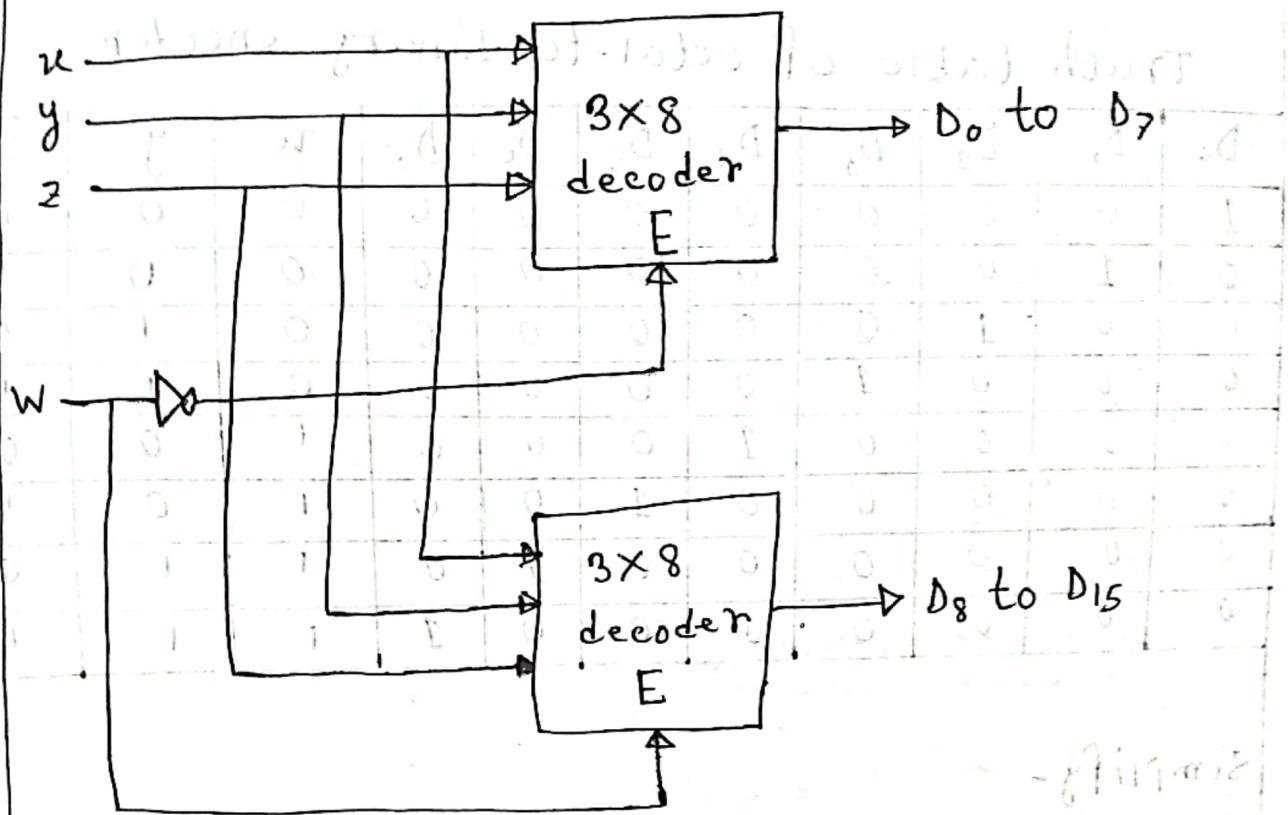


Figure: 4×16 decoder constructed with two 3×8 decoders

$$x_4 + x_6 + x_8 + x_9 = 6$$

$$x_4 + x_5 + x_6 + x_7 = 8$$

* Encoder: 2^n Input n output

Truth table of octal-to-binary encoder

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	u	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Simplify -

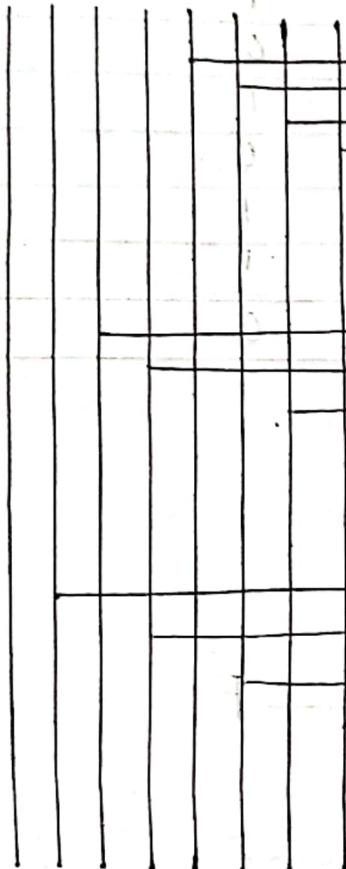
$$u = D_4 + D_5 + D_6 + D_7$$

$$y = D_2 + D_3 + D_6 + D_7$$

$$z = D_1 + D_3 + D_5 + D_7$$

Diagram -

$D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7$



$$u = D_4 + D_5 + D_6 + D_7$$

$$y = D_2 + D_3 + D_6 + D_7$$

$$z = D_1 + D_3 + D_5 + D_7$$

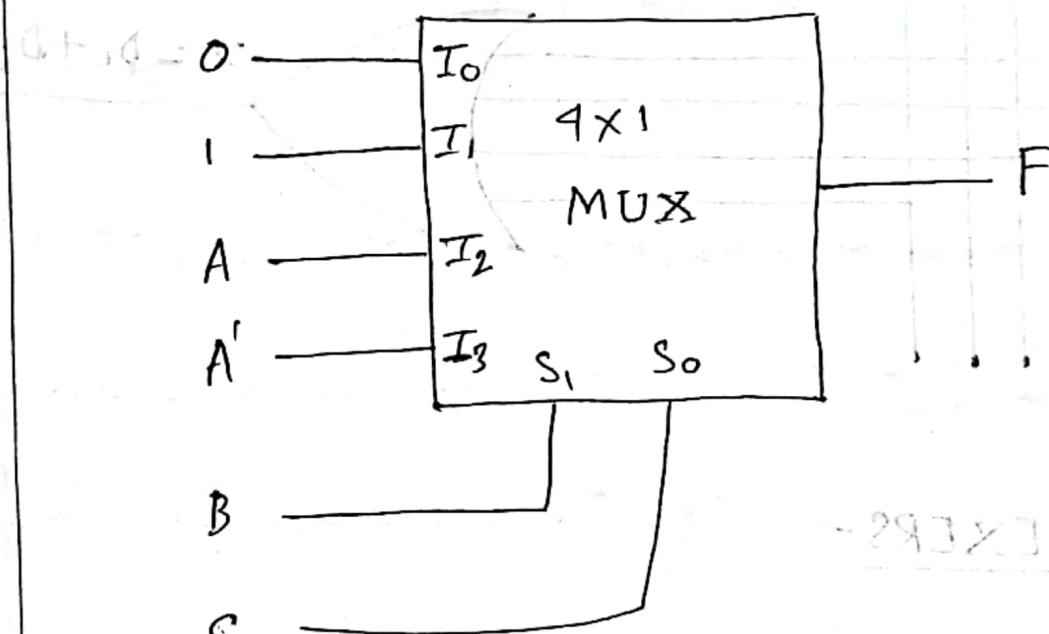
* MULTI PLEXERS -

$$F(A, B, C) = \Sigma(1, 3, 5, 6)$$

Multiple select multi output

Truth table -

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



(a, b, c) \geq (d, e, f)

Multiplexer implementation

A'	I_0	I_1	I_2	I_3
0	①	2	③	
4	⑤	⑥	7	
0	1	A	A'	

Implementation table of subfunction A

Now we have to find out what address is required
 Fig - Implementing $F(A, B, C) = \sum(1, 3, 5, 6)$ with a
 multiplexer

Half adder has been used as a subfunction A &

other half adder has been used as a subfunction B

and also implies "2" to implement a full adder

* Multiplexing means transmitting a large number of information units over a smaller number of channels or lines.

* An encoder is a digital function that produces a reverse operation from that of a decoder.

An encoder has 2^n input lines and n output lines.

* A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.