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| Tool Version : Vivado v.2014.4 (win64) Build 1071353 Tue Nov 18 18:29:27 MST 2014

| Date : Tue Feb 24 20:50:54 2015

| Host : ECJ1-222-04 running 64-bit Service Pack 1 (build 7601) | Command : report_timing_summary -warn_on_violation -max_paths 10 -file

top_timing_summary_routed.rpt -rpx top_timing_summary_routed.rpx

| Design : top

| Device : 7a35t-cpg236

| Speed File : -1 PRODUCTION 1.14 2014-09-11

| Temperature Grade : C

Timing Summary Report

| Timer Settings

Enable Multi Corner Analysis : Yes
Enable Pessimism Removal : Yes

Pessimism Removal Resolution : Nearest Common Node

Enable Input Delay Default Clock : No Enable Preset / Clear Arcs : No Disable Flight Delays : No

Corner Analyze Analyze
Name Max Paths Min Paths
----- Slow Yes Yes
Fast Yes Yes

check_timing report

Table of Contents

- checking no_clock
- 2. checking constant_clock
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- 8. checking generated_clocks
- 9. checking loops
- 10. checking partial_input_delay
- 11. checking partial_output_delay
- 12. checking unexpandable clocks
- 13. checking latch_loops
- checking no_clock

There are 9 register/latch pins with no clock driven by root clock pin: divide/counter_reg[24]/C (HIGH) 2. checking constant_clock -----There are 0 register/latch pins with constant clock. checking pulse_width_clock There are 0 register/latch pins which need pulse_width check 4. checking unconstrained_internal_endpoints There are 21 pins that are not constrained for maximum delay. (HIGH) There are 0 pins that are not constrained for maximum delay due to constant clock. 5. checking no_input_delay There is 1 input port with no input delay specified. (HIGH) There are 0 input ports with no input delay but user has a false path constraint. 6. checking no_output_delay There are 8 ports with no output delay specified. (HIGH) There are 0 ports with no output delay but user has a false path constraint There are 0 ports with no output delay but with a timing clock defined on it or propagating through it 7. checking multiple_clock -----There are 0 register/latch pins with multiple clocks. 8. checking generated_clocks There are 0 generated clocks that are not connected to a clock source.

9. checking loops

There are 0 combinational loops in the design.

10. checking partial_input_delay

There are 0 input ports with partial input delay specified.

	g partial_output_de							
	ports with partia		specifie	d.				
	g unexpandable_cloc							
There are 0	unexpandable cloc	k pairs.						
13. checking	g latch_loops							
There are 0	combinational lat	ch loops in th	e design	through latch	input			
Design Tim	ning Summary							
· 								
Failing Endp Endpoints		ndpoints W	IPWS(ns)	TPWS(ns)	TPWS Failing			
	0.000		0		25 0.	.254	0.000	
0		4.500	.000		0	. 234	26	
Clock	•		Frequ	ency(MHz)				
Intra Cloc	k Table							
Clock THS(ns) THS TPWS Total E	WNS(ns) Failing Endpoints Endpoints			WPWS(ns)			WHS(ns) ailing Endp	oint
sys_clk_pin 0.000	7.502 0	0.000	25	0 4.500	0.000	25	0.254	0

```
______
| Inter Clock Table
| -----
From Clock To Clock
                    WNS(ns)
                             TNS(ns) TNS Failing Endpoints TNS Total Endpoints
WHS(ns)
        THS(ns) THS Failing Endpoints THS Total Endpoints
                 -----
------
Other Path Groups Table
| -----
______
Path Group From Clock To Clock
                              WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total
Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints
        | Timing Details
| -----
------
------
From Clock: sys_clk_pin
 To Clock: sys_clk_pin

    Failing Endpoints, Worst Slack
    Failing Endpoints, Worst Slack
    Failing Endpoints, Worst Slack
    Failing Endpoints, Worst Slack
    Fooms, Total Violation

                                                              0.000ns
Setup :
                                                              0.000ns
Max Delay Paths
______
Slack (MET): 7.502ns (required time - arrival time)
                 divide/counter_reg[2]/C
                   (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                 divide/counter_reg[22]/D
                   (rising edge-triggered cell FDRE clocked by sys clk pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                 sys_clk_pin
 Path Type:
               Setup (Max at Slow Process Corner)
 Requirement:
Data Path Delay:

'ovels:

6 (CARRY4=6)

9 028ns (DCD
               10.000ns (sys clk pin rise@10.000ns - sys clk pin rise@0.000ns)
               2.543ns (logic 1.966ns (77.305%) route 0.577ns (22.695%))
 Clock Path Skew:
                -0.028ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): 4.856ns = (14.856 - 10.000)
```

```
Source Clock Delay (SCD): 5.158ns
   Clock Pessimism Removal (CPR):
                                0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ):
Total Input Jitter (TIJ):
                                0.071ns
                                0.000ns
   Discrete Jitter
                       (DJ): 0.000ns
   Phase Error
                        (PE):
                                0.000ns
   Location
                    Delay type
                                           Incr(ns) Path(ns)
                                                               Netlist Resource(s)
  _____
                                                              -----
                     (clock sys_clk_pin rise edge)
                                              0.000
                                                     0.000 r
   W5
                                              0.000 0.000 r clk100Mhz
                     net (fo=0)
                                             0.000 0.000 clk100Mhz
                                            1.458 1.458 r clk100Mhz_IBUF_inst/0
                     IBUF (Prop ibuf I 0)
                                        0.096 3.521 r clk100Mhz_IBUF_BUFG_inst/0
1.637 5.158 divide/71
                     net (fo=1, routed)
   BUFGCTRL_X0Y0
                     BUFG (Prop_bufg_I_0)
                     net (fo=25, routed)
   SLICE X2Y7
                                                        r divide/counter_reg[2]/C
  _____
                                                             -----
                     FDRE (Prop_fdre_C_Q)
                                            0.518 5.676 r divide/counter_reg[2]/Q
   SLICE_X2Y7
                     net (fo=1, routed)
                                              0.577 6.253 divide/n_0_counter_reg[2]
   SLICE X2Y7
                     CARRY4 (Prop_carry4_S[1]_CO[3])
                                              0.657 6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                      6.910
                                                               divide/n_0_counter_reg[5]_i_2
   SLICE X2Y8
                     CARRY4 (Prop carry4 CI CO[3])
                                              0.117
                                                      7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                      7.027
                                                               divide/n 0 counter reg[9] i 2
   SLICE X2Y9
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                      7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                       7.144
                                                               divide/n 0 counter reg[13] i 2
   SLICE X2Y10
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                       7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                       7.261
                                                               divide/n_0_counter_reg[17]_i_2
   SLICE_X2Y11
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                       7.378 r
divide/counter_reg[18]_i_2_CARRY4/CO[3]
                                              0.000
                     net (fo=1, routed)
                                                       7.378
                                                               divide/n_0_counter_reg[21]_i_2
   SLICE X2Y12
                     CARRY4 (Prop_carry4_CI_0[1])
                                              0.323
                                                       7.701 r
divide/counter_reg[22]_i_2_CARRY4/0[1]
                    net (fo=1, routed)
                                              0.000
                                                       7.701
                                                               divide/n_0_counter_reg[22]_i_1
   SLICE_X2Y12
                   FDRE
                                                       r divide/counter_reg[22]/D
                                                              ______
                     (clock sys clk pin rise edge)
                                             10.000
                                                      10.000 r
   W5
                                              0.000
                                                      10.000 r clk100Mhz
                     net (fo=0)
                                             0.000 10.000 clk100Mhz
   W5
                     IBUF (Prop_ibuf_I_0)
                                             1.388 11.388 r clk100Mhz_IBUF_inst/0
                     net (fo=1, routed)
                                            1.862 13.250 clk100Mhz_IBUF
                                        0.091 13.341 r clk100Mhz_IBUF_BUFG_inst/0
                     BUFG (Prop_bufg_I_0)
   BUFGCTRL_X0Y0
                     net (fo=25, routed)
                                             1.515 14.856 divide/clk
```

```
SLICE_X2Y12
                                                           r divide/counter_reg[22]/C
                                            0.274
                     clock pessimism
                                                     15.130
                     clock uncertainty
                                            -0.035
                                                     15.095
                FDRE (Setup_fdre_C_D)
                                           0.109
   SLICE_X2Y12
                                                     15.204
                                                              divide/counter_reg[22]
 _____
                    required time
                                                     15.204
                    arrival time
 ______
                                                      7.502
                     slack
Slack (MET) :
                     7.511ns (required time - arrival time)
 Source:
                     divide/counter_reg[2]/C
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                      divide/counter_reg[24]/D
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin \{ rise @ 0.000 ns \} 
fall@5.000ns period=10.000ns})
 Path Group:
                     sys_clk_pin
 Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 2.534ns (logic 1.957ns (77.224%) route 0.577ns (22.776%))

Logic Levels: 6 (CARRY4=6)

Clock Path Skew: -0.028ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD):
                               4.856ns = ( 14.856 - 10.000 )
   Source Clock Delay (SCD):
                               5.158ns
   Clock Pessimism Removal (CPR):
                               0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
   Discrete Jitter
                       (DJ):
                                0.000ns
   Phase Error
                       (PE):
                                0.000ns
   Location
             Delay type
                                 Incr(ns) Path(ns) Netlist Resource(s)
 _____
                                                             -----
                    (clock sys_clk_pin rise edge)
                                              0.000 0.000 r
   W5
                                             0.000 0.000 r clk100Mhz
                     net (fo=0)
                                            0.000 0.000 clk100Mhz
                     IBUF (Prop_ibuf_I_0)
                                            1.458 1.458 r clk100Mhz_IBUF_inst/0
   W5
                                           1.967 3.425 clk100Mhz_IBUF
                     net (fo=1, routed)
                     BUFGCTRL_X0Y0
                                                        r divide/counter_reg[2]/C
   SLICE_X2Y7
 ______
                                                             _____
   SLICE_X2Y7
                   FDRE (Prop_fdre_C_Q) 0.518 5.676 r divide/counter_reg[2]/Q
                    net (fo=1, routed)
                                           0.577 6.253 divide/n_0_counter_reg[2]
   SLICE_X2Y7
             CARRY4 (Prop_carry4_S[1]_CO[3])
                                              0.657 6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                     6.910
                                                              divide/n 0 counter reg[5] i 2
   SLICE X2Y8
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                             0.000
                                                     7.027 divide/n_0_counter_reg[9]_i_2
   SLICE_X2Y9
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
```

```
net (fo=1, routed)
                                              0.000
                                                       7.144
                                                               divide/n_0_counter_reg[13]_i_2
   SLICE_X2Y10
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                       7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                       7.261
                                                               divide/n_0_counter_reg[17]_i_2
   SLICE X2Y11
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                       7.378 r
divide/counter_reg[18]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                       7.378
                                                               divide/n_0_counter_reg[21]_i_2
   SLICE X2Y12
                     CARRY4 (Prop_carry4_CI_0[3])
                                              0.314
                                                       7.692 r
divide/counter_reg[22]_i_2_CARRY4/0[3]
                     net (fo=1, routed)
                                              0.000
                                                       7.692
                                                               divide/n_0_counter_reg[24]_i_1
   SLICE X2Y12
                     FDRE
                                                          r divide/counter_reg[24]/D
  _____
                     (clock sys_clk_pin rise edge)
                                             10.000
                                                      10.000 r
   W5
                                              0.000
                                                      10.000 r clk100Mhz
                     net (fo=0)
                                              0.000
                                                      10.000 clk100Mhz
   W5
                     IBUF (Prop_ibuf_I_0)
                                            1.388 11.388 r clk100Mhz_IBUF_inst/0
                     net (fo=1, routed)
                                             1.862 13.250 clk100Mhz_IBUF
                                            0.091 13.341 r clk100Mhz_IBUF_BUFG_inst/0
   BUFGCTRL_X0Y0
                     BUFG (Prop_bufg_I_0)
                                             1.515 14.856 divide/clk
                     net (fo=25, routed)
   SLICE_X2Y12
                                                      r divide/counter_reg[24]/C
                                             0.274
                     clock pessimism
                                                     15.130
                     clock uncertainty
                                             -0.035
                                                      15.095
                     FDRE (Setup_fdre_C_D) 0.109
   SLICE X2Y12
                                                      15.204
                                                              divide/counter_reg[24]
  ______
                     required time
                     arrival time
                                                      -7.692
  ______
                     slack
                                                       7.511
Slack (MET) :
                      7.586ns (required time - arrival time)
 Source:
                      divide/counter_reg[2]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                      divide/counter_reg[23]/D
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                     sys_clk_pin
                      Setup (Max at Slow Process Corner)
 Path Type:
 Requirement:
                    10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
 Data Path Delay:
                    2.459ns (logic 1.882ns (76.529%) route 0.577ns (23.471%))
 Logic Levels:
                    6 (CARRY4=6)
 Clock Path Skew: -0.028ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 4.856ns = ( 14.856 - 10.000 )
   Source Clock Delay (SCD):
                                5.158ns
   Clock Pessimism Removal (CPR):
                                0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ):
                                0.071ns
   Total Input Jitter
                      (TIJ):
                                0.000ns
   Discrete Jitter
                        (DJ):
                                0.000ns
                        (PE):
   Phase Error
                                0.000ns
   Location
                   Delay type
                                           Incr(ns) Path(ns) Netlist Resource(s)
```

	(clock eye alk nin nico			
	(clock sys_clk_pin rise	0.000	0.000 r	
W5		0.000	0.000 r	clk100Mhz
W	net (fo=0)	0.000	0.000	clk100Mhz
W5	IBUF (Prop_ibuf_I_O)	1.458		clk100Mhz_IBUF_inst/0
5	net (fo=1, routed)	1.967	3.425	clk100Mhz_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_0)	0.096	3.521 r	-
	net (fo=25, routed)	1.637	5.158	divide/clk
SLICE_X2Y7	, , ,		r	divide/counter_reg[2]/C
SLICE_X2Y7	<pre>FDRE (Prop_fdre_C_Q)</pre>	0.518	5.676 r	divide/counter_reg[2]/Q
	net (fo=1, routed)	0.577	6.253	divide/n_0_counter_reg[2]
SLICE_X2Y7	CARRY4 (Prop_carry4_S[1]	_CO[3])		
		0.657	6.910 r	
<pre>divide/counter_reg[2]</pre>				
	net (fo=1, routed)	0.000	6.910	divide/n_0_counter_reg[5]_i_2
SLICE_X2Y8	CARRY4 (Prop_carry4_CI_C	0[3])		
		0.117	7.027 r	
<pre>divide/counter_reg[6]</pre>				
C. T.C.T. V.O.V.O.	net (fo=1, routed)	0.000	7.027	divide/n_0_counter_reg[9]_i_2
SLICE_X2Y9	CARRY4 (Prop_carry4_CI_C			
d::d=/	1 ÷ 2 CARRYA/CO[2]	0.117	7.144 r	
divide/counter_reg[10]_1_2_CARRY4/CU[3] net (fo=1, routed)	0.000	7 144	divide/n 0 country neg[12] i 2
CLICE VOVIA		0.000	7.144	divide/n_0_counter_reg[13]_i_2
SLICE_X2Y10	CARRY4 (Prop_carry4_CI_C	0.117	7.261 r	
divide/counter_reg[14	1 ; 2 CAPPV4/CO[3]	0.117	7.201 1	
divide/ codificer_reg[14	net (fo=1, routed)	0.000	7.261	divide/n_0_counter_reg[17]_i_2
SLICE_X2Y11	CARRY4 (Prop_carry4_CI_C		7.201	u1v1uc/11_0_counter_1 cg[1/]_1_2
321C2_X2111	c/ (1.10p_cd.1.y i_c1_c	0.117	7.378 r	
divide/counter_reg[18	l i 2 CARRY4/CO[3]	01227	,,,,,,	
01	net (fo=1, routed)	0.000	7.378	divide/n_0_counter_reg[21]_i_2
SLICE_X2Y12	CARRY4 (Prop_carry4_CI_0	[2])		
_		0.239	7.617 r	
divide/counter_reg[22]_i_2_CARRY4/0[2]			
	net (fo=1, routed)	0.000	7.617	divide/n_0_counter_reg[23]_i_1
SLICE_X2Y12	FDRE		r	divide/counter_reg[23]/D
	<pre>(clock sys_clk_pin rise</pre>	edge)		
		10.000	10.000 r	
W5		0.000	10.000 r	
	net (fo=0)	0.000	10.000	clk100Mhz
W5	IBUF (Prop_ibuf_I_O)	1.388		clk100Mhz_IBUF_inst/0
DUECCEDI VOVO	net (fo=1, routed)	1.862	13.250	clk100Mhz_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_0)	0.091		clk100Mhz_IBUF_BUFG_inst/O
CLICE VOVIO	net (fo=25, routed)	1.515	14.856	<pre>divide/clk divide/counter_reg[23]/C</pre>
SLICE_X2Y12	clock pessimism	0 274	r 15.130	aivide/codiffer_reg[53]/C
	clock pessimism clock uncertainty	0.274 -0.035	15.130	
SLICE_X2Y12	FDRE (Setup_fdre_C_D)	0.109	15.204	divide/counter_reg[23]
JLICL_/\Z11Z			13.207	artrac, counter _1 eg[25]
	required time		15.204	
	arrival time		-7.617	
	slack		7.586	

```
Slack (MET) :
                         7.607ns (required time - arrival time)
 Source:
                         divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys clk pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                          divide/counter reg[21]/D
                           (rising edge-triggered cell FDRE clocked by sys clk pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                        sys_clk_pin
 Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 2.438ns (logic 1.861ns (76.327%) route 0.577ns (23.673%))

Logic Levels: 6 (CARRY4=6)
 Clock Path Skew: -0.028ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 4.856ns = ( 14.856 - 10.000 )
   Source Clock Delay (SCD):
                                   5.158ns
   Clock Pessimism Removal (CPR): 0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ):
                                    0.071ns
   Total Input Jitter (TIJ):
                                     0.000ns
                          (DJ): 0.000ns
   Discrete Jitter
   Phase Error
                           (PE): 0.000ns
   Location
                      Delay type
                                                 Incr(ns) Path(ns) Netlist Resource(s)
                                                                        -----
  ______
                        (clock sys_clk_pin rise edge)
                                                            0.000 r
                                                     0.000
                                                    0.000 0.000 r clk100Mhz
   W5
                        net (fo=0)
                                                   0.000 0.000 clk100Mhz
                        IBUF (Prop_ibuf_I_0) 1.458 1.458 r clk100Mhz_IBUF_inst/0
net (fo=1, routed) 1.967 3.425 clk100Mhz_IBUF
BUFG (Prop_bufg_I_0) 0.096 3.521 r clk100Mhz_IBUF_BUFG_inst/0
net (fo=25, routed) 1.637 5.158 divide/clk
   BUFGCTRL_X0Y0
   SLICE X2Y7
                                                                r divide/counter_reg[2]/C
  FDRE (Prop_fdre_C_Q) 0.518 5.676 r divide/counter_reg[2]/Q net (fo=1, routed) 0.577 6.253 divide/n_0_counter_reg[2]
    SLICE_X2Y7
                                                   0.577 6.253 divide/n_0_counter_reg[2]
   SLICE X2Y7
                        CARRY4 (Prop_carry4_S[1]_CO[3])
                                                     0.657 6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)
                                                     0.000
                                                               6.910
                                                                        divide/n_0_counter_reg[5]_i_2
   SLICE X2Y8
                        CARRY4 (Prop_carry4_CI_CO[3])
                                                              7.027 r
                                                     0.117
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)
                                                     0.000
                                                               7.027
                                                                        divide/n_0_counter_reg[9]_i_2
    SLICE X2Y9
                        CARRY4 (Prop_carry4_CI_CO[3])
                                                     0.117
                                                               7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)
                                                     0.000
                                                               7.144
                                                                        divide/n 0 counter reg[13] i 2
    SLICE X2Y10
                        CARRY4 (Prop_carry4_CI_CO[3])
                                                     0.117
                                                               7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)
                                                     0.000
                                                               7.261
                                                                        divide/n_0_counter_reg[17]_i_2
   SLICE X2Y11
                        CARRY4 (Prop_carry4_CI_CO[3])
                                                     0.117
                                                               7.378 r
divide/counter_reg[18]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)
                                                   0.000
                                                               7.378
                                                                        divide/n_0_counter_reg[21]_i_2
```

```
SLICE_X2Y12 CARRY4 (Prop_carry4_CI_0[0])
                                            0.218
                                                    7.596 r
divide/counter_reg[22]_i_2_CARRY4/0[0]
                    net (fo=1, routed)
                                          0.000 7.596 divide/n_0_counter_reg[21]_i_1
   SLICE X2Y12
                    FDRF
                                                        r divide/counter_reg[21]/D
 _____
                    (clock sys_clk_pin rise edge)
                                           10.000
                                                    10.000 r
   W5
                                            0.000 10.000 r clk100Mhz
                    net (fo=0)
                                           0.000 10.000 clk100Mhz
                    W5
   BUFGCTRL_X0Y0
                                                    r divide/counter_reg[21]/C
   SLICE_X2Y12
                                           0.274 15.130
                    clock pessimism
                    clock uncertainty
                                           -0.035
                                                   15.095
                    FDRE (Setup_fdre_C_D) 0.109
   SLICE X2Y12
                                                   15.204
                                                            divide/counter_reg[21]
 _____
                    required time
                                                    15.204
                    arrival time
                                                    7.607
                    slack
Slack (MET) :
                     7.620ns (required time - arrival time)
 Source:
                    divide/counter reg[2]/C
                      (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                     divide/counter reg[18]/D
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                    sys_clk_pin
 Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 2.426ns (logic 1.849ns (76.210%) route 0.577ns (23.790%))

Logic Levels: 5 (CARRY4=5)

Clock Path Skew: -0.027ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 4.857ns = ( 14.857 - 10.000 )
   Source Clock Delay (SCD):
                              5.158ns
   Clock Pessimism Removal (CPR):
                              0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ): 0.071ns
   Total Input Jitter (TIJ): 0.000ns
   Discrete Jitter
                      (DJ):
                               0.000ns
   Phase Error
                       (PE):
                               0.000ns
                                Incr(ns) Path(ns) Netlist Resource(s)
   Location
             Delay type
 _____
                                                           -----
                    (clock sys_clk_pin rise edge)
                                            0.000
                                                  0.000 r
   W5
                                            0.000 0.000 r clk100Mhz
                    net (fo=0)
                                           0.000 0.000 clk100Mhz
   W5
                    IBUF (Prop_ibuf_I_0)
                                           1.458 1.458 r clk100Mhz_IBUF_inst/0
                                          1.967 3.425 clk100Mhz_IBUF
                    net (fo=1, routed)
                    BUFGCTRL_X0Y0
```

```
SLICE_X2Y7
                                                             r divide/counter_reg[2]/C
                                                               -----
                   FDRE (Prop_fdre_C_Q) 0.518 5.676 r divide/counter_reg[2]/Q net (fo=1, routed) 0.577 6.253 divide/n_0_counter_reg[2]
   SLICE_X2Y7
   SLICE X2Y7
                   CARRY4 (Prop_carry4_S[1]_CO[3])
                                               0.657
                                                       6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                       6.910
                                                                divide/n_0_counter_reg[5]_i_2
   SLICE X2Y8
                     CARRY4 (Prop_carry4_CI_CO[3])
                                               0.117
                                                       7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                               0.000
                                                       7.027
                                                               divide/n_0_counter_reg[9]_i_2
   SLICE X2Y9
                     CARRY4 (Prop_carry4_CI_CO[3])
                                               0.117
                                                       7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                                               0.000
                                                       7.144
                     net (fo=1, routed)
                                                               divide/n_0_counter_reg[13]_i_2
   SLICE_X2Y10
                     CARRY4 (Prop_carry4_CI_CO[3])
                                               0.117
                                                       7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                                               0.000
                     net (fo=1, routed)
                                                       7.261
                                                                divide/n_0_counter_reg[17]_i_2
   SLICE_X2Y11
                     CARRY4 (Prop_carry4_CI_0[1])
                                               0.323
                                                       7.584 r
divide/counter_reg[18]_i_2_CARRY4/0[1]
                     net (fo=1, routed)
                                             0.000
                                                        7.584
                                                                divide/n_0_counter_reg[18]_i_1
   SLICE_X2Y11
                     FDRE
                                                        r divide/counter_reg[18]/D
  _____
                                                                -----
                      (clock sys_clk_pin rise edge)
                                              10.000
                                                       10.000 r
   W5
                                              0.000 10.000 r clk100Mhz
                     net (fo=0)
                                             0.000 10.000 clk100Mhz
                                           1.388 11.388 r clk100Mhz_IBUF_inst/0
1.862 13.250 clk100Mhz_IBUF
   W5
                     IBUF (Prop_ibuf_I_0)
                     net (fo=1, routed)
                                            0.091
                     BUFG (Prop_bufg_I_0)
   BUFGCTRL X0Y0
                                                      13.341 r clk100Mhz_IBUF_BUFG_inst/0
                     net (fo=25, routed)
                                             1.516 14.857 divide/clk
                                                       r divide/counter_reg[18]/C
   SLICE_X2Y11
                     clock pessimism
                                             0.274 15.131
                     clock uncertainty
                                             -0.035
                                                       15.096
                     FDRE (Setup_fdre_C_D)
   SLICE_X2Y11
                                             0.109
                                                       15.205
                                                               divide/counter_reg[18]
  ______
                     required time
                                                       15.205
                     arrival time
                                                       -7.584
  _____
                     slack
                                                        7.620
Slack (MET) :
                      7.629ns (required time - arrival time)
 Source:
                      divide/counter_reg[2]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                      divide/counter reg[20]/D
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                     sys clk pin
 Path Type:
                      Setup (Max at Slow Process Corner)
 Requirement:
                     10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
 Data Path Delay:
                    2.417ns (logic 1.840ns (76.122%) route 0.577ns (23.878%))
 Logic Levels:
                     5 (CARRY4=5)
```

```
-0.027ns (DCD - SCD + CPR)
 Clock Path Skew:
   Destination Clock Delay (DCD): 4.857ns = ( 14.857 - 10.000 )
   Source Clock Delay (SCD):
                                5.158ns
   Clock Pessimism Removal (CPR):
                                0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ):
                                0.071ns
   Total Input Jitter (TIJ):
                                0.000ns
   Discrete Jitter
                       (DJ):
                                0.000ns
                       (PE):
   Phase Error
                                0.000ns
                                          Incr(ns) Path(ns) Netlist Resource(s)
                   Delay type
   Location
 _____
                     (clock sys_clk_pin rise edge)
                                              0.000
                                                      0.000 r
                                              0.000 0.000 r clk100Mhz
   W5
                     net (fo=0)
                                             0.000 0.000 clk100Mhz
                     IBUF (Prop_ibuf_I_0)
                                            1.458 1.458 r clk100Mhz_IBUF_inst/0
   W5
                                            1.967 3.425 clk100Mhz_IBUF
                     net (fo=1, routed)
                                           0.096 3.521 r clk100Mhz_IBUF_BUFG_inst/0
   BUFGCTRL X0Y0
                     BUFG (Prop_bufg_I_0)
                     net (fo=25, routed)
                                            1.637 5.158 divide/clk
   SLICE_X2Y7
                                                       r divide/counter_reg[2]/C
 ------
   SLICE_X2Y7
                    FDRE (Prop_fdre_C_Q) 0.518
                                                      5.676 r divide/counter_reg[2]/Q
                                            0.577 6.253 divide/n_0_counter_reg[2]
                     net (fo=1, routed)
   SLICE_X2Y7
                     CARRY4 (Prop_carry4_S[1]_CO[3])
                                              0.657
                                                      6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                      6.910
                                                              divide/n_0_counter_reg[5]_i_2
   SLICE X2Y8
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                      7.027
                                                              divide/n_0_counter_reg[9]_i_2
   SLICE X2Y9
                     CARRY4 (Prop_carry4_CI_CO[3])
                                              0.117
                                                      7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                              0.000
                                                      7.144
                                                              divide/n_0_counter_reg[13]_i_2
   SLICE X2Y10
                     CARRY4 (Prop_carry4_CI_CO[3])
                                                      7.261 r
                                              0.117
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                                              0.000
                     net (fo=1, routed)
                                                      7.261
                                                              divide/n_0_counter_reg[17]_i_2
   SLICE_X2Y11
                     CARRY4 (Prop_carry4_CI_0[3])
                                              0.314
                                                      7.575 r
divide/counter_reg[18]_i_2_CARRY4/0[3]
                    net (fo=1, routed)
                                              0.000
                                                      7.575
                                                              divide/n_0_counter_reg[20]_i_1
   SLICE_X2Y11
                                                        r divide/counter_reg[20]/D
                     (clock sys_clk_pin rise edge)
                                             10.000
                                                     10.000 r
   W5
                                              0.000
                                                     10.000 r clk100Mhz
                     net (fo=0)
                                             0.000
                                                     10.000 clk100Mhz
   W5
                     IBUF (Prop_ibuf_I_0)
                                            1.388
                                                     11.388 r clk100Mhz IBUF inst/0
                     net (fo=1, routed)
                                            1.862 13.250 clk100Mhz IBUF
   BUFGCTRL_X0Y0
                     BUFG (Prop_bufg_I_0)
                                            0.091 13.341 r clk100Mhz_IBUF_BUFG_inst/0
                                            1.516 14.857
                     net (fo=25, routed)
                                                              divide/clk
   SLICE_X2Y11
                                                      r divide/counter_reg[20]/C
                     clock pessimism
                                            0.274
                                                     15.131
```

```
clock uncertainty -0.035 15.096 FDRE (Setup_fdre_C_D) 0.109 15.205
   SLICE_X2Y11
                                                                   divide/counter_reg[20]
  -----
                      required time
                                                         15.205
                      arrival time
                                                         -7.575
 ______
                      slack
Slack (MET) :
                       7.704ns (required time - arrival time)
 Source:
                       divide/counter_reg[2]/C
                         (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                       divide/counter_reg[19]/D
                         (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                       sys_clk_pin
 Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 2.342ns (logic 1.765ns (75.357%) route 0.577ns (24.643%))

Logic Levels: 5 (CARRY4=5)

Clock Path Skew: -0.027ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 4.857ns = ( 14.857 - 10.000 )
   Source Clock Delay (SCD): 5.158ns
   Clock Pessimism Removal (CPR): 0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
   Phase Error
                         (PE): 0.000ns
   Location
               Delay type
                                            Incr(ns) Path(ns) Netlist Resource(s)
  ------
                      (clock sys_clk_pin rise edge)
                                                 0.000
                                                        0.000 r
   W5
                                                0.000 0.000 r clk100Mhz
                      net (fo=0)
                                               0.000 0.000 clk100Mhz
                                              W5
                      IBUF (Prop_ibuf_I_0)
                      net (fo=1, routed)
                      BUFGCTRL_X0Y0
                                                           r divide/counter_reg[2]/C
   SLICE_X2Y7
                      FDRE (Prop_fdre_C_Q) 0.518 5.676 r divide/counter_reg[2]/Q net (fo=1, routed) 0.577 6.253 divide/n_0_counter_reg[2]
   SLICE_X2Y7
                                               0.577 6.253 divide/n_0_counter_reg[2]
   SLICE_X2Y7
                    CARRY4 (Prop_carry4_S[1]_CO[3])
                                                0.657 6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                      net (fo=1, routed)
                                                 0.000 6.910
                                                                  divide/n_0_counter_reg[5]_i_2
   SLICE X2Y8
                      CARRY4 (Prop_carry4_CI_CO[3])
                                                 0.117
                                                         7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                      net (fo=1, routed)
                                                 0.000
                                                          7.027
                                                                   divide/n_0_counter_reg[9]_i_2
   SLICE X2Y9
                      CARRY4 (Prop_carry4_CI_CO[3])
                                                 0.117
                                                          7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                      net (fo=1, routed) 0.000
                                                          7.144
                                                                  divide/n_0_counter_reg[13]_i_2
   SLICE X2Y10
                     CARRY4 (Prop_carry4_CI_CO[3])
```

```
0.117
                                                   7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                    net (fo=1, routed)
                                            0.000
                                                    7.261
                                                            divide/n_0_counter_reg[17]_i_2
   SLICE X2Y11
                    CARRY4 (Prop_carry4_CI_0[2])
                                            0.239
                                                    7.500 r
divide/counter_reg[18]_i_2_CARRY4/0[2]
                    net (fo=1, routed)
                                          0.000
                                                   7.500
                                                            divide/n 0 counter reg[19] i 1
   SLICE X2Y11
                   FDRE
                                                     r divide/counter_reg[19]/D
 -----
                    (clock sys_clk_pin rise edge)
                                           10.000
                                                   10.000 r
   W5
                                           0.000 10.000 r clk100Mhz
                    net (fo=0)
                                          0.000 10.000 clk100Mhz
                    W5
   BUFGCTRL_X0Y0
                    clock uncertainty

FDRF (Software)

0.274 15.131
   SLICE X2Y11
                                                    r divide/counter_reg[19]/C
                    FDRE (Setup_fdre_C_D)
   SLICE X2Y11
                                          0.109 15.205
                                                            divide/counter_reg[19]
                    required time
                                                   15.205
                    arrival time
                                                   -7.500
 -----
                    slack
                                                    7.704
Slack (MET) :
                    7.725ns (required time - arrival time)
                     divide/counter reg[2]/C
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                     divide/counter reg[17]/D
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group: sys_clk_pin
 Path Type:
                   Setup (Max at Slow Process Corner)
 Requirement:

Data Path Delay:

2.321ns (2.52 column)

5 (CARRY4=5)

2.927ns (DCD
                   10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
                   2.321ns (logic 1.744ns (75.134%) route 0.577ns (24.866%))
                    -0.027ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 4.857ns = (14.857 - 10.000)
   Source Clock Delay (SCD): 5.158ns
   Clock Pessimism Removal (CPR): 0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
   Discrete Jitter
                      (DJ):
                              0.000ns
   Phase Error
                      (PE):
                               0.000ns
   Location
                   Delay type
                                        Incr(ns) Path(ns) Netlist Resource(s)
 (clock sys_clk_pin rise edge)
                                            0.000 0.000 r
   W5
                                            0.000 0.000 r clk100Mhz
                                                  0.000 clk100Mhz
                    net (fo=0)
                                           0.000
   W5
                    IBUF (Prop_ibuf_I_0)
                                          1.458
                                                   1.458 r clk100Mhz IBUF inst/0
```

```
net (fo=1, routed) 1.967 3.425 clk100Mhz_IBUF
BUFG (Prop_bufg_I_0) 0.096 3.521 r clk100Mhz_IBUF_BUFG_inst/0
net (fo=25, routed) 1.637 5.158 divide/clk
   BUFGCTRL_X0Y0
                                                              r divide/counter_reg[2]/C
   SLICE_X2Y7
  _____
                                                                  -----
                     FDRE (Prop_fdre_C_Q) 0.518 5.676 r divide/counter_reg[2]/Q
   SLICE X2Y7
                      net (fo=1, routed)
                                               0.577 6.253 divide/n_0_counter_reg[2]
                      CARRY4 (Prop_carry4_S[1]_CO[3])
   SLICE X2Y7
                                                         6.910 r
                                                 0.657
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                      net (fo=1, routed)
                                                 0.000
                                                          6.910
                                                                   divide/n 0 counter reg[5] i 2
   SLICE X2Y8
                      CARRY4 (Prop_carry4_CI_CO[3])
                                                 0.117
                                                          7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                      net (fo=1, routed)
                                                 0.000
                                                          7.027
                                                                   divide/n 0 counter reg[9] i 2
   SLICE X2Y9
                      CARRY4 (Prop_carry4_CI_CO[3])
                                                 0.117
                                                          7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                                                 0.000
                                                                   divide/n_0_counter_reg[13]_i_2
                      net (fo=1, routed)
                                                          7.144
   SLICE X2Y10
                      CARRY4 (Prop_carry4_CI_CO[3])
                                                 0.117
                                                          7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                                                 0.000
                      net (fo=1, routed)
                                                          7.261
                                                                   divide/n_0_counter_reg[17]_i_2
   SLICE_X2Y11
                      CARRY4 (Prop_carry4_CI_0[0])
                                                 0.218
                                                          7.479 r
divide/counter_reg[18]_i_2_CARRY4/0[0]
                      net (fo=1, routed)
                                                 0.000
                                                          7.479
                                                                   divide/n 0 counter reg[17] i 1
   SLICE X2Y11
                      FDRF
                                                              r divide/counter_reg[17]/D
                       (clock sys_clk_pin rise edge)
                                                10.000
                                                         10.000 r
   W5
                                                0.000
                                                         10.000 r clk100Mhz
                      net (fo=0)
                                                0.000
                                                         10.000 clk100Mhz
                                              1.388 11.388 r clk100Mhz_IBUF_inst/0
   W5
                      IBUF (Prop_ibuf_I_0)
                      net (fo=1, routed)
                                               1.862 13.250 clk100Mhz_IBUF
   BUFGCTRL X0Y0
                      BUFG (Prop_bufg_I_0)
                                               0.091 13.341 r clk100Mhz_IBUF_BUFG_inst/0
                      net (fo=25, routed)
                                               1.516 14.857
                                                                  divide/clk
   SLICE_X2Y11
                                                          r divide/counter_reg[17]/C
                                               0.274
                      clock pessimism
                                                         15.131
                      clock uncertainty
                      clock uncertainty -0.035
FDRE (Setup_fdre_C_D) 0.109
                                                         15.096
   SLICE X2Y11
                                                         15.205
                                                                   divide/counter_reg[17]
  ______
                      required time
                                                         15.205
                      arrival time
                                                          7.725
                      slack
Slack (MET) :
                       7.738ns (required time - arrival time)
 Source:
                       divide/counter reg[2]/C
                         (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                       divide/counter reg[14]/D
                         (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                       sys_clk_pin
 Path Type:
                       Setup (Max at Slow Process Corner)
```

```
10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
 Requirement:
                     2.309ns (logic 1.732ns (75.005%) route 0.577ns (24.995%))
 Data Path Delay:
 Logic Levels: 4 (CARRY4=4)
Clock Path Skew: -0.026ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 4.858ns = ( 14.858 - 10.000 )
   Source Clock Delay (SCD):
                                 5.158ns
   Clock Pessimism Removal (CPR): 0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ):
Total Input Jitter (TIJ):
                                  0.071ns
                                  0.000ns
   Discrete Jitter
                         (DJ):
                                 0.000ns
   Phase Error
                         (PE): 0.000ns
   Location
                    Delay type
                                            Incr(ns) Path(ns) Netlist Resource(s)
                      (clock sys_clk_pin rise edge)
                                                0.000
                                                         0.000 r
   W5
                                                0.000
                                                        0.000 r clk100Mhz
                      net (fo=0)
                                                        0.000 clk100Mhz
                                               0.000
                      IBUF (Prop_ibuf_I_0)
                                              1.458 1.458 r clk100Mhz_IBUF_inst/0
   W5
                      net (fo=1, routed)
                                               1.967 3.425 clk100Mhz_IBUF
   BUFGCTRL_X0Y0
                      BUFG (Prop_bufg_I_0)
                                              0.096 3.521 r clk100Mhz_IBUF_BUFG_inst/0
                                               1.637 5.158 divide/clk
                      net (fo=25, routed)
                                                             r divide/counter_reg[2]/C
   SLICE_X2Y7
                                                                 -----
                                            0.518 5.676 r divide/counter_reg[2]/Q
                      FDRE (Prop_fdre_C_Q)
   SLICE_X2Y7
                      net (fo=1, routed)
                                               0.577 6.253 divide/n_0_counter_reg[2]
   SLICE X2Y7
                      CARRY4 (Prop_carry4_S[1]_CO[3])
                                                0.657
                                                      6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                      net (fo=1, routed)
                                                0.000
                                                         6.910
                                                                 divide/n_0_counter_reg[5]_i_2
                      CARRY4 (Prop_carry4_CI_CO[3])
   SLICE_X2Y8
                                                0.117
                                                         7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                      net (fo=1, routed)
                                                0.000
                                                         7.027
                                                                 divide/n_0_counter_reg[9]_i_2
   SLICE_X2Y9
                      CARRY4 (Prop_carry4_CI_CO[3])
                                                0.117
                                                         7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                      net (fo=1, routed)
                                                0.000
                                                         7.144
                                                                 divide/n_0_counter_reg[13]_i_2
   SLICE_X2Y10
                      CARRY4 (Prop_carry4_CI_0[1])
                                                0.323
                                                         7.467 r
divide/counter_reg[14]_i_2_CARRY4/0[1]
                                                0.000
                      net (fo=1, routed)
                                                         7.467
                                                                 divide/n_0_counter_reg[14]_i_1
   SLICE_X2Y10
                      FDRE
                                                             r divide/counter_reg[14]/D
  _____
                                                                 _____
                      (clock sys_clk_pin rise edge)
                                               10.000
                                                        10.000 r
   W5
                                                0.000
                                                        10.000 r clk100Mhz
                                                0.000
                      net (fo=0)
                                                        10.000 clk100Mhz
   W5
                      IBUF (Prop_ibuf_I_0)
                                               1.388
                                                        11.388 r clk100Mhz_IBUF_inst/0
                      net (fo=1, routed)
                                               1.862 13.250 clk100Mhz IBUF
   BUFGCTRL X0Y0
                      BUFG (Prop bufg I 0)
                                              0.091 13.341 r clk100Mhz IBUF BUFG inst/0
                      net (fo=25, routed)
                                              1.517 14.858 divide/clk
   SLICE_X2Y10
                                                          r divide/counter_reg[14]/C
                                               0.274
                      clock pessimism
                                                        15.132
                      clock uncertainty
                                               -0.035
                                                        15.097
```

```
divide/counter_reg[14]
   SLICE_X2Y10
  ______
                     required time
                     arrival time
                                                       -7.467
  ______
                     slack
                                                        7.738
Slack (MET) :
                      7.747ns (required time - arrival time)
 Source:
                      divide/counter_reg[2]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                      divide/counter_reg[16]/D
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group: sys_clk_pin
 Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 2.300ns (logic 1.723ns (74.907%) route 0.577ns (25.093%))

Logic Levels: 4 (CARPYA-4)
 Logic Levels: 4 (CARRY4=4)
Clock Path Skew: -0.026ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 4.858ns = ( 14.858 - 10.000 )
   Source Clock Delay (SCD): 5.158ns
   Clock Pessimism Removal (CPR): 0.274ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
   Phase Error
                        (PE): 0.000ns
                   Delay type Incr(ns) Path(ns) Netlist Resource(s)
                      (clock sys_clk_pin rise edge)
                                               0.000
                                                       0.000 r
                                                     0.000 r clk100Mhz
   W5
                                               0.000
                     net (fo=0)
                                             0.000 0.000 clk100Mhz
   W5
                     IBUF (Prop_ibuf_I_0)
                                            1.458 1.458 r clk100Mhz_IBUF_inst/0
                     net (fo=1, routed)
                                             1.967 3.425 clk100Mhz_IBUF
   BUFGCTRL X0Y0
                                             0.096 3.521 r clk100Mhz IBUF BUFG inst/0
                     BUFG (Prop bufg I 0)
                     net (fo=25, routed)
                                             1.637 5.158 divide/clk
                                                        r divide/counter_reg[2]/C
   SLICE_X2Y7
  -----
                                                                -----
                     SLICE X2Y7
                     net (fo=1, routed)
                                             0.577 6.253 divide/n_0_counter_reg[2]
   SLICE_X2Y7
                     CARRY4 (Prop_carry4_S[1]_CO[3])
                                               0.657 6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                               0.000
                                                       6.910 divide/n_0_counter_reg[5]_i_2
   SLICE_X2Y8
                     CARRY4 (Prop_carry4_CI_CO[3])
                                               0.117
                                                       7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                               0.000
                                                        7.027
                                                                divide/n_0_counter_reg[9]_i_2
   SLICE X2Y9
                     CARRY4 (Prop_carry4_CI_CO[3])
                                               0.117
                                                       7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                     net (fo=1, routed)
                                               0.000
                                                       7.144
                                                                divide/n_0_counter_reg[13]_i_2
   SLICE X2Y10
                     CARRY4 (Prop_carry4_CI_0[3])
                                               0.314
                                                       7.458 r
```

```
divide/counter_reg[14]_i_2_CARRY4/0[3]
```

SLICE_X2Y10	net (fo=1, routed) FDRE	0.000		r	<pre>divide/n_0_counter_reg[16]_i_1 divide/counter_reg[16]/D</pre>
	(clock sys_clk_pin rise	edge)			
		10.000	10.000	r	
W5		0.000	10.000	r	clk100Mhz
	net (fo=0)	0.000	10.000		clk100Mhz
W5	<pre>IBUF (Prop_ibuf_I_0)</pre>	1.388	11.388	r	clk100Mhz_IBUF_inst/0
	net (fo=1, routed)	1.862	13.250		clk100Mhz_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.091	13.341	r	clk100Mhz_IBUF_BUFG_inst/O
	net (fo=25, routed)	1.517	14.858		divide/clk
SLICE_X2Y10				r	divide/counter_reg[16]/C
	clock pessimism	0.274	15.132		
	clock uncertainty	-0.035	15.097		
SLICE_X2Y10	<pre>FDRE (Setup_fdre_C_D)</pre>	0.109	15.206		<pre>divide/counter_reg[16]</pre>
	required time		15.206		
	arrival time		-7.458		
	slack		7.747		

Min Delay Paths

Slack (MET): 0.254ns (arrival time - required time)

divide/counter_reg[11]/C

(rising edge-triggered cell FDRE clocked by sys_clk_pin $\{ rise @ 0.000 ns \}$

fall@5.000ns period=10.000ns})

Destination: divide/counter_reg[11]/D

(rising edge-triggered cell FDRE clocked by sys_clk_pin $\{ rise @ 0.000 ns \}$

fall@5.000ns period=10.000ns})

Path Group: sys_clk_pin

Path Type: Hold (Min at Fast Process Corner)

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 0.388ns (logic 0.274ns (70.550%) route 0.114ns (29.450%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.992ns Source Clock Delay (SCD): 1.477ns

Clock Pessimism Removal (CPR): 0.515ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)	
	clock sys_clk_pin rise	edge)			
		0.000	0.000 r		
W5		0.000	0.000 r	clk100Mhz	
	net (fo=0)	0.000	0.000	clk100Mhz	
W5	<pre>IBUF (Prop_ibuf_I_0)</pre>	0.226	0.226 r	clk100Mhz_IBUF_inst/0	
	net (fo=1, routed)	0.631	0.858	clk100Mhz_IBUF	
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_0)	0.026	0.884 r	clk100Mhz_IBUF_BUFG_inst/O	
	net (fo=25, routed)	0.594	1.477	divide/clk	
SLICE_X2Y9			r	divide/counter_reg[11]/C	

```
SLICE_X2Y9
                  FDRE (Prop_fdre_C_Q)
   SLICE X2Y9
                     CARRY4 (Prop_carry4_S[2]_0[2])
                                             0.110 1.866 r
divide/counter_reg[10]_i_2_CARRY4/0[2]
                     net (fo=1, routed) 0.000 1.866 divide/n 0 counter reg[11] i 1
   SLICE X2Y9
                    FDRE
                                                       r divide/counter_reg[11]/D
                     (clock sys clk pin rise edge)
                                              0.000
                                                      0.000 r
                                             0.000 0.000 r clk100Mhz
   W5
                     net (fo=0)
                                            0.000 0.000 clk100Mhz
                     BUFGCTRL_X0Y0
                                                       r divide/counter_reg[11]/C
   SLICE X2Y9

        clock pessimism
        -0.515
        1.477

        FDRE (Hold_fdre_C_D)
        0.134
        1.611

   SLICE_X2Y9
                                            0.134 1.611
                                                              divide/counter_reg[11]
                     required time
                                                      -1.611
                     arrival time
                                                      1.866
                                                       0.254
Slack (MET) :
                    0.254ns (arrival time - required time)
 Source:
                     divide/counter reg[15]/C
                       (rising edge-triggered cell FDRE clocked by sys clk pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                      divide/counter_reg[15]/D
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
              sys_clk_pin
                 Hold (Min at Fast Process Corner)
0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
 Path Type:
 Requirement:
 Data Path Delay: 0.388ns (logic 0.274ns (70.550%) route 0.114ns (29.450%))
Logic Levels: 1 (CARRY4=1)
Clock Path Skew: 0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD): 1.991ns
   Source Clock Delay (SCD):
                               1.476ns
   Clock Pessimism Removal (CPR): 0.515ns
                   Delay type Incr(ns) Path(ns) Netlist Resource(s)
                     (clock sys_clk_pin rise edge)
                                              0.000
                                                     0.000 r
   W5
                                              0.000
                                                      0.000 r clk100Mhz
                     net (fo=0)
                                             0.000 0.000 clk100Mhz
   W5
                     IBUF (Prop_ibuf_I_0)
                                            net (fo=1, routed)
                                            0.631 0.858 clk100Mhz_IBUF
   BUFGCTRL X0Y0
                     BUFG (Prop bufg I 0)
                                            0.026 0.884 r clk100Mhz IBUF BUFG inst/0
                                            0.593 1.476 divide/clk
                     net (fo=25, routed)
   SLICE_X2Y10
                                                       r divide/counter_reg[15]/C
 _____
                                                              -----
   SLICE X2Y10
                     FDRE (Prop fdre C Q)
                                            0.164 1.640 r divide/counter reg[15]/Q
```

```
SLICE_X2Y10
                        CARRY4 (Prop_carry4_S[2]_0[2])
                                                      0.110 1.865 r
divide/counter_reg[14]_i_2_CARRY4/0[2]
                        net (fo=1, routed) 0.000
                                                                1.865
                                                                         divide/n_0_counter_reg[15]_i_1
   SLICE X2Y10
                        FDRE
                                                                r divide/counter_reg[15]/D
                         (clock sys_clk_pin rise edge)
                                                      0.000
                                                               0.000 r
                                                      0.000
                                                               0.000 r clk100Mhz
                        net (fo=0)
                                                    0.000 0.000 clk100Mhz

      IBUF (Prop_ibuf_I_0)
      0.414
      0.414 r clk100Mhz_IBUF_inst/0

      net (fo=1, routed)
      0.685
      1.099 clk100Mhz_IBUF

      BUFG (Prop_bufg_I_0)
      0.029
      1.128 r clk100Mhz_IBUF_BUFG_inst/0

      net (fo=25, routed)
      0.864
      1.991 divide/clk

   W5
   BUFGCTRL X0Y0
                                                                r divide/counter_reg[15]/C
   SLICE_X2Y10

        clock pessimism
        -0.515
        1.476

        FDRE (Hold_fdre_C_D)
        0.134
        1.610

   SLICE X2Y10
                                                              1.610 divide/counter_reg[15]
  _____
                        required time
                                                               -1.610
                        arrival time
                                                                0.254
                        slack
Slack (MET) :
                         0.254ns (arrival time - required time)
 Source:
                         divide/counter reg[19]/C
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                         divide/counter reg[19]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group: sys_clk_pin
Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay: 0.388ns (logic 0.274ns (70.550%) route 0.114ns (29.450%))
Logic Levels: 1 (CARRY4=1)
Clock Path Skew: 0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD): 1.991ns
   Source Clock Delay (SCD):
                                    1.476ns
   Clock Pessimism Removal (CPR): 0.515ns
   Location
                      Delay type
                                                Incr(ns) Path(ns) Netlist Resource(s)
  _____
                                                                        _____
                        (clock sys_clk_pin rise edge)
                                                      0.000 0.000 r
                                                      0.000 0.000 r clk100Mhz
   W5
                                                     0.000 0.000 clk100Mhz
                         net (fo=0)
                                                  0.226 0.226 r clk100Mhz_IBUF_inst/0
                        IBUF (Prop ibuf I 0)
                                                    0.631 0.858 clk100Mhz_IBUF
                        net (fo=1, routed)
   BUFGCTRL_X0Y0
                        BUFG (Prop_bufg_I_0)
                                                   0.026 0.884 r clk100Mhz_IBUF_BUFG_inst/0
                        net (fo=25, routed)
                                                   0.593 1.476 divide/clk
   SLICE X2Y11
                                                               r divide/counter_reg[19]/C
  _____
                                                                         -----
                       SLICE_X2Y11
                        CARRY4 (Prop_carry4_S[2]_0[2])
   SLICE X2Y11
```

```
0.110 1.865 r
divide/counter_reg[18]_i_2_CARRY4/0[2]
                     net (fo=1, routed)
                                              0.000
                                                      1.865 divide/n_0_counter_reg[19]_i_1
   SLICE_X2Y11
                    FDRE
                                                       r divide/counter reg[19]/D
 -----
                     (clock sys clk pin rise edge)
                                              0.000
                                                   0.000 r
   W5
                                             0.000 0.000 r clk100Mhz
                                                    0.000 clk100Mhz
                     net (fo=0)
                                             0.000
                    BUFGCTRL_X0Y0
   SLICE X2Y11
                                                      r divide/counter_reg[19]/C

      clock pessimism
      -0.515
      1.476

      FDRE (Hold_fdre_C_D)
      0.134
      1.610

   SLICE_X2Y11
                                                              divide/counter_reg[19]
 _____
                     required time
                                                     -1.610
                     arrival time
 ______
                     slack
                                                      0.254
                     0.254ns (arrival time - required time)
Slack (MET) :
 Source:
                     divide/counter_reg[23]/C
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                      divide/counter_reg[23]/D
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group: sys_clk_pin
 Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 0.388ns (logic 0.274ns (70.550%) route 0.114ns (29.450%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD): 1.989ns
   Source Clock Delay (SCD): 1.475ns
   Clock Pessimism Removal (CPR): 0.514ns
                                         Incr(ns) Path(ns) Netlist Resource(s)
   Location
                   Delay type
                     (clock sys_clk_pin rise edge)
                                             0.000 0.000 r
   W5
                                             0.000 0.000 r clk100Mhz
                                            0.000 0.000 clk100Mhz
                     net (fo=0)
                                         0.226 0.226 r clk100Mhz_IBUF_inst/0
   W5
                     IBUF (Prop_ibuf_I_0)
                                           0.631 0.858 clk100Mhz_IBUF
                     net (fo=1, routed)
                     BUFGCTRL X0Y0
   SLICE X2Y12
                                                       r divide/counter_reg[23]/C
 FDRE (Prop_fdre_C_Q)
net (fo=1, routed)
   SLICE X2Y12
                                           0.164 1.639 r divide/counter reg[23]/Q
                                           0.114 1.754 divide/n_0_counter_reg[23]
                    CARRY4 (Prop_carry4_S[2]_0[2])
   SLICE_X2Y12
                                             0.110 1.864 r
divide/counter_reg[22]_i_2_CARRY4/0[2]
```

```
net (fo=1, routed) 0.000 1.864 divide/n_0_counter_reg[23]_i_1
   SLICE_X2Y12
                    FDRE
                                                   r divide/counter_reg[23]/D
  -----
                                                          -----
                    (clock sys_clk_pin rise edge)
                                           0.000 0.000 r
   W5
                                           0.000 0.000 r clk100Mhz
                    net (fo=0)
                                          0.000 0.000 clk100Mhz
                   W5
   BUFGCTRL X0Y0
                                                   r divide/counter_reg[23]/C
   SLICE X2Y12
                    clock pessimism
                                         -0.514 1.475
                   FDRE (Hold_fdre_C_D) 0.134 1.609 divide/counter_reg[23]
   SLICE X2Y12
                    required time
                                                   -1.609
                    arrival time
                    slack
                                                   0.254
Slack (MET) :
                     0.254ns (arrival time - required time)
 Source:
                    divide/counter_reg[3]/C
                      (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                    divide/counter_reg[3]/D
                      (rising edge-triggered cell FDRE clocked by sys clk pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group: sys_clk_pin
 Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 0.388ns (logic 0.274ns (70.550%) route 0.114ns (29.450%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD): 1.992ns
   Source Clock Delay (SCD): 1.477ns
  Clock Pessimism Removal (CPR): 0.515ns
                                       Incr(ns) Path(ns) Netlist Resource(s)
  Location
                   Delay type
 ______
                                                          _____
                    (clock sys_clk_pin rise edge)
                                           0.000
                                                 0.000 r
                                           0.000 0.000 r clk100Mhz
   W5
                                          0.000 0.000 clk100Mhz
                    net (fo=0)
                BUFGCTRL_X0Y0
   SLICE X2Y7
                                                    r divide/counter_reg[3]/C
 ------
                   FDRE (Prop_fdre_C_Q)
net (fo=1, routed)
                                         0.164 1.641 r divide/counter_reg[3]/Q
   SLICE_X2Y7
                                          0.114  1.756  divide/n_0_counter_reg[3]
                  CARRY4 (Prop_carry4_S[2]_0[2])
   SLICE X2Y7
                                           0.110
                                                  1.866 r
divide/counter_reg[2]_i_2_CARRY4/0[2]
                   net (fo=1, routed) 0.000 1.866
                                                           divide/n_0_counter_reg[3]_i_1
   SLICE X2Y7
                    FDRE
                                                        r divide/counter_reg[3]/D
```

------(clock sys_clk_pin rise edge) 0.000 0.000 r 0.000 0.000 r clk100Mhz W5 net (fo=0) 0.000 0.000 clk100Mhz 0.414 0.414 r clk100Mhz_IBUF_inst/0 0.685 1.099 clk100Mhz_IBUF W5 IBUF (Prop ibuf I O) net (fo=1, routed) BUFGCTRL_X0Y0 SLICE X2Y7 r divide/counter reg[3]/C clock pessimism -0.515 1.477 FDRE (Hold_fdre_C_D) 0.134 SLICE X2Y7 1.611 divide/counter_reg[3] ______ required time -1.611 arrival time 0.254 Slack (MET) : 0.254ns (arrival time - required time) Source: divide/counter_reg[7]/C (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns}) Destination: divide/counter_reg[7]/D (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns}) Path Group: sys_clk_pin Hold (Min at Fast Process Corner) Path Type: Requirement: Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 0.388ns (logic 0.274ns (70.550%) route 0.114ns (29.450%)) 1 (CARRY4=1) Logic Levels: Clock Path Skew: 0.000ns (DCD - SCD - CPR) Destination Clock Delay (DCD): 1.992ns Source Clock Delay (SCD): 1.477ns Clock Pessimism Removal (CPR): 0.515ns Incr(ns) Path(ns) Netlist Resource(s) Delay type ------(clock sys_clk_pin rise edge) 0.000 0.000 r W5 0.000 0.000 r clk100Mhz net (fo=0) 0.000 0.000 clk100Mhz W5 BUFGCTRL_X0Y0 r divide/counter_reg[7]/C SLICE_X2Y8 -----FDRE (Prop_fdre_C_Q)
net (fo=1, routed) 0.164 1.641 r divide/counter_reg[7]/Q SLICE X2Y8 0.114 1.756 divide/n_0_counter_reg[7] CARRY4 (Prop_carry4_S[2]_0[2]) SLICE X2Y8 0.110 1.866 r divide/counter_reg[6]_i_2_CARRY4/0[2] net (fo=1, routed) 0.000 1.866 divide/n_0_counter_reg[7]_i_1 FDRE r divide/counter_reg[7]/D SLICE_X2Y8 _____

```
(clock sys_clk_pin rise edge)
                                           0.000
                                                0.000 r
                                                0.000 r clk100Mhz
   W5
                                           0.000
                                          0.000 0.000 clk100Mhz
                   net (fo=0)
                   IBUF (Prop_ibuf_I_0)
   W5
                                        0.414 0.414 r clk100Mhz_IBUF_inst/0
                   net (fo=1, routed)
                                         0.685 1.099 clk100Mhz_IBUF
   BUFGCTRL X0Y0
                   BUFG (Prop bufg I 0)
                                         0.029 1.128 r clk100Mhz IBUF BUFG inst/0
                                         0.865 1.992 divide/clk
                   net (fo=25, routed)
   SLICE_X2Y8
                                                    r divide/counter_reg[7]/C
                                         -0.515 1.477
                   clock pessimism
                                         0.134
                   FDRE (Hold_fdre_C_D)
                                                  1.611
   SLICE X2Y8
                                                        divide/counter reg[7]
 ______
                   required time
                                                  -1.611
                   arrival time
                                                   1.866
 ______
                   slack
                                                   0.254
Slack (MET) :
                    0.262ns (arrival time - required time)
 Source:
                    divide/counter_reg[0]/C
                      (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                    divide/counter_reg[0]/D
                      (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                    sys_clk_pin
                   Hold (Min at Fast Process Corner)
 Path Type:
                  0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
 Requirement:
 Data Path Delay:
                  0.353ns (logic 0.186ns (52.691%) route 0.167ns (47.309%))
 Logic Levels:
                   1 (LUT1=1)
 Clock Path Skew: 0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD): 1.992ns
   Source Clock Delay (SCD): 1.477ns
   Clock Pessimism Removal (CPR): 0.515ns
   Location
                  Delay type
                                       Incr(ns) Path(ns) Netlist Resource(s)
 (clock sys_clk_pin rise edge)
                                           0.000
                                                0.000 r
                                          0.000 0.000 r clk100Mhz
   W5
                                          0.000 0.000 clk100Mhz
                   net (fo=0)
                                        0.226
                                                0.226 r clk100Mhz_IBUF_inst/0
   W5
                   IBUF (Prop_ibuf_I_0)
                   BUFGCTRL_X0Y0
   SLICE_X3Y7
                                                    r divide/counter_reg[0]/C
                   FDRE (Prop_fdre_C_Q) 0.141 1.618 f divide/counter_reg[0]/Q
   SLICE_X3Y7
                   net (fo=2, routed) 0.167 1.785 divide/n_0_counter_reg[0] LUT1 (Prop_lut1_I0_0) 0.045 1.830 r divide/counter[0]_i_1/0 net (fo=1, routed) 0.000 1.830 divide/n_0_counter[0]_i_1
   SLICE X3Y7
   SLICE X3Y7
                   FDRE
                                                    r divide/counter_reg[0]/D
 -----
                                                         -----
                    (clock sys_clk_pin rise edge)
                                           0.000
                                                   0.000 r
   W5
                                           0.000
                                                   0.000 r clk100Mhz
                    net (fo=0)
                                           0.000
                                                   0.000 clk100Mhz
```

```
W5
   BUFGCTRL_X0Y0
   SLICE X3Y7
                                                  r divide/counter_reg[0]/C
                   clock pessimism
                                       -0.515 1.477
  SLICE X3Y7
                   FDRE (Hold_fdre_C_D)
                                        0.091 1.568 divide/counter reg[0]
 ______
                   required time
                                                -1.568
                   arrival time
                                                 1.830
                   slack
Slack (MET) :
                   0.279ns (arrival time - required time)
 Source:
                    divide/counter reg[0]/C
                     (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                    divide/counter_reg[1]/D
                     (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:
                   sys_clk_pin
 Path Type:
                  Hold (Min at Fast Process Corner)
               0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
 Requirement:
 Data Path Delay: 0.426ns (logic 0.299ns (70.143%) route 0.127ns (29.857%))
Logic Levels: 1 (CARRY4=1)
                  0.013ns (DCD - SCD - CPR)
 Clock Path Skew:
  Destination Clock Delay (DCD): 1.992ns
   Source Clock Delay (SCD): 1.477ns
  Clock Pessimism Removal (CPR): 0.502ns
  Location
                  Delay type
                                      Incr(ns) Path(ns) Netlist Resource(s)
 ------
                   (clock sys_clk_pin rise edge)
                                          0.000
                                                0.000 r
  W5
                                         0.000 0.000 r clk100Mhz
                   net (fo=0)
                                        0.000 0.000 clk100Mhz
                                       W5
                   IBUF (Prop_ibuf_I_0)
                   net (fo=1, routed)
                   net (TO-1, 10000)

BUFG (Prop_bufg_I_O)

0.026

0.004

1.477

divide/clk

divide/cour
   BUFGCTRL_X0Y0
                                       0.026 0.884 r clk100Mhz_IBUF_BUFG_inst/0
                                                  r divide/counter_reg[0]/C
   SLICE_X3Y7
                   FDRE (Prop_fdre_C_Q) 0.141 1.618 r divide/counter_reg[0]/Q net (fo=2, routed) 0.127 1.745 divide/n_0_counter_reg[0]
   SLICE_X3Y7
                                        0.127 1.745 divide/n_0_counter_reg[0]
   SLICE_X2Y7
              CARRY4 (Prop_carry4_CYINIT_0[0])
                                         0.158 1.903 r
divide/counter_reg[2]_i_2_CARRY4/0[0]
                  net (fo=1, routed) 0.000 1.903 divide/n_0_counter_reg[1]_i_1
   SLICE X2Y7
                  FDRE
                                                 r divide/counter reg[1]/D
 _____
                   (clock sys_clk_pin rise edge)
                                          0.000 0.000 r
   W5
                                         0.000 0.000 r clk100Mhz
                                         0.000 0.000 clk100Mhz
                   net (fo=0)
                   W5
```

```
BUFGCTRL_X0Y0
     SLICE_X2Y7
                                                                                     r divide/counter_reg[1]/C
                                                                    -0.502
                                 clock pessimism
                                                                                    1.490
                                FDRE (Hold_fdre_C_D)
                                                                     0.134
     SLICE X2Y7
                                                                                                 divide/counter_reg[1]
                                                                                    1.624
   -----
                                required time
                                                                                   -1.624
                                 arrival time
                                                                                    1.903
   ______
                                 slack
                                                                                     0.279
Slack (MET) :
                                  0.290ns (arrival time - required time)
  Source:
                                  divide/counter_reg[11]/C
                                    (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:
                                  divide/counter_reg[12]/D
                                     (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
 Path Group: sys_clk_pin
Path Type: Hold (Min at Fast Process Corner)
Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay: 0.424ns (logic 0.310ns (73.048%) route 0.114ns (26.952%))
Logic Levels: 1 (CARRY4=1)
Clock Path Skew: 0.000ns (DCD - SCD - CPR)
fall@5.000ns period=10.000ns})
     Destination Clock Delay (DCD): 1.992ns
                                                1.477ns
     Source Clock Delay (SCD):
    Clock Pessimism Removal (CPR): 0.515ns
    Location
                               Delay type
                                                                 Incr(ns) Path(ns) Netlist Resource(s)
                                 (clock sys_clk_pin rise edge)
                                                                        0.000
                                                                                 0.000 r
     W5
                                                                        0.000
                                                                                 0.000 r clk100Mhz
                                                                                    0.000 clk100Mhz
                                                                     0.000
                                 net (fo=0)

      net (f0=0)
      0.000
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     W5
     BUFGCTRL X0Y0
                                                                                          r divide/counter_reg[11]/C
     SLICE_X2Y9
                                                                                                 _____
   _____
                                SLICE_X2Y9
     SLICE_X2Y9
                              CARRY4 (Prop_carry4_S[2]_0[3])
                                                                       0.146 1.902 r
divide/counter_reg[10]_i_2_CARRY4/0[3]
                               net (fo=1, routed) 0.000 1.902 divide/n_0_counter_reg[12]_i_1
     SLICE_X2Y9
                              FDRE
                                                                                     r divide/counter_reg[12]/D
                                                                                                 -----
                                 (clock sys clk pin rise edge)
                                                                                 0.000 r
                                                                        0.000
     W5
                                                                        0.000 0.000 r clk100Mhz
                                 net (fo=0)
                                                                     0.000 0.000 clk100Mhz
                                                                    0.414 0.414 r clk100Mhz_IBUF_inst/0
     W5
                                 IBUF (Prop_ibuf_I_0)
                                                                    0.685 1.099 clk100Mhz_IBUF
                                 net (fo=1, routed)
                                 BUFGCTRL_X0Y0
```

```
SLICE_X2Y9
                                                                        r divide/counter_reg[12]/C
                         clock pessimism
                                                     -0.515 1.477
                         FDRE (Hold_fdre_C_D) 0.134 1.611
    SLICE_X2Y9
                                                                           divide/counter_reg[12]
  ______
                         required time
                                                                -1.611
                         arrival time
                                                                 1.902
                         slack
                                                                 0.290
Slack (MET) :
                          0.290ns (arrival time - required time)
 Source:
                          divide/counter reg[3]/C
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:
                          divide/counter_reg[4]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group: sys_clk_pin
Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay: 0.424ns (logic 0.310ns (73.048%) route 0.114ns (26.952%))
Logic Levels: 1 (CARRY4=1)
Clock Path Skew: 0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD): 1.992ns
    Source Clock Delay (SCD): 1.477ns
   Clock Pessimism Removal (CPR): 0.515ns
   Location
                       Delay type
                                                  Incr(ns) Path(ns) Netlist Resource(s)
  _____
                                                                         -----
                         (clock sys_clk_pin rise edge)
                                                       0.000 0.000 r
                                                      0.000 0.000 r clk100Mhz
    W5
                                                     0.000 0.000 clk100Mhz
                         net (fo=0)
                         net (fo=0) 0.000 0.000 clk100Mhz

IBUF (Prop_ibuf_I_0) 0.226 0.226 r clk100Mhz_IBUF_inst/0

net (fo=1, routed) 0.631 0.858 clk100Mhz_IBUF

BUFG (Prop_bufg_I_0) 0.026 0.884 r clk100Mhz_IBUF_BUFG_inst/0

net (fo=25, routed) 0.594 1.477 divide/clk
    BUFGCTRL X0Y0
    SLICE X2Y7
                                                                   r divide/counter_reg[3]/C
                                                                          -----
                       FDRE (Prop_fdre_C_Q) 0.164 1.641 r divide/counter_reg[3]/Q net (fo=1, routed) 0.114 1.756 divide/n_0_counter_reg[3]
    SLICE_X2Y7
    SLICE X2Y7
                        CARRY4 (Prop_carry4_S[2]_0[3])
                                                      0.146
                                                                1.902 r
divide/counter_reg[2]_i_2_CARRY4/0[3]
                        net (fo=1, routed) 0.000
                                                              1.902
                                                                           divide/n_0_counter_reg[4]_i_1
    SLICE_X2Y7
                                                                  r divide/counter_reg[4]/D
                         (clock sys_clk_pin rise edge)
                                                       0.000
                                                               0.000 r
    W5
                                                       0.000 0.000 r clk100Mhz
                         net (fo=0)
                                                     0.000 0.000 clk100Mhz
                                                    0.414 0.414 r clk100Mhz_IBUF_inst/0
    W5
                         IBUF (Prop_ibuf_I_0)
                         net (fo=1, routed)
                                                    0.685 1.099 clk100Mhz IBUF
                                                    0.029 1.128 r clk100Mhz_IBUF_BUFG_inst/0
    BUFGCTRL_X0Y0
                         BUFG (Prop_bufg_I_0)
                                                    0.865 1.992 divide/clk
                         net (fo=25, routed)
    SLICE_X2Y7
                                                                 r divide/counter_reg[4]/C
                         clock pessimism
                                                    -0.515
                                                              1.477
```

SLICE_X2Y7	FDRE (Hold_fdre_C_D)	0.134	1.611	divide/counter_reg[4]
	required time arrival time		-1.611 1.902	
	slack		0.290	

Pulse Width Checks

Clock Name: sys_clk_pin
Waveform: { 0 5 }
Period: 10.000
Sources: { clk100Mhz }

Check Type	Corner	Lib Pin	Reference Pin	Required	Actual	Slack	Location	Pin
Min Period	n/a	BUFG/I	n/a	2.155	10.000	7.845	BUFGCTRL_X0Y0	
clk100Mhz_IBUF_BU	FG_inst/	I						
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X3Y7	
divide/counter_re	g[0]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y9	
divide/counter_re	g[10]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y9	
divide/counter_re	g[11]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y9	
divide/counter_re	g[12]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y10	
divide/counter_re	g[13]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y10	
divide/counter_re	g[14]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y10	
divide/counter_re	g[15]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y10	
divide/counter_re	g[16]/C							
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X2Y11	
divide/counter_re	g[17]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X3Y7	
divide/counter_re	g[0]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9	
divide/counter_re	g[10]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9	
divide/counter_re	g[11]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9	
divide/counter_re	g[12]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10	
divide/counter_re	g[13]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10	
divide/counter_re	g[14]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10	
divide/counter_re	g[15]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10	
divide/counter_re	g[16]/C							
Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y11	
divide/counter_re	g[17]/C							

Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y11
divide/counter_re	g[18]/C						
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X3Y7
divide/counter_re	g[0]/C						
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9
divide/counter_re	g[10]/C						
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9
divide/counter_re	g[11]/C						
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9
divide/counter_re	g[12]/C						
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10
divide/counter_re	g[13]/C						
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10
divide/counter_re	g[14]/C						
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10
divide/counter_re	g[15]/C						
High Pulse Width		FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10
divide/counter_re							
High Pulse Width		FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y7
divide/counter_re							
High Pulse Width		FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y7
divide/counter_re	g[2]/C						