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| Tool Version : Vivado v.2014.4 (win64) Build 1071353 Tue Nov 18 18:29:27 MST 2014
| Date : Tue Feb 24 20:50:14 2015
| Host : ECJ1-222-04 running 64-bit Service Pack 1 (build 7601)
| Command : report_utilization -file top_utilization_placed.rpt -pb top_utilization_placed.pb
| Design : top
| Device : xc7a35t
| Design State : Fully Placed

Utilization Design Information

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1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	21	0	20800	0.10
LUT as Logic	21	0	20800	0.10
LUT as Memory	0	0	9600	0.00
Slice Registers	34	0	41600	0.08
Register as Flip Flop	34	0	41600	0.08
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
6	Yes	-	Set
3	Yes	-	Reset
0	Yes	Set	-
25	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	13	0	8150	0.15
SLICEL	7	0		
SLICEM	6	0		
LUT as Logic	21	0	20800	0.10
using O5 output only	0			
using O6 output only	12			
using O5 and O6	9			
LUT as Memory	0	0	9600	0.00
LUT as Distributed RAM	0	0		
LUT as Shift Register	0	0		
LUT Flip Flop Pairs	45	0	20800	0.21
fully used LUT-FF pairs	9			
LUT-FF pairs with unused LUT	24			
LUT-FF pairs with unused Flip Flop	12			
Unique Control Sets	4			
Minimum number of registers lost to control set restriction	22(Lost)			

3. Memory

+----------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00
+----------------+------+-------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. DSP

+-----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------+------+-------+-----------+-------+
| DSPs | 0 | 0 | 90 | 0.00 |
+-----------+------+-------+-----------+-------+

5. IO and GT Specific

+----------------------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+----------------------------+------+-------+-----------+-------+
Bonded IOB	10	10	106	9.43
IOB Master Pads	4			
IOB Slave Pads	5			
Bonded IPADs	0	0	10	0.00
Bonded OPADs	0	0	4	0.00
PHY_CONTROL	0	0	5	0.00
PHASER_REF	0	0	5	0.00
OUT_FIFO	0	0	20	0.00
IN_FIFO	0	0	20	0.00
IDELAYCTRL	0	0	5	0.00

IBUFGDS	0	0	104	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00
IBUFDS_GTE2	0	0	2	0.00
ILOGIC	0	0	106	0.00
OLOGIC	0	0	106	0.00
+----------+------+-------+-----------+-------+

6. Clocking

+----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+----------+------+-------+-----------+-------+
BUFGCTRL	1	0	32	3.12
BUFIO	0	0	20	0.00
MMCME2_ADV	0	0	5	0.00
PLLE2_ADV	0	0	5	0.00
BUFMRCE	0	0	10	0.00
BUFHCE	0	0	72	0.00
BUFR	0	0	20	0.00
+----------+------+-------+-----------+-------+

7. Specific Feature

+----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+----------+------+-------+-----------+-------+
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
PCIE_2_1	0	0	1	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00
+----------+------+-------+-----------+-------+

8. Primitives

Ref Name	Used	Functional Category
FDRE	25	Flop & Latch
LUT5	10	LUT
OBUF	8	IO
LUT4	8	LUT
LUT6	6	LUT
FDPE	6	Flop & Latch
CARRY4	6	CarryLogic
FDCE	3	Flop & Latch
LUT3	2	LUT
LUT2	2	LUT
LUT1	2	LUT
IBUF	2	IO
BUFG	1	Clock

9. Black Boxes

Ref Name	Used

10. Instantiated Netlists

Ref Name	Used