```
#-----------------------------------------------------------
# Vivado v2014.4 (64-bit)
# SW Build 1071353 on Tue Nov 18 18:29:27 MST 2014
# IP Build 1070531 on Tue Nov 18 01:10:18 MST 2014
# Start of session at: Tue Feb 24 20:45:59 2015
# Process ID: 1824
# Log file: C:/Users/gln276/project_1/project_1.runs/synth_1/top.vds
# Journal file: C:/Users/gln276/project_1/project_1.runs/synth_1\vivado.jou
#-----------------------------------------------------------
source top.tcl
# set_param gui.test TreeTableDev
# debug::add_scope template.lib 1
# set_msg_config -id {HDL 9-1061} -limit 100000
# set_msg_config -id {HDL 9-1654} -limit 100000
# create_project -in_memory -part xc7a35tcpg236-1
# set_param project.compositeFile.enableAutoGeneration 0
# set_param synth.vivado.isSynthRun true
# set_property webtalk.parent_dir C:/Users/gln276/project_1/project_1.cache/wt
[current_project]
# set_property parent.project_path C:/Users/gln276/project_1/project_1.xpr [current_project]
# set_property default_lib xil_defaultlib [current_project]
# set_property target_language Verilog [current_project]
# read_verilog -library xil_defaultlib
C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v
# read_xdc C:/Users/gln276/project_1/project_1.srcs/constrs_1/new/trafficContConst.xdc
# set_property used_in_implementation false [get_files
C:/Users/gln276/project_1/project_1.srcs/constrs_1/new/trafficContConst.xdc]
# catch { write_hwdef -file top.hwdef }
INFO: [Vivado_Tcl 4-279] hardware handoff file cannot be generated as there is no block
diagram instance in the design
# synth_design -top top -part xc7a35tcpg236-1
Command: synth_design -top top -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB):
peak = 239.148 ; gain = 80.613
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'top'
[C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:371]
INFO: [Synth 8-638] synthesizing module 'divider'
[C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:348]
```

```
INFO: [Synth 8-256] done synthesizing module 'divider' (1#1)
[C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:348]
INFO: [Synth 8-638] synthesizing module 'traffic_controller'
[C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:12]
WARNING: [Synth 8-567] referenced signal 'RST' should be on the sensitivity list
[C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:82]
INFO: [Synth 8-256] done synthesizing module 'traffic_controller' (2#1)
[C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:12]
INFO: [Synth 8-256] done synthesizing module 'top' (3#1)
[C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:371]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:09 ; elapsed = 00:00:11 . Memory (MB):
peak = 273.336 ; gain = 114.801
---------------------------------------------------------------------------------

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------------+
|      |Item             |Errors |Warnings |Status |Description      |
+------+-----------------+-------+---------+-------+-----------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+-----------------+
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:09 ; elapsed = 00:00:11 . Memory
(MB): peak = 273.336 ; gain = 114.801
---------------------------------------------------------------------------------
Loading clock regions from
C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/artix7/xc7a35t/ClockRegion.xml
Loading clock buffers from
C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/artix7/xc7a35t/ClockBuffers.xml
Loading clock placement rules from
C:/Xilinx/Vivado/2014.4/data/parts/xilinx/artix7/ClockPlacerRules.xml
Loading package pin functions from
C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/PinFunctions.xml...
Loading package from
C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/artix7/xc7a35t/cpg236/Package.xml
Loading io standards from C:/Xilinx/Vivado/2014.4/data\./parts/xilinx/artix7/IOStandards.xml
Loading device configuration modes from
C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/ConfigModes.xml
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File
```

[C:/Users/gln276/project_1/project_1.srcs/constrs_1/new/trafficContConst.xdc]
Finished Parsing XDC File
[C:/Users/gln276/project_1/project_1.srcs/constrs_1/new/trafficContConst.xdc]
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.005 . Memory (MB): peak = 562.352 ; gain = 0.000

Finished Constraint Validation : Time (s): cpu = 00:00:21 ; elapsed = 00:00:23 . Memory (MB): peak = 562.352 ; gain = 403.816

Start Loading Part and Timing Information

Loading part: xc7a35tcpg236-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:21 ; elapsed = 00:00:23 . Memory (MB): peak = 562.352 ; gain = 403.816

Start Applying 'set_property' XDC Constraints

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:21 ; elapsed = 00:00:23 . Memory (MB): peak = 562.352 ; gain = 403.816

INFO: [Synth 8-3537] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the inputs of the operator [C:/Users/gln276/project_1/project_1.srcs/sources_1/new/top.v:63]

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 562.352 ; gain = 403.816

Report RTL Partitions:
+-+-------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+-------------+-----------+----------+
+-+-------------+-----------+----------+

Start RTL Component Statistics

Detailed RTL Component Info :

+---Adders :

2 Input 4 Bit Adders := 1

+---Muxes :

2 Input 4 Bit Muxes := 9

3 Input 4 Bit Muxes := 2

16 Input 3 Bit Muxes := 2

2 Input 3 Bit Muxes := 1

16 Input 2 Bit Muxes := 1

2 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

Finished RTL Component Statistics

Start RTL Hierarchical Component Statistics

Hierarchical RTL Component report

Module top

Detailed RTL Component Info :

Module divider

Detailed RTL Component Info :

Module traffic_controller

Detailed RTL Component Info :

+---Adders :

2 Input 4 Bit Adders := 1

+---Muxes :

2 Input 4 Bit Muxes := 9

3 Input 4 Bit Muxes := 2

16 Input 3 Bit Muxes := 2

2 Input 3 Bit Muxes := 1

16 Input 2 Bit Muxes := 1

2 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

Finished RTL Hierarchical Component Statistics

Start Part Resource Summary

Part Resources:

DSPs: 120 (col length:60)
BRAMs: 150 (col length: RAMB18 60 RAMB36 30)

Finished Part Resource Summary

Start Parallel Synthesis Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 562.352 ; gain = 403.816

Start Cross Boundary Optimization

Finished Cross Boundary Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 562.352 ; gain = 403.816

Finished Parallel Reinference : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 562.352 ; gain = 403.816

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start RAM, DSP and Shift Register Reporting

Finished RAM, DSP and Shift Register Reporting

WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[25]) is unused and will be removed from module top.
WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[26]) is unused and will be removed from module top.
WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[27]) is unused and will be removed from module top.

Start Area Optimization

Finished Area Optimization : Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 562.352 ; gain = 403.816

Finished Area Optimization : Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB):

peak = 562.352 ; gain = 403.816

Finished Parallel Area Optimization : Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 562.352 ; gain = 403.816

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
Finished Parallel Synthesis Optimization : Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 562.352 ; gain = 403.816

Start Timing Optimization

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:40 ; elapsed = 00:00:43 . Memory (MB): peak = 562.352 ; gain = 403.816

WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[25]) is unused and will be removed from module top.
WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[26]) is unused and will be removed from module top.
WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[27]) is unused and will be removed from module top.
WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[25]) is unused and will be removed from module top.
WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[26]) is unused and will be removed from module top.
WARNING: [Synth 8-3332] Sequential element (\divide/counter_reg[27]) is unused and will be removed from module top.

Finished Timing Optimization : Time (s): cpu = 00:00:40 ; elapsed = 00:00:43 . Memory (MB): peak = 562.352 ; gain = 403.816

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+

```
+-+-------------+------------+----------+
--------------------------------------------------------------------------------
Start Technology Mapping
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:40 ; elapsed = 00:00:43 . Memory (MB):
peak = 562.352 ; gain = 403.816
--------------------------------------------------------------------------------

Report RTL Partitions:
+-+-------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+-------------+------------+----------+
+-+-------------+------------+----------+
--------------------------------------------------------------------------------
Start IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Start Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished Final Netlist Cleanup
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:40 ; elapsed = 00:00:43 . Memory (MB): peak =
562.352 ; gain = 403.816
--------------------------------------------------------------------------------

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------------+
|      |Item             |Errors |Warnings |Status |Description      |
+------+-----------------+-------+---------+-------+-----------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+-----------------+
--------------------------------------------------------------------------------
Start Renaming Generated Instances
--------------------------------------------------------------------------------
```

Finished Renaming Generated Instances : Time (s): cpu = 00:00:40 ; elapsed = 00:00:43 . Memory (MB): peak = 562.352 ; gain = 403.816

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:40 ; elapsed = 00:00:43 . Memory (MB): peak = 562.352 ; gain = 403.816

Start RAM, DSP and Shift Register Reporting

Finished RAM, DSP and Shift Register Reporting

Start Writing Synthesis Report

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+--------+------+
| |Cell |Count |
+------+--------+------+
1	BUFG	1
2	INV	1
3	LUT1	2
4	LUT2	2
5	LUT3	2
6	LUT4	8

```
|7     |LUT5    |    10|
|8     |LUT6    |     6|
|9     |MUXCY_L |    23|
|10    |XORCY   |    24|
|11    |FDCE    |     3|
|12    |FDPE    |     6|
|13    |FDRE    |    25|
|14    |IBUF    |     2|
|15    |OBUF    |     8|
+------+--------+------+

Report Instance Areas:
+------+----------+------------------+------+
|      |Instance  |Module            |Cells |
+------+----------+------------------+------+
|1     |top       |                  |   123|
|2     |  divide  |divider           |    73|
|3     |  traffic |traffic_controller |    39|
+------+----------+------------------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:40 ; elapsed = 00:00:43 . Memory
(MB): peak = 562.352 ; gain = 403.816
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 9 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:32 . Memory
(MB): peak = 562.352 ; gain = 84.887
Synthesis Optimization Complete : Time (s): cpu = 00:00:41 ; elapsed = 00:00:44 . Memory
(MB): peak = 562.352 ; gain = 403.816
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 49 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-140] Inserted 0 IBUFs to IO ports without IO buffers.
INFO: [Opt 31-141] Inserted 0 OBUFs to IO ports without IO buffers.
INFO: [Opt 31-138] Pushed 1 inverter(s) to 9 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 6 instances were transformed.
  (MUXCY,XORCY) => CARRY4: 6 instances

INFO: [Common 17-83] Releasing license: Synthesis
19 Infos, 10 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:39 ; elapsed = 00:00:42 . Memory (MB): peak = 562.352
```

; gain = 377.020
write_checkpoint -noxdef top.dcp
catch { report_utilization -file top_utilization_synth.rpt -pb top_utilization_synth.pb }
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.068 . Memory (MB): peak = 562.352 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Tue Feb 24 20:46:46 2015...