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| Tool Version      : Vivado v.2014.4 (win64) Build 1071353 Tue Nov 18 18:29:27 MST 2014
| Date              : Tue Feb 24 20:50:54 2015
| Host              : ECJ1-222-04 running 64-bit Service Pack 1  (build 7601)
| Command           : report_timing_summary -warn_on_violation -max_paths 10 -file
top_timing_summary_routed.rpt -rpx top_timing_summary_routed.rpx
| Design            : top
| Device            : 7a35t-cpg236
| Speed File        : -1  PRODUCTION 1.14 2014-09-11
| Temperature Grade : C
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Timing Summary Report

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| Timer Settings
| --------------
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  Enable Multi Corner Analysis               :  Yes
  Enable Pessimism Removal                   :  Yes
  Pessimism Removal Resolution               :  Nearest Common Node
  Enable Input Delay Default Clock           :  No
  Enable Preset / Clear Arcs                 :  No
  Disable Flight Delays                      :  No

  Corner  Analyze    Analyze
  Name    Max Paths  Min Paths
  ------  ---------  ---------
  Slow    Yes        Yes
  Fast    Yes        Yes



check_timing report

Table of Contents
-----------------
1. checking no_clock
2. checking constant_clock
3. checking pulse_width_clock
4. checking unconstrained_internal_endpoints
5. checking no_input_delay
6. checking no_output_delay
7. checking multiple_clock
8. checking generated_clocks
9. checking loops
10. checking partial_input_delay
11. checking partial_output_delay
12. checking unexpandable_clocks
13. checking latch_loops

1. checking no_clock
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There are 9 register/latch pins with no clock driven by root clock pin: divide/counter_reg[24]/C
(HIGH)

2. checking constant_clock

There are 0 register/latch pins with constant_clock.

3. checking pulse_width_clock

There are 0 register/latch pins which need pulse_width check

4. checking unconstrained_internal_endpoints

There are 21 pins that are not constrained for maximum delay. (HIGH)

There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no_input_delay

There is 1 input port with no input delay specified. (HIGH)

There are 0 input ports with no input delay but user has a false path constraint.

6. checking no_output_delay

There are 8 ports with no output delay specified. (HIGH)

There are 0 ports with no output delay but user has a false path constraint

There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple_clock

There are 0 register/latch pins with multiple clocks.

8. checking generated_clocks

There are 0 generated clocks that are not connected to a clock source.

9. checking loops

There are 0 combinational loops in the design.

10. checking partial_input_delay

There are 0 input ports with partial input delay specified.

11. checking partial_output_delay

 There are 0 ports with partial output delay specified.

12. checking unexpandable_clocks

 There are 0 unexpandable clock pairs.

13. checking latch_loops

 There are 0 combinational latch loops in the design through latch input

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| Design Timing Summary
| ---

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
7.502	0.000	0	25	0.254	0.000	0	25	4.500	0.000	0	26

All user specified timing constraints are met.

| Clock Summary
| ---

Clock	Waveform(ns)	Period(ns)	Frequency(MHz)
sys_clk_pin	{0.000 5.000}	10.000	100.000

| Intra Clock Table
| ---

Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
sys_clk_pin	7.502	0.000	0	25	0.254	0.000	0	25	4.500	0.000	0	26

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| Inter Clock Table
| -----------------
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From Clock    To Clock          WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total Endpoints
WHS(ns)      THS(ns)  THS Failing Endpoints  THS Total Endpoints
----------    --------          -------      -------  --------------------  ------------------
-------      -------  --------------------  ------------------


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| Other Path Groups Table
| -----------------------
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Path Group    From Clock    To Clock          WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total
Endpoints      WHS(ns)      THS(ns)  THS Failing Endpoints  THS Total Endpoints
----------    ----------    --------          -------      -------  --------------------
------------------      -------      -------  --------------------  ------------------


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| Timing Details
| --------------
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From Clock:  sys_clk_pin
  To Clock:  sys_clk_pin

Setup :            0  Failing Endpoints,  Worst Slack        7.502ns,  Total Violation        0.000ns
Hold  :            0  Failing Endpoints,  Worst Slack        0.254ns,  Total Violation        0.000ns
PW    :            0  Failing Endpoints,  Worst Slack        4.500ns,  Total Violation        0.000ns
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Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             7.502ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[22]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.543ns  (logic 1.966ns (77.305%)  route 0.577ns (22.695%))
  Logic Levels:           6  (CARRY4=6)
  Clock Path Skew:        -0.028ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.856ns = ( 14.856 - 10.000 )
```

```
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.637     5.158    divide/clk
    SLICE_X2Y7                                                    r  divide/counter_reg[2]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)       0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)         0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                    0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11          CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.378 r
divide/counter_reg[18]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.378    divide/n_0_counter_reg[21]_i_2
    SLICE_X2Y12          CARRY4 (Prop_carry4_CI_O[1])
                                                    0.323     7.701 r
divide/counter_reg[22]_i_2_CARRY4/O[1]
                         net (fo=1, routed)         0.000     7.701    divide/n_0_counter_reg[22]_i_1
    SLICE_X2Y12          FDRE                                     r  divide/counter_reg[22]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                   10.000    10.000 r
    W5                                              0.000    10.000 r  clk100Mhz
                         net (fo=0)                 0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.515    14.856    divide/clk
```

```
    SLICE_X2Y12                                                       r  divide/counter_reg[22]/C
                         clock pessimism              0.274    15.130
                         clock uncertainty           -0.035    15.095
    SLICE_X2Y12          FDRE (Setup_fdre_C_D)        0.109    15.204    divide/counter_reg[22]
  -------------------------------------------------------------------
                         required time                         15.204
                         arrival time                          -7.701
  -------------------------------------------------------------------
                         slack                                  7.502

Slack (MET) :             7.511ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[24]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.534ns  (logic 1.957ns (77.224%)  route 0.577ns (22.776%))
  Logic Levels:           6  (CARRY4=6)
  Clock Path Skew:        -0.028ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.856ns = ( 14.856 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.637     5.158    divide/clk
    SLICE_X2Y7                                                        r  divide/counter_reg[2]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)       0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)         0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                    0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
```

```
                         net (fo=1, routed)           0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11          CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.378 r
divide/counter_reg[18]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.378    divide/n_0_counter_reg[21]_i_2
    SLICE_X2Y12          CARRY4 (Prop_carry4_CI_O[3])
                                                      0.314     7.692 r
divide/counter_reg[22]_i_2_CARRY4/O[3]
                         net (fo=1, routed)           0.000     7.692    divide/n_0_counter_reg[24]_i_1
    SLICE_X2Y12          FDRE                                       r  divide/counter_reg[24]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                                0.000    10.000 r  clk100Mhz
                         net (fo=0)                   0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.515    14.856    divide/clk
    SLICE_X2Y12                                                   r  divide/counter_reg[24]/C
                         clock pessimism              0.274    15.130
                         clock uncertainty           -0.035    15.095
    SLICE_X2Y12          FDRE (Setup_fdre_C_D)        0.109    15.204    divide/counter_reg[24]
  -------------------------------------------------------------------
                         required time                         15.204
                         arrival time                          -7.692
  -------------------------------------------------------------------
                         slack                                  7.511

Slack (MET) :             7.586ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[23]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.459ns  (logic 1.882ns (76.529%)  route 0.577ns (23.471%))
  Logic Levels:           6  (CARRY4=6)
  Clock Path Skew:        -0.028ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.856ns = ( 14.856 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
```

```
  ------------------------------------------------------------------    -------------------
                        (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                        net (fo=0)                    0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)          1.458     1.458 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)            1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)          0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)           1.637     5.158    divide/clk
    SLICE_X2Y7                                                      r  divide/counter_reg[2]/C
  ------------------------------------------------------------------    -------------------
    SLICE_X2Y7          FDRE (Prop_fdre_C_Q)          0.518     5.676 r  divide/counter_reg[2]/Q
                        net (fo=1, routed)            0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7          CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)            0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8          CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)            0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9          CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)            0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)            0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.378 r
divide/counter_reg[18]_i_2_CARRY4/CO[3]
                        net (fo=1, routed)            0.000     7.378    divide/n_0_counter_reg[21]_i_2
    SLICE_X2Y12         CARRY4 (Prop_carry4_CI_O[2])
                                                      0.239     7.617 r
divide/counter_reg[22]_i_2_CARRY4/O[2]
                        net (fo=1, routed)            0.000     7.617    divide/n_0_counter_reg[23]_i_1
    SLICE_X2Y12         FDRE                                        r  divide/counter_reg[23]/D
  ------------------------------------------------------------------    -------------------

                        (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                                0.000    10.000 r  clk100Mhz
                        net (fo=0)                    0.000    10.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)          1.388    11.388 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)            1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)          0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)           1.515    14.856    divide/clk
    SLICE_X2Y12                                                     r  divide/counter_reg[23]/C
                        clock pessimism               0.274    15.130
                        clock uncertainty            -0.035    15.095
    SLICE_X2Y12         FDRE (Setup_fdre_C_D)         0.109    15.204    divide/counter_reg[23]
  ------------------------------------------------------------------
                        required time                         15.204
                        arrival time                          -7.617
  ------------------------------------------------------------------
                        slack                                  7.586
```

```
Slack (MET) :             7.607ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[21]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.438ns  (logic 1.861ns (76.327%)  route 0.577ns (23.673%))
  Logic Levels:           6  (CARRY4=6)
  Clock Path Skew:        -0.028ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.856ns = ( 14.856 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.637     5.158    divide/clk
    SLICE_X2Y7                                                    r  divide/counter_reg[2]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)       0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)         0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                    0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11          CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.378 r
divide/counter_reg[18]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.378    divide/n_0_counter_reg[21]_i_2
```

```
    SLICE_X2Y12          CARRY4 (Prop_carry4_CI_O[0])
                                                      0.218     7.596 r
divide/counter_reg[22]_i_2_CARRY4/O[0]
                         net (fo=1, routed)           0.000     7.596    divide/n_0_counter_reg[21]_i_1
    SLICE_X2Y12          FDRE                                         r  divide/counter_reg[21]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                                0.000    10.000 r  clk100Mhz
                         net (fo=0)                   0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.515    14.856    divide/clk
    SLICE_X2Y12                                                   r  divide/counter_reg[21]/C
                         clock pessimism              0.274    15.130
                         clock uncertainty           -0.035    15.095
    SLICE_X2Y12          FDRE (Setup_fdre_C_D)        0.109    15.204    divide/counter_reg[21]
  -------------------------------------------------------------------
                         required time                         15.204
                         arrival time                          -7.596
  -------------------------------------------------------------------
                         slack                                  7.607

Slack (MET) :             7.620ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[18]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.426ns  (logic 1.849ns (76.210%)  route 0.577ns (23.790%))
  Logic Levels:           5  (CARRY4=5)
  Clock Path Skew:        -0.027ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.857ns = ( 14.857 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                         net (fo=0)                   0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.637     5.158    divide/clk
```

```
    SLICE_X2Y7                                                        r  divide/counter_reg[2]/C
  ----------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)         0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)           0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11          CARRY4 (Prop_carry4_CI_O[1])
                                                      0.323     7.584 r
divide/counter_reg[18]_i_2_CARRY4/O[1]
                         net (fo=1, routed)           0.000     7.584    divide/n_0_counter_reg[18]_i_1
    SLICE_X2Y11          FDRE                                        r  divide/counter_reg[18]/D
  ----------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                                0.000    10.000 r  clk100Mhz
                         net (fo=0)                   0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.516    14.857    divide/clk
    SLICE_X2Y11                                                       r  divide/counter_reg[18]/C
                         clock pessimism              0.274    15.131
                         clock uncertainty           -0.035    15.096
    SLICE_X2Y11          FDRE (Setup_fdre_C_D)        0.109    15.205    divide/counter_reg[18]
  ----------------------------------------------------------------------
                         required time                         15.205
                         arrival time                          -7.584
  ----------------------------------------------------------------------
                         slack                                  7.620

Slack (MET) :             7.629ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[20]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.417ns  (logic 1.840ns (76.122%)  route 0.577ns (23.878%))
  Logic Levels:           5  (CARRY4=5)
```

```
  Clock Path Skew:        -0.027ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.857ns = ( 14.857 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.637     5.158    divide/clk
    SLICE_X2Y7                                                    r  divide/counter_reg[2]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)       0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)         0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                    0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11          CARRY4 (Prop_carry4_CI_O[3])
                                                    0.314     7.575 r
divide/counter_reg[18]_i_2_CARRY4/O[3]
                         net (fo=1, routed)         0.000     7.575    divide/n_0_counter_reg[20]_i_1
    SLICE_X2Y11          FDRE                                     r  divide/counter_reg[20]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                   10.000    10.000 r
    W5                                              0.000    10.000 r  clk100Mhz
                         net (fo=0)                 0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.516    14.857    divide/clk
    SLICE_X2Y11                                                   r  divide/counter_reg[20]/C
                         clock pessimism            0.274    15.131
```

```
                         clock uncertainty           -0.035    15.096
    SLICE_X2Y11          FDRE (Setup_fdre_C_D)        0.109    15.205    divide/counter_reg[20]
  -------------------------------------------------------------------
                         required time                         15.205
                         arrival time                          -7.575
  -------------------------------------------------------------------
                         slack                                  7.629

Slack (MET) :             7.704ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[19]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.342ns  (logic 1.765ns (75.357%)  route 0.577ns (24.643%))
  Logic Levels:           5  (CARRY4=5)
  Clock Path Skew:        -0.027ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.857ns = ( 14.857 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.637     5.158    divide/clk
    SLICE_X2Y7                                                    r  divide/counter_reg[2]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)       0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)         0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                    0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_CO[3])
```

```
                                                    0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11          CARRY4 (Prop_carry4_CI_O[2])
                                                    0.239     7.500 r
divide/counter_reg[18]_i_2_CARRY4/O[2]
                         net (fo=1, routed)           0.000     7.500    divide/n_0_counter_reg[19]_i_1
    SLICE_X2Y11          FDRE                                       r  divide/counter_reg[19]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                   10.000    10.000 r
    W5                                              0.000    10.000 r  clk100Mhz
                         net (fo=0)                 0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.516    14.857    divide/clk
    SLICE_X2Y11                                                 r  divide/counter_reg[19]/C
                         clock pessimism            0.274    15.131
                         clock uncertainty         -0.035    15.096
    SLICE_X2Y11          FDRE (Setup_fdre_C_D)      0.109    15.205    divide/counter_reg[19]
  -------------------------------------------------------------------
                         required time                         15.205
                         arrival time                          -7.500
  -------------------------------------------------------------------
                         slack                                  7.704

Slack (MET) :             7.725ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[17]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.321ns  (logic 1.744ns (75.134%)  route 0.577ns (24.866%))
  Logic Levels:           5  (CARRY4=5)
  Clock Path Skew:        -0.027ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.857ns = ( 14.857 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk100Mhz_IBUF_inst/O
```

```
                         net (fo=1, routed)           1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.637     5.158    divide/clk
    SLICE_X2Y7                                                       r  divide/counter_reg[2]/C
  ----------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)         0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)           0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.261 r
divide/counter_reg[14]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.261    divide/n_0_counter_reg[17]_i_2
    SLICE_X2Y11          CARRY4 (Prop_carry4_CI_O[0])
                                                      0.218     7.479 r
divide/counter_reg[18]_i_2_CARRY4/O[0]
                         net (fo=1, routed)           0.000     7.479    divide/n_0_counter_reg[17]_i_1
    SLICE_X2Y11          FDRE                                        r  divide/counter_reg[17]/D
  ----------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                                0.000    10.000 r  clk100Mhz
                         net (fo=0)                   0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.516    14.857    divide/clk
    SLICE_X2Y11                                                      r  divide/counter_reg[17]/C
                         clock pessimism              0.274    15.131
                         clock uncertainty           -0.035    15.096
    SLICE_X2Y11          FDRE (Setup_fdre_C_D)        0.109    15.205    divide/counter_reg[17]
  -------------------------------------------------------------------
                         required time                         15.205
                         arrival time                          -7.479
  -------------------------------------------------------------------
                         slack                                  7.725

Slack (MET) :             7.738ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[14]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
```

```
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.309ns  (logic 1.732ns (75.005%)  route 0.577ns (24.995%))
  Logic Levels:           4  (CARRY4=4)
  Clock Path Skew:        -0.026ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.858ns = ( 14.858 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                         net (fo=0)                   0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.637     5.158    divide/clk
    SLICE_X2Y7                                                      r  divide/counter_reg[2]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)         0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)           0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)           0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_O[1])
                                                      0.323     7.467 r
divide/counter_reg[14]_i_2_CARRY4/O[1]
                         net (fo=1, routed)           0.000     7.467    divide/n_0_counter_reg[14]_i_1
    SLICE_X2Y10          FDRE                                       r  divide/counter_reg[14]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                                0.000    10.000 r  clk100Mhz
                         net (fo=0)                   0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.517    14.858    divide/clk
    SLICE_X2Y10                                                     r  divide/counter_reg[14]/C
                         clock pessimism              0.274    15.132
                         clock uncertainty           -0.035    15.097
```

```
    SLICE_X2Y10          FDRE (Setup_fdre_C_D)        0.109    15.206    divide/counter_reg[14]
  -------------------------------------------------------------------
                         required time                         15.206
                         arrival time                          -7.467
  -------------------------------------------------------------------
                         slack                                  7.738

Slack (MET) :             7.747ns  (required time - arrival time)
  Source:                 divide/counter_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[16]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        2.300ns  (logic 1.723ns (74.907%)  route 0.577ns (25.093%))
  Logic Levels:           4  (CARRY4=4)
  Clock Path Skew:        -0.026ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.858ns = ( 14.858 - 10.000 )
    Source Clock Delay      (SCD):    5.158ns
    Clock Pessimism Removal (CPR):    0.274ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         1.967     3.425    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096     3.521 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        1.637     5.158    divide/clk
    SLICE_X2Y7                                                    r  divide/counter_reg[2]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)       0.518     5.676 r  divide/counter_reg[2]/Q
                         net (fo=1, routed)         0.577     6.253    divide/n_0_counter_reg[2]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[1]_CO[3])
                                                    0.657     6.910 r
divide/counter_reg[2]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     6.910    divide/n_0_counter_reg[5]_i_2
    SLICE_X2Y8           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.027 r
divide/counter_reg[6]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.027    divide/n_0_counter_reg[9]_i_2
    SLICE_X2Y9           CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117     7.144 r
divide/counter_reg[10]_i_2_CARRY4/CO[3]
                         net (fo=1, routed)         0.000     7.144    divide/n_0_counter_reg[13]_i_2
    SLICE_X2Y10          CARRY4 (Prop_carry4_CI_O[3])
                                                    0.314     7.458 r
```

```
divide/counter_reg[14]_i_2_CARRY4/O[3]
                         net (fo=1, routed)           0.000     7.458    divide/n_0_counter_reg[16]_i_1
    SLICE_X2Y10          FDRE                                         r  divide/counter_reg[16]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                                0.000    10.000 r  clk100Mhz
                         net (fo=0)                   0.000    10.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           1.862    13.250    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091    13.341 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          1.517    14.858    divide/clk
    SLICE_X2Y10                                                  r  divide/counter_reg[16]/C
                         clock pessimism              0.274    15.132
                         clock uncertainty           -0.035    15.097
    SLICE_X2Y10          FDRE (Setup_fdre_C_D)        0.109    15.206    divide/counter_reg[16]
  -------------------------------------------------------------------
                         required time                         15.206
                         arrival time                          -7.458
  -------------------------------------------------------------------
                         slack                                  7.747
```

Min Delay Paths

```
--------------------------------------------------------------------------------------
Slack (MET) :             0.254ns  (arrival time - required time)
  Source:                 divide/counter_reg[11]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[11]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.388ns  (logic 0.274ns (70.550%)  route 0.114ns (29.450%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.992ns
    Source Clock Delay      (SCD):    1.477ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                         net (fo=0)                   0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         0.226     0.226 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          0.594     1.477    divide/clk
    SLICE_X2Y9                                                   r  divide/counter_reg[11]/C
```

```
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y9           FDRE (Prop_fdre_C_Q)         0.164     1.641 r  divide/counter_reg[11]/Q
                         net (fo=1, routed)           0.114     1.756    divide/n_0_counter_reg[11]
    SLICE_X2Y9           CARRY4 (Prop_carry4_S[2]_O[2])
                                                      0.110     1.866 r
divide/counter_reg[10]_i_2_CARRY4/O[2]
                         net (fo=1, routed)           0.000     1.866    divide/n_0_counter_reg[11]_i_1
    SLICE_X2Y9           FDRE                                       r  divide/counter_reg[11]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                         net (fo=0)                   0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          0.865     1.992    divide/clk
    SLICE_X2Y9                                                   r  divide/counter_reg[11]/C
                         clock pessimism             -0.515     1.477
    SLICE_X2Y9           FDRE (Hold_fdre_C_D)         0.134     1.611    divide/counter_reg[11]
  -------------------------------------------------------------------
                         required time                         -1.611
                         arrival time                           1.866
  -------------------------------------------------------------------
                         slack                                  0.254

Slack (MET) :             0.254ns  (arrival time - required time)
  Source:                 divide/counter_reg[15]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[15]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.388ns  (logic 0.274ns (70.550%)  route 0.114ns (29.450%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.991ns
    Source Clock Delay      (SCD):    1.476ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                         net (fo=0)                   0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         0.226     0.226 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          0.593     1.476    divide/clk
    SLICE_X2Y10                                                  r  divide/counter_reg[15]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y10          FDRE (Prop_fdre_C_Q)         0.164     1.640 r  divide/counter_reg[15]/Q
```

```
                         net (fo=1, routed)           0.114     1.755    divide/n_0_counter_reg[15]
    SLICE_X2Y10          CARRY4 (Prop_carry4_S[2]_O[2])
                                                      0.110     1.865 r
divide/counter_reg[14]_i_2_CARRY4/O[2]
                         net (fo=1, routed)           0.000     1.865    divide/n_0_counter_reg[15]_i_1
    SLICE_X2Y10          FDRE                                       r  divide/counter_reg[15]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                         net (fo=0)                   0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          0.864     1.991    divide/clk
    SLICE_X2Y10                                                 r  divide/counter_reg[15]/C
                         clock pessimism             -0.515     1.476
    SLICE_X2Y10          FDRE (Hold_fdre_C_D)         0.134     1.610    divide/counter_reg[15]
  -------------------------------------------------------------------
                         required time                         -1.610
                         arrival time                           1.865
  -------------------------------------------------------------------
                         slack                                  0.254

Slack (MET) :             0.254ns  (arrival time - required time)
  Source:                 divide/counter_reg[19]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[19]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.388ns  (logic 0.274ns (70.550%)  route 0.114ns (29.450%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.991ns
    Source Clock Delay      (SCD):    1.476ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                         net (fo=0)                   0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)         0.226     0.226 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)           0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          0.593     1.476    divide/clk
    SLICE_X2Y11                                                 r  divide/counter_reg[19]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y11          FDRE (Prop_fdre_C_Q)         0.164     1.640 r  divide/counter_reg[19]/Q
                         net (fo=1, routed)           0.114     1.755    divide/n_0_counter_reg[19]
    SLICE_X2Y11          CARRY4 (Prop_carry4_S[2]_O[2])
```

```
                                                    0.110     1.865 r
divide/counter_reg[18]_i_2_CARRY4/O[2]
                         net (fo=1, routed)           0.000     1.865    divide/n_0_counter_reg[19]_i_1
    SLICE_X2Y11          FDRE                                         r  divide/counter_reg[19]/D
  ----------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       0.414     0.414 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        0.864     1.991    divide/clk
    SLICE_X2Y11                                                 r  divide/counter_reg[19]/C
                         clock pessimism           -0.515     1.476
    SLICE_X2Y11          FDRE (Hold_fdre_C_D)       0.134     1.610    divide/counter_reg[19]
  ----------------------------------------------------------------------
                         required time                         -1.610
                         arrival time                           1.865
  ----------------------------------------------------------------------
                         slack                                  0.254

Slack (MET) :             0.254ns  (arrival time - required time)
  Source:                 divide/counter_reg[23]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[23]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.388ns  (logic 0.274ns (70.550%)  route 0.114ns (29.450%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.989ns
    Source Clock Delay      (SCD):    1.475ns
    Clock Pessimism Removal (CPR):    0.514ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  ----------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       0.226     0.226 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        0.592     1.475    divide/clk
    SLICE_X2Y12                                                 r  divide/counter_reg[23]/C
  ----------------------------------------------------------------------    -------------------
    SLICE_X2Y12          FDRE (Prop_fdre_C_Q)       0.164     1.639 r  divide/counter_reg[23]/Q
                         net (fo=1, routed)         0.114     1.754    divide/n_0_counter_reg[23]
    SLICE_X2Y12          CARRY4 (Prop_carry4_S[2]_O[2])
                                                    0.110     1.864 r
divide/counter_reg[22]_i_2_CARRY4/O[2]
```

```
                        net (fo=1, routed)           0.000     1.864    divide/n_0_counter_reg[23]_i_1
    SLICE_X2Y12         FDRE                                         r  divide/counter_reg[23]/D
  -------------------------------------------------------------------    -------------------

                        (clock sys_clk_pin rise edge)
                                                     0.000     0.000 r
    W5                                               0.000     0.000 r  clk100Mhz
                        net (fo=0)                   0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)           0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)          0.862     1.989    divide/clk
    SLICE_X2Y12                                                  r  divide/counter_reg[23]/C
                        clock pessimism             -0.514     1.475
    SLICE_X2Y12         FDRE (Hold_fdre_C_D)         0.134     1.609    divide/counter_reg[23]
  -------------------------------------------------------------------
                        required time                         -1.609
                        arrival time                           1.864
  -------------------------------------------------------------------
                        slack                                  0.254

Slack (MET) :             0.254ns  (arrival time - required time)
  Source:                 divide/counter_reg[3]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[3]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.388ns  (logic 0.274ns (70.550%)  route 0.114ns (29.450%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.992ns
    Source Clock Delay      (SCD):    1.477ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                        (clock sys_clk_pin rise edge)
                                                     0.000     0.000 r
    W5                                               0.000     0.000 r  clk100Mhz
                        net (fo=0)                   0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)         0.226     0.226 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)           0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)          0.594     1.477    divide/clk
    SLICE_X2Y7                                                   r  divide/counter_reg[3]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7          FDRE (Prop_fdre_C_Q)         0.164     1.641 r  divide/counter_reg[3]/Q
                        net (fo=1, routed)           0.114     1.756    divide/n_0_counter_reg[3]
    SLICE_X2Y7          CARRY4 (Prop_carry4_S[2]_O[2])
                                                     0.110     1.866 r
divide/counter_reg[2]_i_2_CARRY4/O[2]
                        net (fo=1, routed)           0.000     1.866    divide/n_0_counter_reg[3]_i_1
    SLICE_X2Y7          FDRE                                         r  divide/counter_reg[3]/D
```

```
  ----------------------------------------------------------------    -------------------

                        (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                        net (fo=0)                    0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)          0.414     0.414 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)            0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)          0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)           0.865     1.992    divide/clk
    SLICE_X2Y7                                                      r  divide/counter_reg[3]/C
                        clock pessimism              -0.515     1.477
    SLICE_X2Y7          FDRE (Hold_fdre_C_D)          0.134     1.611    divide/counter_reg[3]
  ----------------------------------------------------------------
                        required time                          -1.611
                        arrival time                            1.866
  ----------------------------------------------------------------
                        slack                                   0.254

Slack (MET) :             0.254ns  (arrival time - required time)
  Source:                 divide/counter_reg[7]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[7]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.388ns  (logic 0.274ns (70.550%)  route 0.114ns (29.450%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.992ns
    Source Clock Delay      (SCD):    1.477ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  ----------------------------------------------------------------    -------------------
                        (clock sys_clk_pin rise edge)
                                                      0.000     0.000 r
    W5                                                0.000     0.000 r  clk100Mhz
                        net (fo=0)                    0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)          0.226     0.226 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)            0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)          0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)           0.594     1.477    divide/clk
    SLICE_X2Y8                                                      r  divide/counter_reg[7]/C
  ----------------------------------------------------------------    -------------------
    SLICE_X2Y8          FDRE (Prop_fdre_C_Q)          0.164     1.641 r  divide/counter_reg[7]/Q
                        net (fo=1, routed)            0.114     1.756    divide/n_0_counter_reg[7]
    SLICE_X2Y8          CARRY4 (Prop_carry4_S[2]_O[2])
                                                      0.110     1.866 r
divide/counter_reg[6]_i_2_CARRY4/O[2]
                        net (fo=1, routed)            0.000     1.866    divide/n_0_counter_reg[7]_i_1
    SLICE_X2Y8          FDRE                                      r  divide/counter_reg[7]/D
  ----------------------------------------------------------------    -------------------
```

```
                        (clock sys_clk_pin rise edge)
                                                     0.000     0.000 r
    W5                                               0.000     0.000 r  clk100Mhz
                        net (fo=0)                   0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)           0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)          0.865     1.992    divide/clk
    SLICE_X2Y8                                                     r  divide/counter_reg[7]/C
                        clock pessimism             -0.515     1.477
    SLICE_X2Y8          FDRE (Hold_fdre_C_D)         0.134     1.611    divide/counter_reg[7]
  ------------------------------------------------------------------
                        required time                         -1.611
                        arrival time                           1.866
  ------------------------------------------------------------------
                        slack                                  0.254

Slack (MET) :             0.262ns  (arrival time - required time)
  Source:                 divide/counter_reg[0]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[0]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.353ns  (logic 0.186ns (52.691%)  route 0.167ns (47.309%))
  Logic Levels:           1  (LUT1=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.992ns
    Source Clock Delay      (SCD):    1.477ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                        (clock sys_clk_pin rise edge)
                                                     0.000     0.000 r
    W5                                               0.000     0.000 r  clk100Mhz
                        net (fo=0)                   0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)         0.226     0.226 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)           0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)          0.594     1.477    divide/clk
    SLICE_X3Y7                                                     r  divide/counter_reg[0]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X3Y7          FDRE (Prop_fdre_C_Q)         0.141     1.618 f  divide/counter_reg[0]/Q
                        net (fo=2, routed)           0.167     1.785    divide/n_0_counter_reg[0]
    SLICE_X3Y7          LUT1 (Prop_lut1_I0_O)        0.045     1.830 r  divide/counter[0]_i_1/O
                        net (fo=1, routed)           0.000     1.830    divide/n_0_counter[0]_i_1
    SLICE_X3Y7          FDRE                                       r  divide/counter_reg[0]/D
  -------------------------------------------------------------------    -------------------

                        (clock sys_clk_pin rise edge)
                                                     0.000     0.000 r
    W5                                               0.000     0.000 r  clk100Mhz
                        net (fo=0)                   0.000     0.000    clk100Mhz
```

```
    W5                  IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)           0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)          0.865     1.992    divide/clk
    SLICE_X3Y7                                                     r  divide/counter_reg[0]/C
                        clock pessimism             -0.515     1.477
    SLICE_X3Y7          FDRE (Hold_fdre_C_D)         0.091     1.568    divide/counter_reg[0]
  -------------------------------------------------------------------
                        required time                         -1.568
                        arrival time                           1.830
  -------------------------------------------------------------------
                        slack                                  0.262

Slack (MET) :             0.279ns  (arrival time - required time)
  Source:                 divide/counter_reg[0]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[1]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.426ns  (logic 0.299ns (70.143%)  route 0.127ns (29.857%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.013ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.992ns
    Source Clock Delay      (SCD):    1.477ns
    Clock Pessimism Removal (CPR):    0.502ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                        (clock sys_clk_pin rise edge)
                                                     0.000     0.000 r
    W5                                               0.000     0.000 r  clk100Mhz
                        net (fo=0)                   0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)         0.226     0.226 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)           0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                        net (fo=25, routed)          0.594     1.477    divide/clk
    SLICE_X3Y7                                                     r  divide/counter_reg[0]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X3Y7          FDRE (Prop_fdre_C_Q)         0.141     1.618 r  divide/counter_reg[0]/Q
                        net (fo=2, routed)           0.127     1.745    divide/n_0_counter_reg[0]
    SLICE_X2Y7          CARRY4 (Prop_carry4_CYINIT_O[0])
                                                     0.158     1.903 r
divide/counter_reg[2]_i_2_CARRY4/O[0]
                        net (fo=1, routed)           0.000     1.903    divide/n_0_counter_reg[1]_i_1
    SLICE_X2Y7          FDRE                                       r  divide/counter_reg[1]/D
  -------------------------------------------------------------------    -------------------

                        (clock sys_clk_pin rise edge)
                                                     0.000     0.000 r
    W5                                               0.000     0.000 r  clk100Mhz
                        net (fo=0)                   0.000     0.000    clk100Mhz
    W5                  IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk100Mhz_IBUF_inst/O
                        net (fo=1, routed)           0.685     1.099    clk100Mhz_IBUF
```

```
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)          0.865     1.992    divide/clk
    SLICE_X2Y7                                                      r  divide/counter_reg[1]/C
                         clock pessimism             -0.502     1.490
    SLICE_X2Y7           FDRE (Hold_fdre_C_D)         0.134     1.624    divide/counter_reg[1]
  -------------------------------------------------------------------
                         required time                         -1.624
                         arrival time                           1.903
  -------------------------------------------------------------------
                         slack                                  0.279

Slack (MET) :             0.290ns  (arrival time - required time)
  Source:                 divide/counter_reg[11]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[12]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.424ns  (logic 0.310ns (73.048%)  route 0.114ns (26.952%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.992ns
    Source Clock Delay      (SCD):    1.477ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       0.226     0.226 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        0.594     1.477    divide/clk
    SLICE_X2Y9                                                      r  divide/counter_reg[11]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y9           FDRE (Prop_fdre_C_Q)       0.164     1.641 r  divide/counter_reg[11]/Q
                         net (fo=1, routed)         0.114     1.756    divide/n_0_counter_reg[11]
    SLICE_X2Y9           CARRY4 (Prop_carry4_S[2]_O[3])
                                                    0.146     1.902 r
divide/counter_reg[10]_i_2_CARRY4/O[3]
                         net (fo=1, routed)         0.000     1.902    divide/n_0_counter_reg[12]_i_1
    SLICE_X2Y9           FDRE                                   r  divide/counter_reg[12]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       0.414     0.414 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        0.865     1.992    divide/clk
```

```
    SLICE_X2Y9                                                        r  divide/counter_reg[12]/C
                         clock pessimism             -0.515     1.477
    SLICE_X2Y9           FDRE (Hold_fdre_C_D)         0.134     1.611    divide/counter_reg[12]
  -------------------------------------------------------------------
                         required time                         -1.611
                         arrival time                           1.902
  -------------------------------------------------------------------
                         slack                                  0.290

Slack (MET) :             0.290ns  (arrival time - required time)
  Source:                 divide/counter_reg[3]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            divide/counter_reg[4]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.424ns  (logic 0.310ns (73.048%)  route 0.114ns (26.952%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.992ns
    Source Clock Delay      (SCD):    1.477ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       0.226     0.226 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         0.631     0.858    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.026     0.884 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        0.594     1.477    divide/clk
    SLICE_X2Y7                                                        r  divide/counter_reg[3]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X2Y7           FDRE (Prop_fdre_C_Q)       0.164     1.641 r  divide/counter_reg[3]/Q
                         net (fo=1, routed)         0.114     1.756    divide/n_0_counter_reg[3]
    SLICE_X2Y7           CARRY4 (Prop_carry4_S[2]_O[3])
                                                    0.146     1.902 r
divide/counter_reg[2]_i_2_CARRY4/O[3]
                         net (fo=1, routed)         0.000     1.902    divide/n_0_counter_reg[4]_i_1
    SLICE_X2Y7           FDRE                                  r  divide/counter_reg[4]/D
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk100Mhz
                         net (fo=0)                 0.000     0.000    clk100Mhz
    W5                   IBUF (Prop_ibuf_I_O)       0.414     0.414 r  clk100Mhz_IBUF_inst/O
                         net (fo=1, routed)         0.685     1.099    clk100Mhz_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.029     1.128 r  clk100Mhz_IBUF_BUFG_inst/O
                         net (fo=25, routed)        0.865     1.992    divide/clk
    SLICE_X2Y7                                                        r  divide/counter_reg[4]/C
                         clock pessimism             -0.515     1.477
```

```
    SLICE_X2Y7           FDRE (Hold_fdre_C_D)         0.134     1.611    divide/counter_reg[4]
  -------------------------------------------------------------------
                         required time                         -1.611
                         arrival time                           1.902
  -------------------------------------------------------------------
                         slack                                  0.290
```

```
Pulse Width Checks
------------------------------------------------------------------------------------------
Clock Name:         sys_clk_pin
Waveform:           { 0 5 }
Period:             10.000
Sources:            { clk100Mhz }

Check Type        Corner  Lib Pin  Reference Pin  Required  Actual  Slack  Location       Pin
Min Period        n/a     BUFG/I   n/a            2.155     10.000  7.845  BUFGCTRL_X0Y0
clk100Mhz_IBUF_BUFG_inst/I
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X3Y7
divide/counter_reg[0]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y9
divide/counter_reg[10]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y9
divide/counter_reg[11]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y9
divide/counter_reg[12]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y10
divide/counter_reg[13]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y10
divide/counter_reg[14]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y10
divide/counter_reg[15]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y10
divide/counter_reg[16]/C
Min Period        n/a     FDRE/C   n/a            1.000     10.000  9.000  SLICE_X2Y11
divide/counter_reg[17]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X3Y7
divide/counter_reg[0]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y9
divide/counter_reg[10]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y9
divide/counter_reg[11]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y9
divide/counter_reg[12]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y10
divide/counter_reg[13]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y10
divide/counter_reg[14]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y10
divide/counter_reg[15]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y10
divide/counter_reg[16]/C
Low Pulse Width   Slow    FDRE/C   n/a            0.500     5.000   4.500  SLICE_X2Y11
divide/counter_reg[17]/C
```

Low Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y11 divide/counter_reg[18]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X3Y7 divide/counter_reg[0]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9 divide/counter_reg[10]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9 divide/counter_reg[11]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y9 divide/counter_reg[12]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10 divide/counter_reg[13]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10 divide/counter_reg[14]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10 divide/counter_reg[15]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y10 divide/counter_reg[16]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y7 divide/counter_reg[1]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X2Y7 divide/counter_reg[2]/C