Requirements

1. Specify the design requirements that your solution must fulfill.
2. This does not require tools in the lab.
3. Inputs: report (lab manual) specifying the requirements. Outputs: concise list of functional requirements.

Design Specifications

1. Refer to design requirements, and specify the specifications that your solution must operate under.
2. This does not require tools in the lab.
3. Inputs: List of all the functional requirements Output: Detailed description of all the design specifications which the system should operate under

Design Entry

1. Here we create a high level solution using a descriptive language according to the design specifications.
2. This step does not require tools in the lab.
3. Inputs: design specifications. Outputs: code for solution.

Simulation

1. Simulate the hardware that may be synthesized by the solution’s code.
2. This step requires a computer that can simulate code: modelsim
3. Inputs: untested code for solution Outputs: tested code for solution.

Logic Synthesis

1. Conversion of the higher-level abstract description of the design to actual components at the gate and flip-flop level.
2. This step uses the Vivado synthesis tool
3. Input: Design specifications with requirements for solution Output: Description of the hardware needed at a gate level

Post Synthesis Simulation

1. Load synthesized code (bitfile) onto the test fpga to debug design according to specs.
2. This step requires vivado with a license to load the board with the bitfile an fpga board
3. Input: synthesized code (bitfile) Output: code synthesized to a particular hardware configuration

Design Realizations

1. Put a design on a FPGA or ASIC so the design can be implemented and used to satisfy the design requirements and specifications.
2. The hardware manager (vivado) which allows you to program the device
3. Input: synthesized code specific to a particular hardware configuration, and design requirements and specifications to refer to. Output: a working FPGA or ASIC with the design mapped onto a specific target, placed into a specific part in the target, and the connections between all components routed, which satisfies the requirements and specifications.