COSC 290

Class Exercises #11 (Ch. 6-1)

* + - 1. Suppose a computer has 220 bytes of byte-addressable main memory and a cache size of 212 bytes, and each cache block contains 128 bytes.

1. How many blocks of main memory are there?

8192 blocks in MM

1. What is the format of a memory address as seen by cache if this cache is a direct mapped cache? To which cache block will the memory address 0x7A6DC map?

|  |  |  |
| --- | --- | --- |
| Tag – 8 bits | Block – 5 bits | Offset – 7 bits |
| 0111 1010 | 0110 1 | 101 1100 |

0x7A6DC maps to block 13.

1. What is the format of a memory address as seen by cache if this cache is using fully associative cache? To which cache block will the memory address 0x7A6DC map?

|  |  |
| --- | --- |
| Tag – 13 bits | Offset – 7 bits |
| 0111 1010 0110 1 | 101 1100 |

0x7A6DC could map to any block by nature of the fully associative cache.

1. What is the format of a memory address as seen by cache if this cache is 2-way set associative cache? To which cache block will the memory address 0x7A6DC map?

|  |  |  |
| --- | --- | --- |
| Tag – 9 bits | Set – 4 bits | Offset – 7 bits |
| 0111 1010 0 | 110 1 | 101 1100 |

0x7A6DC could map to any block in set 13 (Blocks 16, 27 in 2-way set-associative)

1. What is the format of a memory address as seen by cache if this cache is 4-way set associative cache? To which cache block will the memory address 0x7A6DC map?

|  |  |  |
| --- | --- | --- |
| Tag – 10 bits | Set – 3 bits | Offset – 7 bits |
| 0111 1010 01 | 10 1 | 101 1100 |

0x7A6DC could map to any block in set 5 (Blocks 20, 21, 22, 23 in 4-way set-associative)

1. Suppose we have a computer that uses a memory address word size of 8 bits. This computer has a 16-byte cache with 4 bytes per block. The computer accesses a number of memory locations throughout the course of running a program.

Suppose this computer uses direct-mapped cache. The format of a memory address as seen

by the cache is shown below:



The system accesses memory addresses in this exact order: 0x6E, 0xB9, 0x17, 0xE0, 0x4E,

0x4F, 0x50, 0x91, 0xA8, 0xA9, 0xAB, 0xAD, 0x93, and 0x94. The memory addresses of the

first four accesses have been loaded into the cache blocks as shown below. (The contents

of the tag are shown in binary and the cache “contents” are simply the address stored at

that cache location.)



a) What is the hit ratio for the entire memory reference sequence given above, assuming

we count the first four accesses as misses?

|  |  |
| --- | --- |
| Address | Hit or Miss |
| 0x6E | Miss |
| 0xB9 | Miss |
| 0x17 | Miss |
| 0xE0 | Miss |
| 0x4E | Miss |
| 0x4F | Hit |
| 0x50 | Miss |
| 0x91 | Miss |
| 0xA8 | Miss |
| 0xA9 | Hit |
| 0xAB | Hit |
| 0xAD | Miss |
| 0x093 | Hit |
| 0x94 | Miss |

b) What memory blocks will be in the cache after the last address has been accessed?

The cache stores MM blocks 36, 37, 42, and 43 after accessing all addresses, as diagrammed below.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Tag | Cache Contents |  |  | Tag | Cache Contents |
| Block 0 | 1001 | 0x90 |  | Block 1 | 1001 | 0x94 |
|  |  | 0x91 |  |  |  | 0x95 |
|  |  | 0x92 |  |  |  | 0x97 |
|  |  | 0x93 |  |  |  | 0x98 |
|  |  |  |  |  |  |  |
| Block 2 | 1010 | 0xA8 |  | Block 3 | 1010 | 0xAC |
|  |  | 0xA9 |  |  |  | 0xAD |
|  |  | 0xAA |  |  |  | 0xAE |
|  |  | 0xAB |  |  |  | 0xAF |