Design Assignment: Washing Machine Health Monitor With Vibration Analysis

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Course: Design of Electronic Devices and Systems

1. Introduction & Project Definition

1.1 Project Abstract

The "Washing Machine Health Monitor" is a portable, battery-powered diagnostic instrument designed to implement predictive maintenance for domestic washing machines. Unlike traditional repair strategies which are reactive (fixing a machine after it breaks), this device enables proactive monitoring by analyzing the acoustic and vibrational "fingerprint" of the appliance.

The device utilizes a piezoelectric contact sensor to capture mechanical vibrations. The signal is processed through a custom analog front-end—featuring a programmable gain amplifier and split-path filtering—before being analyzed by an onboard microcontroller. By comparing real-time Fast Fourier Transform (FFT) data and high-frequency envelope signatures against a learned statistical baseline, the device detects incipient faults such as bearing wear, belt degradation, and suspension failure. The system provides the user with a quantitative "Health Percentage" and specific fault alerts via an LCD interface, allowing for maintenance before catastrophic failure occurs.

1.2 Product Classification

Based on the definitions provided in the course material (Lecture 1), this device is classified as follows:

- **Product Type: Prototype.**
  The device is a fully functional, autonomous unit designed to verify performance and usability. It is "ready for use" and encapsulated, distinguishing it from a simple technology demonstrator. While currently a single unit, the design choices (PCB layout, component selection) are made with **Small Series** production standards in mind, ensuring reproducibility.
- **Customer Profile: Group A (Professional/Enthusiast).**
  The intended user is an engineering enthusiast or appliance technician. This profile implies a user who understands the device's operating principles and limitations. However, regarding environmental robustness, the device is designed to withstand the conditions typical of a "Group C" environment (a humid, vibrating laundry room), requiring the durability of a consumer product.
- **Lifecycle & Usage:**
  The device is designed for intermittent use over a lifecycle of 3-5 years. It features a rechargeable power system and a robust enclosure to survive the physical handling associated with attaching sensors to vibrating machinery.

1.3 Target Specifications

- **Core Functionality:**
    - **Vibration Analysis:** Real-time FFT (Frequency Domain) for detecting unbalance and motor faults.
    - **Envelope Analysis:** High-frequency demodulation for detecting early-stage bearing pitting.
    - **Adaptive Monitoring:** "Learn Mode" to establish statistical baselines for specific machine load cycles (e.g., Spin, Drain).
- **Inputs & Sensors:**
    - **Primary Sensor:** External Piezoelectric Transducer (contact microphone) for direct mechanical coupling.
    - **User Interface:** Two buttons, one for scrolling and one for Selecting.
- **Outputs & Display:**
    - **Visual:** 128x64 Graphic LCD (or 16x2 Character LCD) displaying "Health %" and active fault codes.
    - **Status Indicators:** LED indicator for Charging status and Power state.
- **Electronic System:**
    - **Logic Voltage:** 3.3V System.
    - **Analog Front End:** Custom multi-stage op-amp circuit with active filtering (2nd Order Sallen-Key) and Envelope Detection.
    - **Processing:** Microcontroller with DSP capabilities.
- **Power System:**
    - **Source:** Single-cell Lithium-Polymer (LiPo) battery (3.7V).
    - **Charging:** USB-C 5V input with TP4056 management.
    - **Regulation:** Low-Dropout (LDO) regulation for stable analog and digital rails.
- **Mechanical:**
    - **Form Factor:** Handheld plastic enclosure (ABS).
    - **Protection:** Shielded internal analog section; vibration-resistant component mounting.

2. The Core Function

2.1 Operational Theory

The core engineering challenge of this device is the detection of low-amplitude, high-frequency fault signatures in the presence of high-amplitude, low-frequency noise.

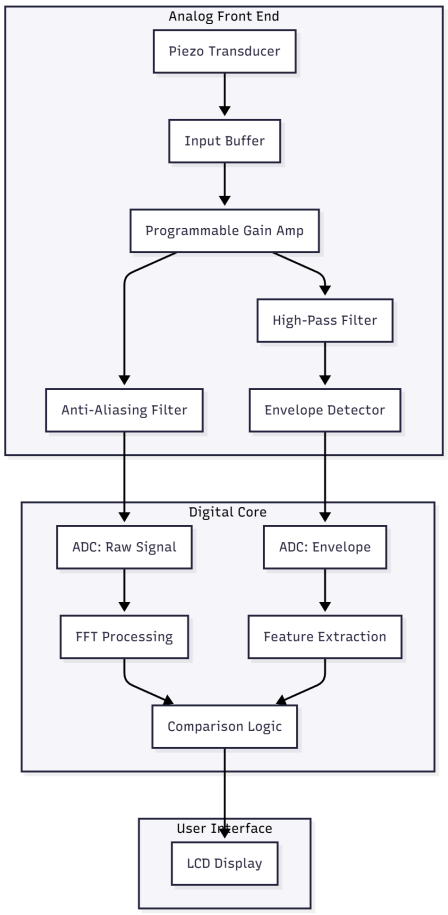
A washing machine is a dynamic system. Normal operation involves significant vibration caused by the rotation of an unbalanced load of wet laundry. This creates a powerful sinusoidal vibration signal at the fundamental rotational frequency (1x RPM, typically 10-20 Hz). In a standard vibration meter, this signal would completely mask the subtle signatures of incipient mechanical failure.

This device differentiates between "Healthy Variation" and "Defect Signatures" based on the following physical principles:

- **Load Unbalance (Benign):** Manifests as a high-energy peak at the fundamental frequency (1x RPM) and low harmonics. Its amplitude varies with laundry load mass but its frequency content is predictable.
- **Bearing Faults (Malign):** Early-stage bearing pitting creates repetitive, microscopic impacts. These impacts excite the machine's structural resonances, producing low-energy "ringing" in the high-frequency spectrum (typically >2 kHz).
- **Envelope Demodulation:** To detect bearing faults, the device utilizes a dedicated analog path to isolate these high-frequency impulse chains from the low-frequency unbalance noise. By demodulating the amplitude of the resonant ringing, the system extracts the repetition rate of the impacts, allowing for the identification of specific bearing or motor faults.

2.2 Signal Chain Architecture

The system architecture is designed as a mixed-signal pipeline. To ensure signal integrity (Lecture 4), the architecture physically partitions the sensitive Analog Signal Conditioning from the high-speed Digital Processing.



- **Sensor Interface:** A piezoelectric contact transducer converts mechanical stress into a high-impedance voltage signal.
- **Analog Front-End (AFE):**
    1. **Impedance Buffering:** Preserves the sensor signal integrity.
    2. **Programmable Gain Amplifier (PGA):** An MCU-controlled stage that optimizes dynamic range, preventing clipping during heavy spin cycles while amplifying weak signals during agitation.
    3. **Path A (Spectral Analysis):** A 2nd-order Anti-Aliasing Low-Pass Filter prepares the signal for the MCU's ADC.
    4. **Path B (Feature Extraction):** A High-Pass Filter (>2 kHz) removes load noise, followed by an Envelope Detector to convert high-frequency fault impacts into a readable DC voltage.
- **Digital Core:** An embedded microcontroller samples both analog paths, performs a Fast Fourier Transform (FFT), and executes the diagnostic algorithms.

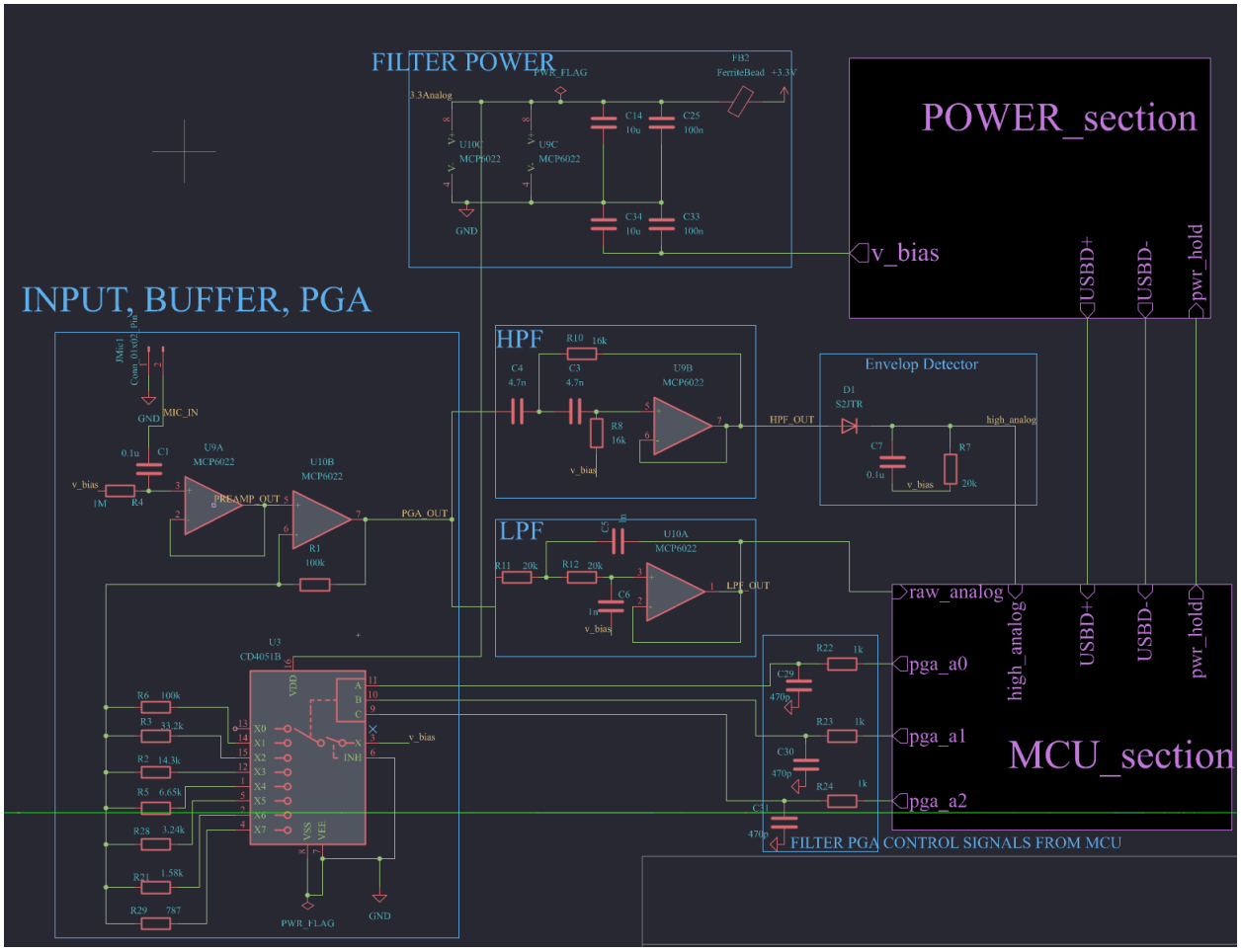
2.3 Software Strategy

The device firmware addresses the lack of manufacturer data by utilizing a **Reference-Based Comparison Strategy**. The definition of "Fault" is derived from statistical deviation rather than absolute thresholds.

- **State-Aware Operation:** To account for different mechanical states, the user selects a specific profile (e.g., "Spin Cycle", "Drain Cycle") before operation. Data is only compared against historical data from the same state.
- **Learning Mode (Baseline Creation):** The device records multiple cycles of a healthy machine. It computes the **Mean** and **Standard Deviation** for each frequency bin in the FFT. This builds a statistical model of "Normal," where high variance in low frequencies (due to load) is accepted as healthy behavior. This obviously complicates the software. Ideally there is a “Healthy Operation” data from the manufacturer and the comparison is done against that.
- **Monitoring Mode (Fault Detection):**
    - **Health Trending:** The current measurement is compared to the baseline. Progressive deviations (e.g., slowly rising high-frequency noise floor) result in a gradual decrease of the "Health %" metric.
    - **Fault Alerting:** Sudden, statistically significant anomalies—such as the appearance of a new peak at 100Hz (Electrical Fault) or a spike in the Envelope Detector output—trigger specific fault alerts.

3. Circuit Design & Schematics

3.1 Analog Front-End (AFE) Design



The Analog Front-End is responsible for conditioning the raw, high-impedance signal from the piezoelectric sensor into a robust, buffered, and filtered signal suitable for the microcontroller's Analog-to-Digital Converter (ADC). The circuit is powered by a single-supply 3.3V rail and utilizes a 1.65V Virtual Ground (V_bias) to allow AC signals to swing within the rail limits.

3.1.1 Input Stage, Buffer, and Programmable Gain Amplifier (PGA)

The input stage provides impedance matching and dynamic range control.

Input Filter: A passive High-Pass filter formed by C1 (0.1 µF) and R4 (1 MΩ). This blocks any DC offset from the sensor and biases the signal to V_bias (1.65 V).

Cutoff Frequency:
$f_c = 1 / (2\pi RC) \approx 1.6$ Hz.
This ensures low-frequency unbalance signals (typically 10 Hz) are preserved.

Input Buffer (U9A): A unity-gain voltage follower prevents the subsequent circuitry from loading down the high-impedance piezo sensor, preserving signal integrity.

Programmable Gain Amplifier (U10B): A non-inverting amplifier configuration where the gain is controlled digitally by the MCU.
Gain Logic: The feedback resistor R1 is fixed at 100 kΩ. The ground-leg resistance (R_g) is selected by a CD4051B analog multiplexer (U3).
Gain Formula:
$A_v = 1 + R1 / R_g$
Selected Gains: By switching different resistors (R6 through R29), the gain can be set in binary steps (1×, 2×, 4× … up to 128×), allowing the device to handle both massive spin-cycle vibrations and microscopic bearing ticks without clipping or losing resolution.

3.1.2 High-Pass Filter (HPF)

Purpose: To remove high-amplitude low-frequency noise (motor hum, drum unbalance) and isolate the high-frequency "ringing" characteristic of bearing faults.
Topology: 2nd-Order Sallen-Key Active High-Pass Filter (U9B).
Design Values:
$C3 = C4 = 4.7$ nF
$R8 = R10 = 16$ kΩ

Calculation:
$f_c = 1 / (2\pi \cdot R8 \cdot R10 \cdot C3 \cdot C4)$

$f_c = 1 / (2\pi \cdot 16000 \cdot 4.7\times10^{-9}) \approx 2116$ Hz

Result: Signals below ~2.1 kHz are attenuated at 40 dB/decade, effectively isolating the fault signature.

3.1.3 Envelope Detector

Purpose: To convert the high-frequency AC ringing from the HPF into a DC voltage representing the amplitude of the fault impacts. This allows the MCU to read the "severity" of the bearing fault without needing to sample at ultrasonic speeds.

Circuit Operation:

Rectification: Diode D1 allows current to flow only on positive signal peaks.

Smoothing: Capacitor C7 (0.1 µF) stores the peak voltage, while resistor R7 (20 kΩ) slowly discharges it.

Time Constant (τ):

$\tau = R \cdot C = 20000 \cdot 0.1 \times 10^{-6} = 2$ ms

Result: This time constant is optimized to smooth out the 2 kHz carrier wave while still responding fast enough to track impact repetition rates up to 500 Hz.

3.1.4 Anti-Aliasing Low-Pass Filter (LPF)

Purpose: To remove frequencies above the Nyquist limit of the MCU's ADC sampling rate, preventing high-frequency noise from appearing as false low-frequency aliases in the FFT.

Topology: 2nd-Order Sallen-Key Active Low-Pass Filter (U10A).

Design Values:

R11 = R12 = 20 kΩ

C5 = C6 = 1 nF

Calculation:

$f_c = 1 / (2\pi \cdot 20000 \cdot 1 \times 10^{-9}) \approx 7957$ Hz

Result: With a cutoff at ~8 kHz, this filter allows for a sampling rate of roughly 16–20 kSPS, capturing all relevant mechanical vibration data while rejecting ultrasonic noise.

3.1.5 Digital Control Filtering

Purpose: To prevent high-frequency digital switching noise from the MCU traveling along the control lines (pga_a0, pga_a1, pga_a2) and radiating into the sensitive analog section.

Circuit: Simple RC Low-Pass filters placed at the entry to the analog shield.

Values: R = 1 kΩ, C = 470 pF.

Calculation:

$f_c = 1 / (2\pi \cdot 1000 \cdot 470 \times 10^{-12}) \approx 338$ kHz

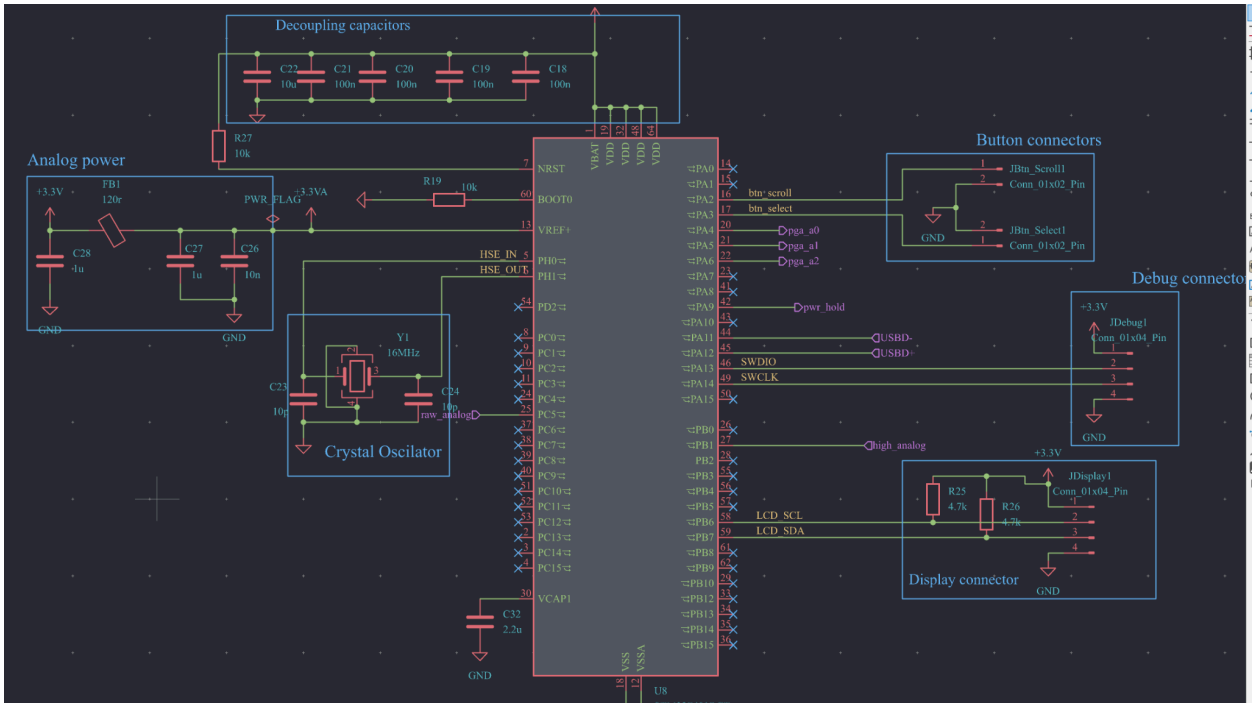
Result: This passes the static logic levels for gain selection but blocks megahertz-range clock noise from the MCU.

3.1.6 Power and Bias

Filter Power: Decoupling capacitors (C14, C25, C34, C33) are placed close to the op-amp power pins to provide local energy reservoirs and filter power supply noise.

Bias Voltage (V_bias): A stable 1.65 V DC reference connects to the non-inverting inputs of the filters and buffers. This "lifts" the AC signals to the midpoint of the 0 V–3.3 V range, preventing clipping against the ground rail. The ferrite bead (FB2) provides high-frequency isolation between the main 3.3 V rail and the sensitive Analog 3.3 V rail.

3.2 Digital Core Design



The Digital Core is built around an STM32F4-series microcontroller (MCU). This section handles the system orchestration, including sampling the analog signals, performing the Fast Fourier Transform (FFT) mathematics, driving the user interface, and managing power states.

3.2.1 Microcontroller Selection

Component: STM32F401RCT6 (LQFP-64 Package).

Justification:

Performance: Contains an ARM Cortex-M4 core with a Floating Point Unit (FPU). The FPU is critical for calculating FFTs efficiently in real time without stalling the system.
ADC Specs: Features a 12-bit ADC capable of high sample rates (>2 Msps), comfortably satisfying the Nyquist requirement for the 8 kHz bandwidth defined in the Analog Front-End.
Voltage: Native 3.3 V operation simplifies interfacing with the analog section.

3.2.2 Clock System (Crystal Oscillator)

While the MCU has an internal RC oscillator, the precise timing required for accurate frequency analysis (FFT) demands a stable external clock source.
Configuration: High-Speed External (HSE) Oscillator.
Component: Y1, a 16 MHz Quartz Crystal.
Load Capacitors (C23, C24): 10 pF.

Calculation:
The load capacitance seen by the crystal is defined as:

$$C_{load} = (C23 \cdot C24) / (C23 + C24) + C_{stray}$$

Assuming parasitic stray capacitance C_{stray} of approx. 4–5 pF, using 10 pF capacitors provides a load of ≈9 pF, which matches standard low-profile crystals.

3.2.3 Power Stability & Analog Isolation

Digital switching noise is mitigated through a rigorous decoupling network, ensuring the MCU does not crash during high current demands and does not inject noise back into the power rails.

Decoupling Network: A bank of capacitors (C18–C22) is placed immediately adjacent to the MCU power pins. This includes:
- **100 nF Ceramic:** Handles high-frequency switching transients (nanosecond response).
- **10 µF Bulk:** Handles lower-frequency current surges (microsecond response).

Analog Power Filter:
The MCU's internal ADC requires a clean voltage reference.
Circuit: A Pi-filter formed by a Ferrite Bead (FB1) and capacitors (C26, C27, C28).
Function: Creates a local “quiet zone” for the ADC power supply pins (V_{DDA}), blocking high-frequency digital noise from the main 3.3 V rail.

Core Regulator:
Capacitor C32 (2.2 µF) is connected to pin 30 (V_CAP1) to stabilize the MCU's internal 1.2 V logic core regulator.

3.2.4 User Interface & Peripherals

Display Interface: The LCD connects via an I2C bus (pins PB6/PB7).
Pull-Up Resistors: R25 and R26 (4.7 kΩ) pull the open-drain SDA and SCL lines to 3.3 V, defining the idle state of the bus.

Input Controls:
- **Rotary Encoder:** Connected to PA0 and PA1 (btn_scroll) for menu navigation.
- **Selection Button:** Connected to PA2 (btn_select).

Internal pull-up resistors are enabled in software.

Debug Interface:
A standard SWD (Serial Wire Debug) header connects to PA13/PA14, allowing programming and real-time debugging.

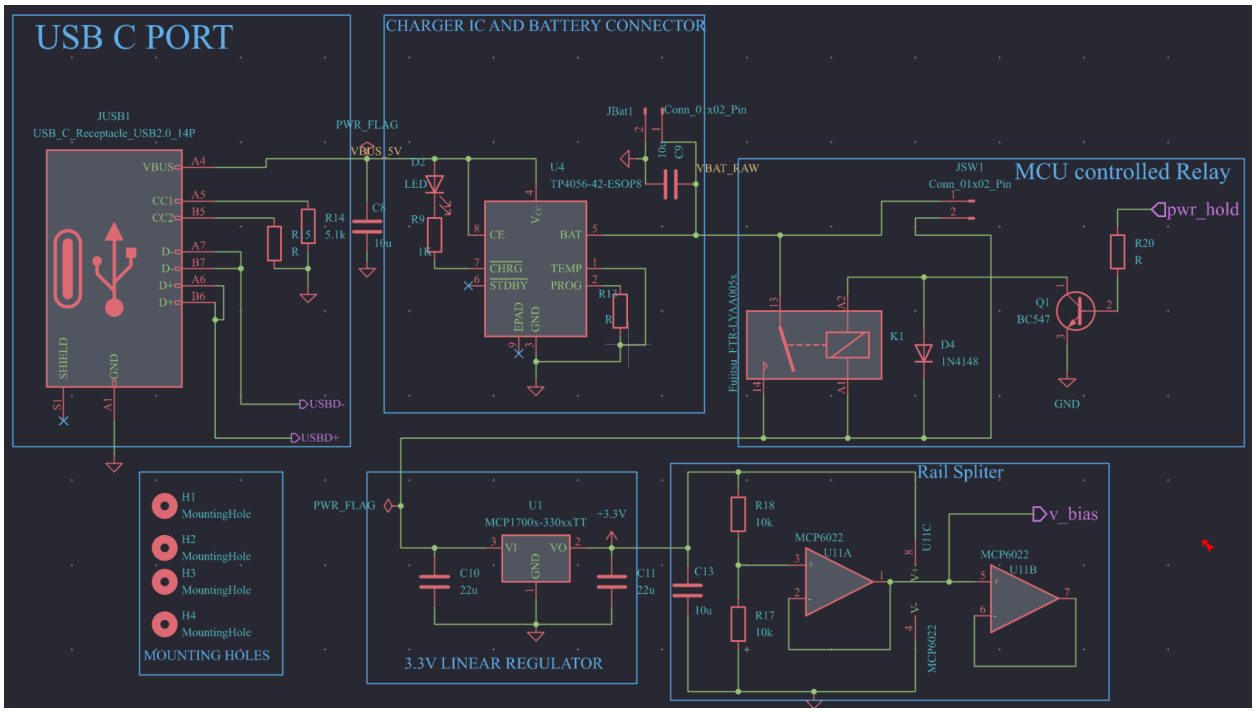
3.2.5 Signal Interfacing

The MCU bridges the analog and digital domains through specific assignments:

ADC Inputs:
- PC0: Samples the Raw Analog signal (for FFT).
- PB1: Samples the High-Analog (Envelope Detector) signal.

Digital Outputs:
- PA4, PA5, PA6: Control the CD4051 Multiplexer to set the PGA gain.
- PA9: Controls the Power Hold transistor, maintaining system power after the user releases the momentary button.

3.3 Power System Design



The power architecture is designed for portability, utilizing a single-cell Lithium-Polymer (LiPo) battery as the primary energy source. The system manages three distinct voltage domains: Raw Battery Voltage (V_{BAT}), the System Logic Voltage ($3.3V$), and the Analog Bias Voltage (1.65V).

3.3.1 Input and Charging

- **USB-C Interface (JUSB1):** A standard USB-C receptacle provides 5V for charging.
    - **Configuration:** The configuration channel pins ($CC1$ and $CC2$) are pulled down via $5.1\text{k}\Omega$ resistors (R14,R15). This identifies the device as a "Sink" to the power source, enabling charging from modern USB-C PD chargers as well as legacy USB-A ports.

- **Charge Management (U4):** A TP4056 Constant-Current/Constant-Voltage (CC/CV) linear charger manages the LiPo battery.
    - **Programming:** Resistor $\mathrm{R13}$ sets the maximum charging current to safe levels for the specific battery capacity selected.
    - **Indication:** An LED ($D2$) provides visual feedback during the active charging phase.

3.3.2 Power Control Logic (Auto-Power-Off)

To maximize battery life and fulfill the course requirement for an electromechanical relay, the device utilizes a "Soft Latch" power circuit. This allows the microcontroller to physically disconnect the battery when idle, reducing standby current to near zero.

- **Start-Up:** When the user presses the momentary switch $JSW1$, raw battery power bypasses the relay and feeds the regulator, booting the MCU.
- **Latching:** Upon boot, the MCU asserts a HIGH signal on the `pwr_hold` line. This saturates the NPN transistor $Q1$ (BC547), which energizes the coil of Relay $K1$. The relay contacts close, creating a parallel path for the power.
- **Run State:** The user can release the button, and the relay maintains the power connection.
- **Shutdown:** To turn off, the MCU drives `pwr_hold` LOW. The transistor cuts current to the relay coil, the contacts open, and the system performs a hard power-down.

3.3.3 Voltage Regulation (LDO)

- **Component:** MCP1700-3302E ($\mathrm{U1}U1$).
- **Specification:** 3.3V Fixed Output, Low Quiescent Current.
- **Selection Justification:** Standard linear regulators (like the AMS1117) have a high dropout voltage ($\approx 1.2V$), requiring an input of $>4.5V$ to output $3.3V$. Since a LiPo battery voltage ranges from $4.2V$ (full) down to $3.0V$ (empty), a standard regulator would fail. The MCP1700 is a **Low Dropout (LDO)** regulator with a dropout of only $178mV$, allowing stable 3.3V regulation even as the battery discharges down to $\approx 3.5V$.

3.3.4 Virtual Ground (Rail Splitter)

To allow the single-supply op-amps in the Analog Front-End to amplify AC signals without clipping against the ground rail, a stable mid-point reference (V_{bias}) is required.**Circuit:** An active voltage divider using an Op-Amp Buffer.

    - **Reference:** A resistive divider ($R17$,$R18$) creates a $1.65V$ reference $\mathrm{VCC}/2$$V_{CC}/2$).
    - **Buffer (U11A):** An MCP6022 op-amp configured as a voltage follower buffers this reference. This provides a low-impedance "Virtual Ground" that can source and sink current to maintain a steady $1.65V$ regardless of the load presented by the analog filters.
- **Stability:** The unused half of the op-amp ($U11B$) is safely terminated as a voltage follower connected to V_{bias}, preventing oscillation and reducing power consumption.

3.4 Software Architecture

The device firmware utilizes a finite state machine (FSM) architecture to manage user inputs, power consumption, and signal processing. The logic is divided into two primary flows: the **Main Control Loop** and the **Measurement & Analysis Subroutine**.

3.5.1 Main Control Flowchart

The main loop monitors the user interface and manages battery life. It implements the "Auto-Power-Off" feature using the relay/transistor latch circuit designed in the hardware phase.

3.5.2 Core Analysis Algorithm Flowchart

This routine contains the DSP (Digital Signal Processing) and the predictive maintenance logic. It handles the auto-ranging gain and the statistical comparison

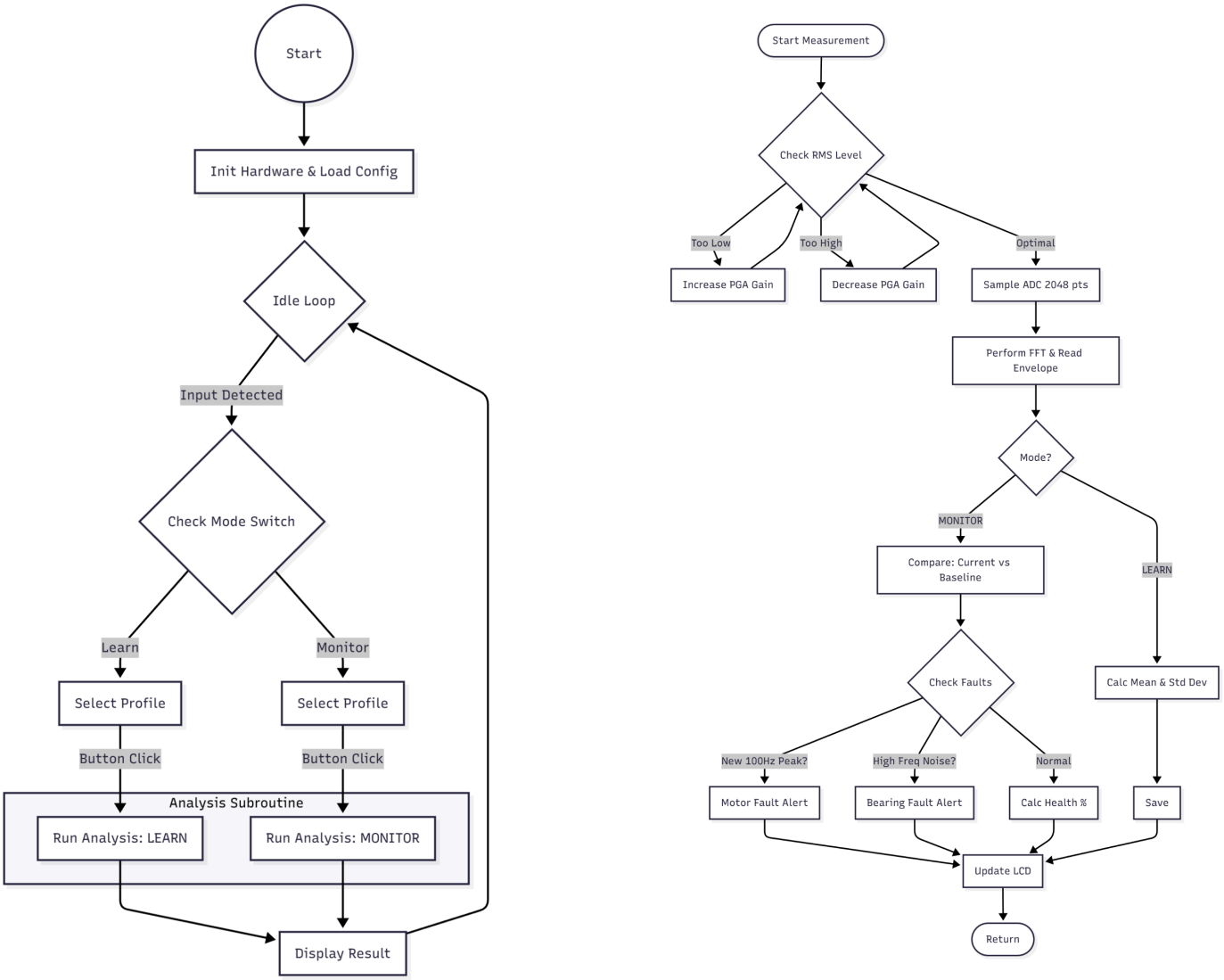


Figure: Software Flowcharts

4. Environmental Conditions & Robustness

4.1 Environmental Analysis

The intended operating environment for this device—a domestic laundry room or basement, directly attached to vibrating machinery—presents specific hazards categorized as "Hostile" in Lecture 3.

- **Moisture and Humidity:**
    - **Condensation:** Laundry environments often experience rapid temperature and humidity shifts (e.g., a dryer running in a cool basement), creating a risk of condensation forming on the PCB.
    - **Liquid Ingress:** There is a moderate risk of direct splashes from water supply hoses, laundry sinks, or detergents.
    - **Chemical Exposure:** Detergents and softeners are corrosive agents that can degrade exposed copper and solder joints over time.
- **Mechanical Stress (Vibration & Shock):**
    - **Direct Coupling:** Unlike a device sitting on a shelf, this monitor is mechanically coupled to the vibration source. It must endure the low-frequency, high-displacement "thumping" of an unbalanced load (approx. 10 Hz) and the high-frequency vibration of the motor.
    - **Drop Risk:** As a handheld portable device, it is subject to shock loads from being dropped onto hard tiled floors.

4.2 Design Mitigations

To ensure reliability under these conditions, the following design strategies (derived from Lecture 3) have been implemented:

4.2.1 Mechanical Rigidity & Assembly

- **PCB Mounting Strategy:**
    - To prevent mechanical stress from transferring to the circuit board during thermal expansion or vibration, the PCB is secured using **M3 screws** passing through **3.5mm diameter mounting holes**.
    - As suggested in Lecture 3, this loose tolerance (0.5mm clearance) prevents shear forces from cracking the PCB material or stressing solder joints when the enclosure flexes.

- **Massive Component Security:**
    - **Battery:** The LiPo battery is the heaviest component. It is **not** supported by its solder tabs. Instead, it is mechanically secured to the enclosure chassis using industrial double-sided foam tape (VHB) to prevent detachment during vibration.
    - **Connectors:** Locking **JST-XH** connectors are used for the battery and sensor interfaces instead of standard pin headers, preventing disconnection due to shaking.

4.2.2 Component Selection for Vibration

- **Crystal Oscillator:** Standard vertical crystals act as levers during vibration and are prone to fatigue failure. This design utilizes a **Through-Hole HC-49/U crystal mounted horizontally (flat)** against the PCB.

4.2.3 Ingress Protection Strategy (Target: IP54)

To ensure reliability in a laundry environment—characterized by high humidity, airborne lint, and potential water splashing—the device is designed to meet the **IP54 standard** (Dust Protected / Splash Proof). This is achieved through a multi-layered mechanical and chemical defense strategy.

- **Enclosure Sealing (The Primary Barrier):**
    - **Mating Surfaces:** The split-line between the top and bottom enclosure halves is sealed using a **die-cut silicone rubber gasket** or a continuous bead of RTV silicone sealant during assembly. This accommodates mechanical flexing caused by vibration without breaking the seal.
    - **Display Window:** The LCD opening is sealed by a clear polycarbonate window, bonded to the inside of the enclosure using a waterproof structural adhesive. This eliminates the gap typically found in bezel-mounted displays.
    - **I/O Ports:** The USB-C charging port is protected by a removable **silicone dust plug** when not in use, preventing lint accumulation and water entry.
- **Internal Circuit Protection (The Secondary Barrier):**
    - **Conformal Coating:** As a final line of defense against condensation (which can form inside even sealed enclosures due to temperature drops), the assembled PCB will be treated with an **Acrylic Conformal Coating** (e.g., MG Chemicals 419D).
    - **Application:** This dielectric coating covers the microcontroller legs, passive components, and sensitive analog traces. It prevents the formation of conductive dendrites or short circuits caused by moisture, while still allowing for thermal expansion.

5. Electromagnetic Compatibility (EMC) & Shielding

5.1 Noise Source Analysis

To determine the appropriate shielding strategy, the “Noise Budget” was analyzed by identifying the dominant interference sources affecting the high-impedance piezoelectric signal.

Internal Source: Microcontroller (Electric Field Dominant)

Mechanism: The STM32 microcontroller and its associated digital logic lines operate with fast rise-time clock edges (high dV/dtdV/dtdV/dt). This creates broadband high-frequency noise harmonics extending into the MHz range.
Coupling: As a high-impedance source, this noise couples primarily via Electric Fields (Capacitive Coupling) onto adjacent traces.

External Source: Washing Machine Motor (Magnetic Field Dominant)

Mechanism: The device is mounted directly onto a machine driven by a high-power electric motor. Universal motors (brushed) generate significant broadband arcing noise, while the high currents create strong magnetic flux.
Coupling: As a low-impedance, high-current source, this noise couples primarily via Magnetic Fields (Inductive Coupling) into any loop areas present in the signal path.

5.2 Shielding Strategy

A multi-layered defense strategy was implemented to address both field types based on the “Near Field” characteristics (Lecture 4).

5.2.1 PCB Level: Partitioning

The PCB layout utilizes physical separation as the first defense. The board is divided into two distinct zones:

- **Zone A (Noisy):** Contains the Power inputs, Battery management, and Microcontroller.
- **Zone B (Quiet):** Contains the Piezo input, Op-Amps, and Filters.

Implementation: These zones are placed on opposite ends of the PCB to maximize the distance between the noise source and the victim.

5.2.2 Cable Level: Coaxial Transmission

The external sensor connection represents the largest potential antenna for interference.

Solution: A shielded coaxial cable is used.
Termination: The cable shield is grounded immediately at the PCB entry point (JMic1). This shunts external induced currents to the system ground before they can penetrate the shielded analog zone.

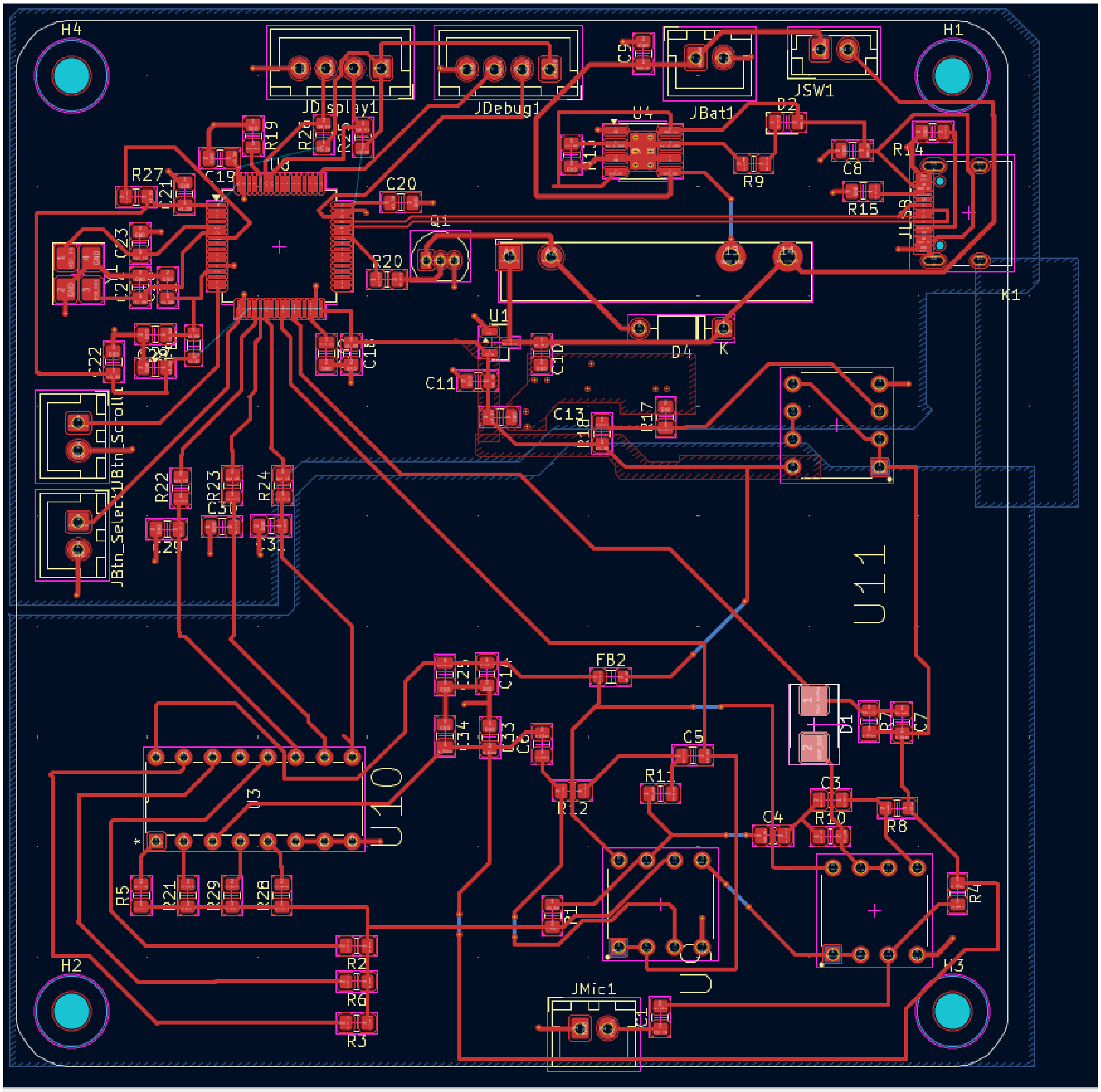
5.3 Grounding Topology

To prevent “Ground Bounce” (where noise currents create voltage offsets in the ground plane), a Split-Plane Star Grounding topology is implemented.

Concept: Analog signals are referenced to a precise voltage. If digital return currents flow through the analog ground reference, the resistance of the copper trace ($V = I_{noise} \times R_{trace}$) creates a noise voltage that is added to the signal.

Implementation:

- **Dirty Ground Plane:** A large copper pour under the Digital/Power section handles the noisy return currents from the MCU and LEDs.
- **Clean Ground Plane:** A separate, isolated copper pour lies under the Analog section.
- **The Star Point:** These two planes are connected at one single point (via a rectangle near the USB). This ensures they share a DC reference potential, but prevents high-frequency digital currents from traversing the analog plane.


H4
H1
H2
H3
JDisplay1
JDebug1
JBat1
JSW1
U4
D2
R9
C8
R14
R15
K1
C9
R19
R27
C19
C20
Q1
R20
U1
D4
K
C11
C13
R17
R22
R23
R24
C29
C31
U11
FB2
D1
R7
C7
C5
R11
R12
C3
C4
R10
R8
R4
U10
U3
R5
R21
R29
R28
R2
R6
R3
JMic1

6. Component Selection

6.1 Bill of Materials (BOM)

Electronic Components (PCB)

Reference	Qty	Value	Description	Package / Footprint	Est. Price (Unit)
U8	1	STM32F401RCT6	Microcontroller, ARM Cortex-M4	LQFP-64	$4.50
U4	1	TP4056	LiPo Battery Charger IC	SOIC-8-EP	$0.20
U1	1	MCP1700-3302E	LDO Voltage Regulator, 3.3V	SOT-23	$0.35
U9, U10, U11	3	MCP6022	Rail-to-Rail Op-Amp, Dual	SOIC-8	$0.90
U3	1	CD4051B	Analog Multiplexer 8:1	SOIC-16	$0.40
K1	1	FTR-LYAA005x	Relay, 5V Coil, SPST-NO	THT	$1.50
Q1	1	BC547	NPN Transistor	TO-92	$0.05
D1	1	S2JTR	Rectifier Diode (Fast Recovery)	SMB	$0.10
D2	1	LED (Red)	Charging Indicator	0805 SMD	$0.05
D4	1	1N4148	Small Signal Diode (Flyback)	DO-35	$0.02
Y1	1	16 MHz	Crystal Oscillator	HC-49/US SMD	$0.30
FB1, FB2	2	600Ω @ 100MHz	Ferrite Bead	0805 SMD	$0.05
JUSB1	1	USB-C	USB Type-C Receptacle (16-pin)	HRO-TYPE-C-31	$0.50
JBat, JMic, etc.	6	JST-XH	Connectors (2-pin & 4-pin)	JST-XH THT	$0.15
C_Various	23	(Various)	Ceramic Capacitors (10pF - 100nF)	0805 SMD	$0.01
C_Bulk	8	10uF, 22uF	Ceramic Capacitors (Bulk)	0805 SMD	$0.05
R_Various	23	(Various)	Resistors (1% Tolerance)	0805 SMD	$0.01

Mechanical & Off-Board Components

Component	Qty	Description	Purpose	Est. Price
Sensor	1	Piezoelectric Disc (27mm)	Vibration Transducer	$0.50
Battery	1	LiPo Battery 3.7V 1000mAh	Power Source	$8.00
Display	1	LCD 1602 (I2C)	User Interface Display	$4.00
Controls	1	Rotary Encoder w/ Button	Menu Navigation	$1.50
Switch	1	Momentary Push Button	Power On / Select	$0.50
Cable	1m	RG-174 Coaxial Cable	Shielded Sensor Connection	$1.00
Enclosure	1	Custom 3D Printed / ABS Box	Device Housing	$5.00
Protection	1	Acrylic Conformal Coating	Moisture Protection	$15.00 (Can)
Sealing	1	RTV Silicone Sealant	Waterproofing Gaskets	$5.00 (Tube)
Hardware	4	M3 Screws & Standoffs	PCB Mounting	$0.50

6.2 Selection Justification

- **Microcontroller (STM32F401**): Selected for its ARM Cortex-M4F core which includes a hardware Floating Point Unit (FPU), enabling efficient real-time calculation of FFTs. Its low power consumption and rich peripheral set (ADC, I2C) minimize external component count.
- **Op-Amp (MCP6022)**: Chosen specifically for its Rail-to-Rail Input/Output capability and low operating voltage (2.5V - 5.5V). This allows the analog front-end to run directly from the 3.3V system rail, eliminating the need for a noisy high-voltage switching regulator and protecting the MCU ADC inputs.
- **Voltage Regulator (MCP1700)**: Selected over standard regulators (like AMS1117) due to its Low Dropout (LDO) characteristic. It can maintain a stable 3.3V output even when the LiPo battery drops to 3.5V, maximizing usable battery life.
- **Charging IC (TP4056)**: Chosen as a robust, industry-standard solution for single-cell LiPo charging, featuring integrated protection against over-current and thermal runaway.

- **Crystal (HC-49)**: A larger metal-can package was selected over miniature ceramic crystals to provide greater mechanical robustness against the vibration of the washing machine environment.

7. PCB Design & Layout

7.1 Layout Strategy

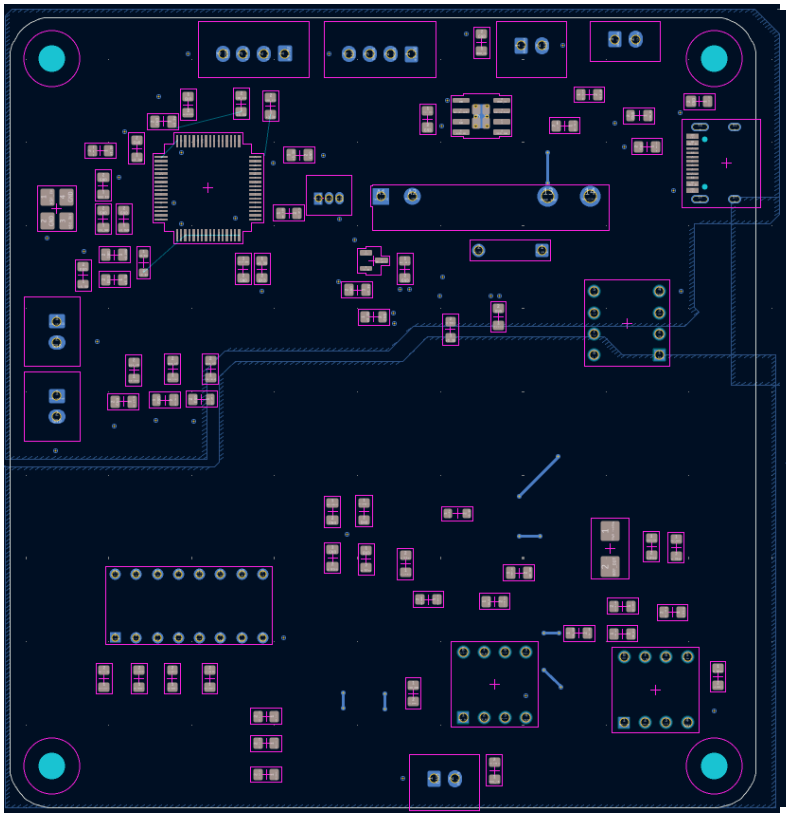
The physical layout of the printed circuit board is critical to the device's signal integrity. A strict **Partitioning Strategy** was employed to separate noise sources from sensitive measurement circuits.

- **Zone A: Digital & Power (Top)**
    - Contains the USB-C connector, Battery Charger (TP4056), LDO Regulator (MCP1700), and the STM32 Microcontroller.
    - This area handles high-speed digital logic (16 MHz).
- **Zone B: Analog Front-End (Bottom Right)**
    - Contains the Piezo input, Op-Amps, and Filters.
    - This area is physically isolated by a "moat" (gap in the copper pour) to prevent digital return currents from crossing under sensitive analog traces.
- **Star Point:** The two ground planes connect at a single point near the power supply filter, forcing noise currents to return directly to the source without contaminating the analog reference.

7.2 PCB Layers

The design utilizes a standard **2-Layer FR-4** stack-up.

- **Top Layer (Signal & Component):** Carries the majority of signal traces. A copper pour on this layer is connected to Ground to provide additional shielding.
- **Bottom Layer (Ground Plane):** Dedicated almost entirely to solid Ground Planes ("Clean" and "Dirty") to minimize loop inductance.
- **Silk Screen:** Provides clear labeling for connectors (BAT, MIC, USB) and test points for easier assembly and debugging.



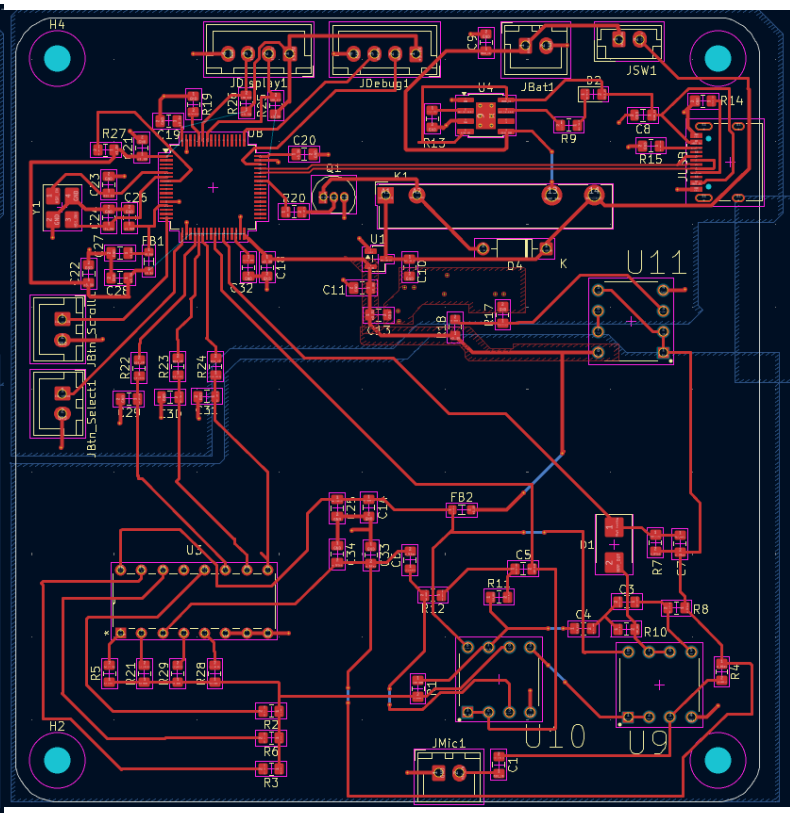


Figure: Bottom layer(Ground) and Top Layer(connections)

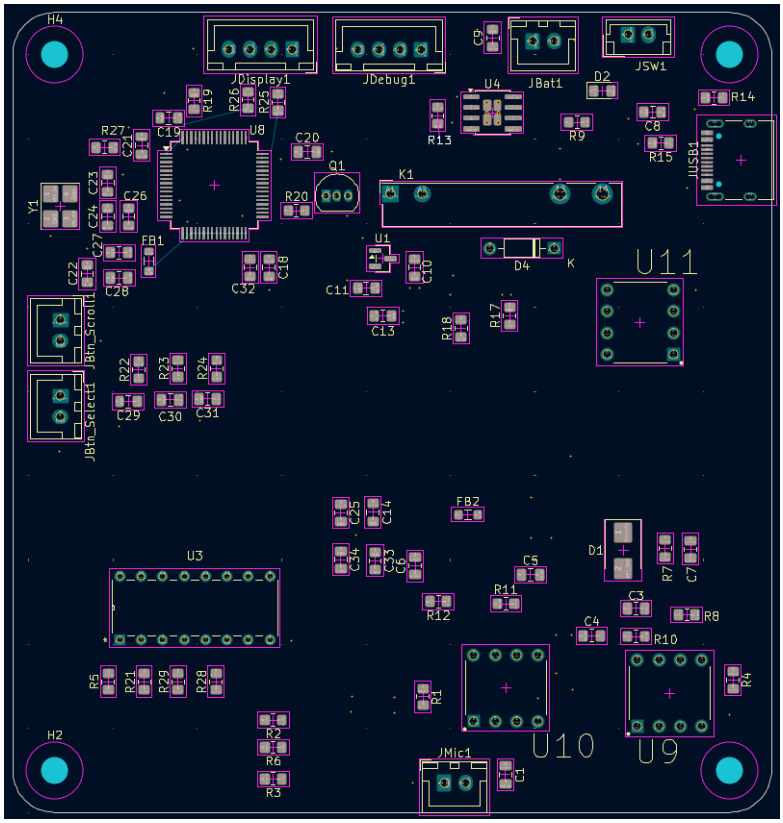


Figure: Silkscreen layer

7.3 3D Visualization

The board was modeled in 3D to verify component clearances and connector placement.
(Note: 3D models for specific components like the JST connectors were not available in the library and are represented by their footprint outlines).

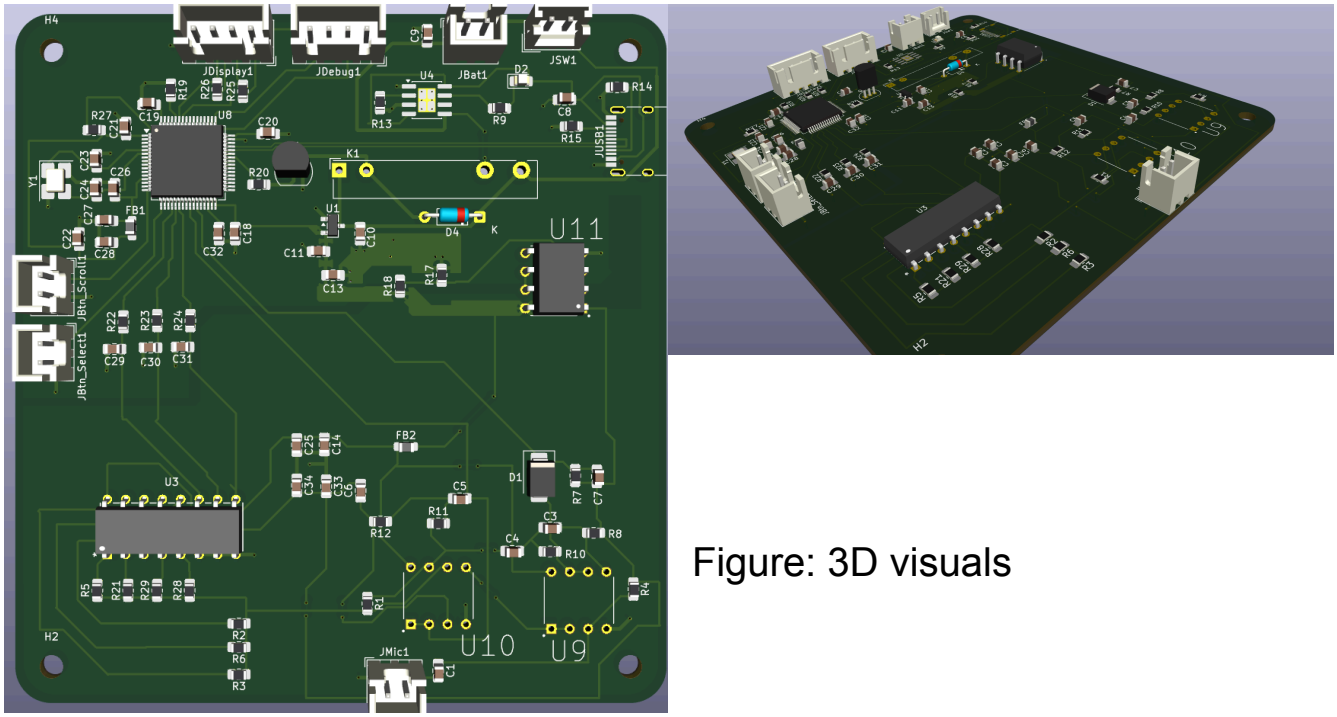


Figure: 3D visuals

7.4 Design Rules (DRC)

The PCB was routed according to the manufacturing capabilities of **JLCPCB** for a standard 2-layer board.

- **Manufacturing Specifications:**
  - **Minimum Track Width:** 0.25 mm (10 mil) for signals, exceeding the vendor minimum of 0.127 mm to ensure robustness.
  - **Minimum Clearance:** 0.2 mm between tracks and pads.
  - **Via Size:** 0.3 mm drill / 0.6 mm diameter.
  - **Copper Weight:** 1 oz (35µm).

- **Power Distribution:**
    - **Signal Traces:** 0.3 mm width.
    - **Power Traces (3.3V, VBUS, VBAT): 0.5 mm** width. This increased width reduces resistance and voltage drop for the high-current paths from the USB port and battery.
    - **Ground:** Handled by full copper pours (zones) on the bottom layer to provide the lowest possible impedance path.

8. Mechanical Design & Enclosure

8.1 Sensor Interface (Acoustic Coupling)

To maintain the **IP54** ingress protection rating without requiring complex seals, the piezoelectric sensor is mounted internally using a **"Blind Pocket"** configuration.

- **Design:** A recessed pocket is modeled into the interior bottom face of the enclosure. While the standard enclosure wall thickness is 2.5 mm for structural rigidity, the floor of this pocket is reduced to a thickness of **0.6 mm**.
- **Acoustic Transmission:** This thin membrane minimizes the attenuation of high-frequency vibrations (bearing fault signatures) that would otherwise be absorbed by the plastic.
- **Assembly:** The piezoelectric disc is bonded directly to this thin section using a rigid cyanoacrylate or epoxy adhesive. This ensures the sensor moves in unity with the enclosure floor, effectively acting as a contact microphone.

8.2 User Interface (Top Panel)

The user interface is arranged on the top face to allow for easy reading and manipulation while the device is pressed vertically against a washing machine.

- **Display:** The LCD is mounted behind a clear acrylic window. The window is bonded to the enclosure using a waterproof structural adhesive to prevent fluid ingress.
- **Controls:**
    - **Buttons:** Two buttons, one for scrolling through options and the other for selecting.
    - **Power Switch:** A sealed toggle switch or push-button allows for mode selection and power control.
- **Status Indicators:** A light pipe is used to transmit the status of the internal charging LED to the exterior, eliminating the need for a through-hole LED that could leak. A small hole near the USB port.

8.3 Mechanical Drawings & Specifications

The enclosure is designed for manufacturing via FDM 3D Printing (Prototype) or Injection Molding (Series Production).

- **Material:** ABS or PETG (Selected for impact resistance and thermal stability up to 60°C).
- **Dimensions:** Approx. 100mm x 60mm x 30mm (customized to fit PCB).
- **Mounting Strategy:**
    - **PCB:** Secured via four internal mounting bosses utilizing M3 self-tapping screws. The boss locations align exactly with the PCB mounting holes.
    - **Battery:** Secured to the chassis via VHB tape, independent of the PCB.
    - **Enclosure Assembly:** The case consists of a "tub" and a "lid," secured by four corner screws. A groove is designed into the mating rim to accept a silicone sealing cord or RTV gasket.

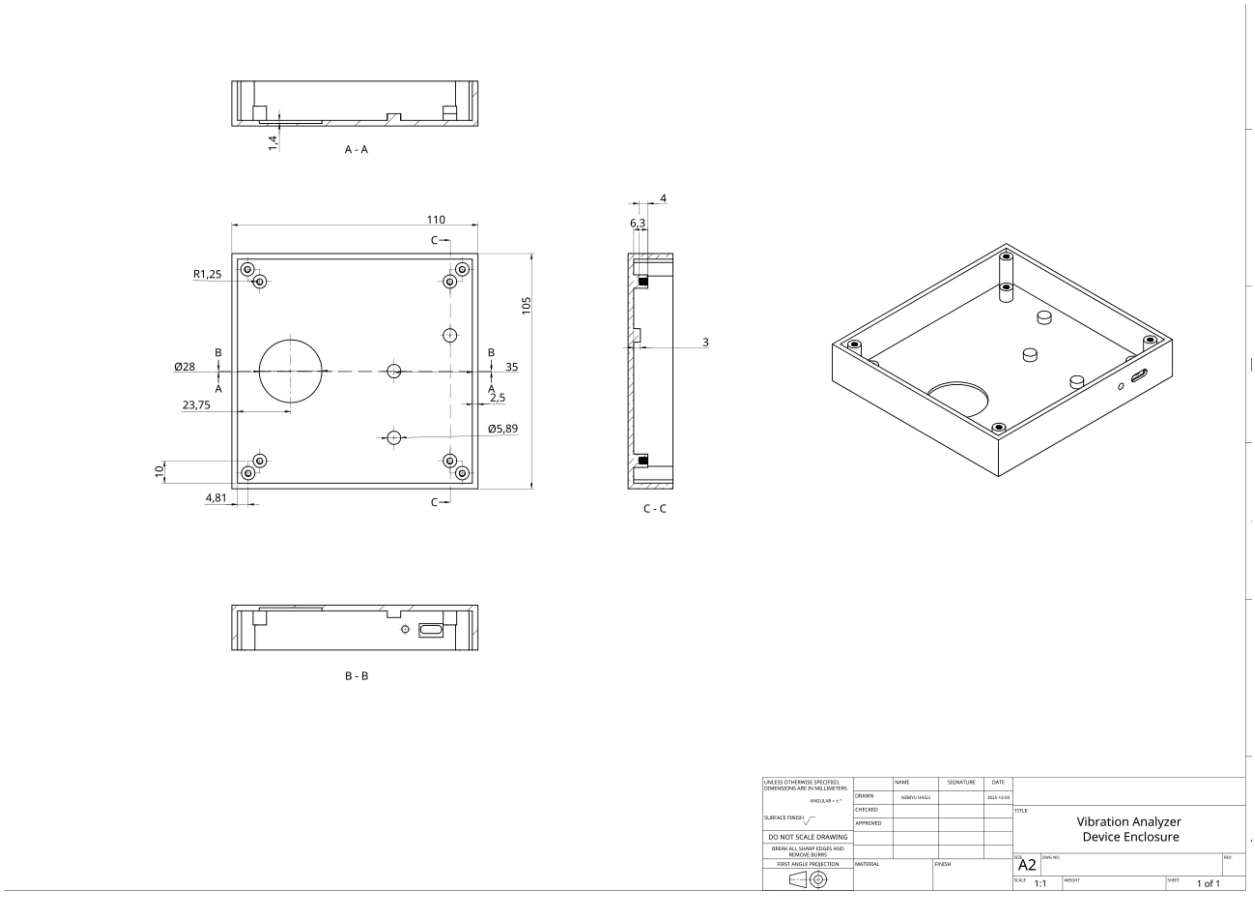


Figure: Enclosure Drawing Part 1

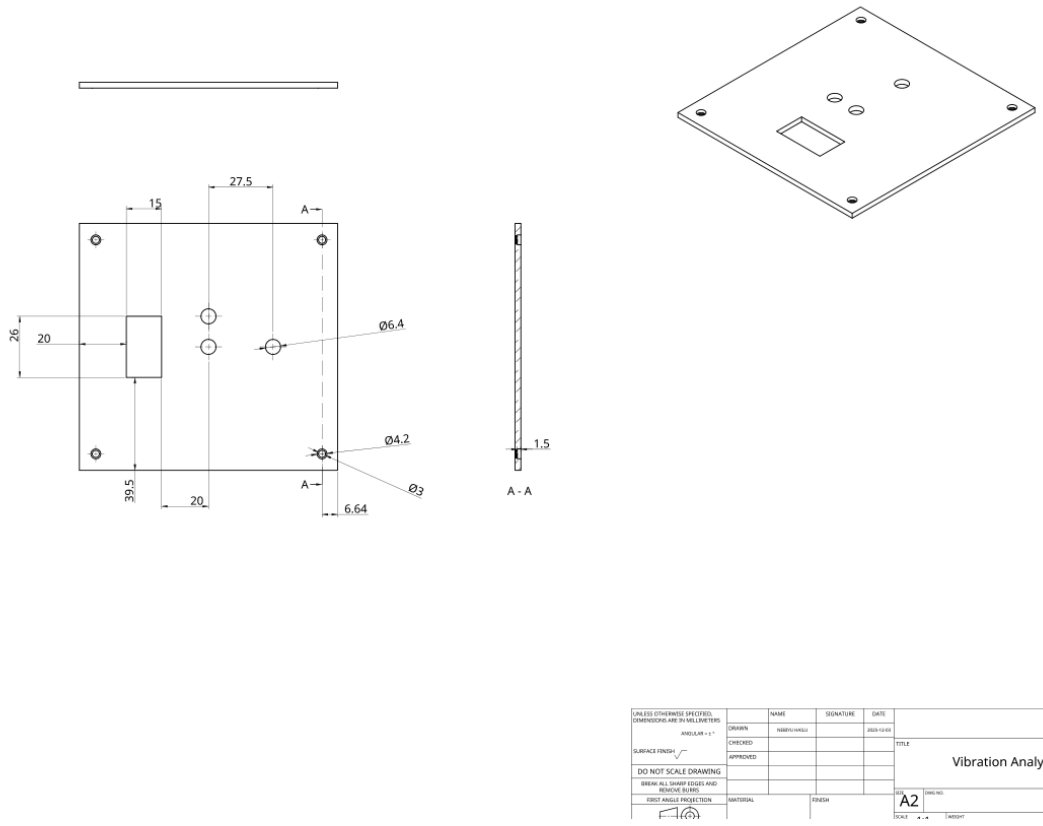


Figure: Enclosure Drawing, Part 2

9. Testing & Validation Plan

This section outlines the standardized test procedures required to verify the prototype's functionality, calibration, and robust operation. Following the principles of Lecture 11, testing is divided into **Simulation**, **Step-by-Step Electrical Bring-up**, and **Functional Validation**.

9.1 Simulation Validation (SPICE)

Before physical assembly, the Analog Front-End (AFE) performance is verified using **LTspice** simulation to ensure component values match the calculated frequency response.

- **Test 1: High-Pass Filter Response (AC Analysis)**
    - **Stimulus:** AC Sweep from 1 Hz to 20 kHz at 1V amplitude.
    - **Measurement Point:** Output of Op-Amp U9B.

    - **Pass Criteria:** Gain must be -3dB at approx. **2.1 kHz**. Frequencies below 100 Hz must be attenuated by >40dB.
- **Test 2: Envelope Detector (Transient Analysis)**
    - **Stimulus:** 2 kHz Sine Wave (simulated bearing fault) modulated at 50 Hz.
    - **Measurement Point:** Output of Diode D1/Capacitor C7.
    - **Pass Criteria:** Output must be a smooth DC voltage (ripple < 100mV) that tracks the amplitude of the 2 kHz bursts.

9.2 Prototype Electrical Verification

Following the "Step-by-Step" approach recommended in Lecture 11, the physical hardware is tested in stages to prevent catastrophic component failure.

Required Instruments: Digital Multimeter (DVM) with 10 MΩ input impedance, Oscilloscope (2-Channel), Adjustable Laboratory Power Supply (3.7V).

Procedure:

1. **Power Rail Verification (Passive):**
    - *Action:* With **no power applied**, check continuity between VCC and GND.
    - *Pass Criteria:* No short circuits (Resistance > 1 kΩ).

2. **Power Regulation (Active, No Load):**
    - *Action:* Apply 3.7V to the Battery Connector.
    - *Measurement:* Probe Output of U1 (LDO) and the Virtual Ground point.
    - *Pass Criteria:* LDO Output **= 3.3V** ± **1%**. Virtual Ground **= 1.65V** ± **1%**.
3. **Quiescent Bias Check:**
    - *Action:* Probe the non-inverting inputs of all Op-Amps.
    - *Pass Criteria:* All inputs must sit exactly at **1.65V (Virtual Ground)**. If an input is at 0V or 3.3V, the biasing resistor network is faulty.
4. **Digital "Heartbeat":**
    - *Action:* Flash minimal firmware to toggle an LED.
    - *Pass Criteria:* LED blinks, confirming MCU is alive and clock is running.

9.3 Shielding Effectiveness Test

This procedure validates the EMI design decisions (Chapter 5) using a comparative "Before and After" test.

- **Setup:** Place the device near a known noise source (e.g., a running universal motor or a mains transformer).
- **Configuration A (Unshielded):** Remove the metal shield can from the Analog Section.
    - *Action:* Run the device's "Spectrum Monitor" mode. Record the noise floor level on the display.
- **Configuration B (Shielded):** Install and solder the metal shield can. Connect the Sensor Cable shield to chassis ground.
    - *Action:* Repeat measurement in the exact same position.
- **Pass Criteria:** The noise floor in Configuration B must be at least **-20dB lower** than in Configuration A, proving the effectiveness of the Faraday cage and cable shielding.

9.4 Functional Calibration & Reference Test

As "Primary Standards" for washing machine health do not exist (Lecture 11), the device is calibrated against a **Reference Healthy Machine** (Working Standard).

1. **Sensor Coupling Test:**
    - *Action:* Attach device to a machine. Tap the machine frame lightly with a metal tool.
    - *Observation:* The Envelope Detector value on the LCD should spike immediately, confirming the piezo is mechanically coupled to the chassis.
2. **Baseline Acquisition:**
    - *Action:* Run a full "Spin Cycle" in **LEARN Mode**.
    - *Validation:* The device must successfully generate a `.dat` file on the internal flash/SD card containing the mean FFT signature.
3. **Simulated Fault Test:**
    - *Action:* Attach a small eccentric weight (e.g., a magnet) to the washing machine drum to simulate an Unbalance Fault. Run in **MONITOR Mode**.
    - *Pass Criteria:* The device must detect the increased amplitude at the 1x RPM frequency and trigger a "High Vibration / Unbalance" alert

10. Wiring Diagram

10.1 System Interconnection

The device utilizes a modular wiring harness to connect the rigid PCB to the chassis-mounted components. This approach facilitates assembly and maintenance.

10.2 Harness Specifications

- **Power Input (JBat1):**
    - **Connection:** LiPo Battery to PCB.
    - **Wire Type:** 24 AWG Stranded, Twisted Pair.
    - **Purpose:** Twisting the VCC/GND wires minimizes the magnetic loop area, reducing the emission of magnetic interference from the battery current and improving immunity to external fields (Lecture 4).
    - **Polarity Protection:** Mechanical keying via the JST-XH connector.
- **Sensor Interface (JMic1):**
    - **Connection:** Piezoelectric Disc (Bottom Case) to PCB.
    - **Wire Type: RG-174 Coaxial Cable** (50Ω impedance).
    - **Shielding:** The center conductor carries the high-impedance signal. The outer braided shield is connected to the metal sensor diaphragm on one end and the PCB Analog Ground plane on the other. This creates a continuous Faraday shield protecting the weak vibration signal from motor noise.
- **User Interface (JDisplay1 & Buttons):**
    - **Display:** Connected via a 4-wire flat ribbon cable (VCC, GND, SDA, SCL). The ribbon configuration keeps the Clock (SCL) and Data (SDA) lines in a fixed geometry, stabilizing the I2C bus impedance.
    - **Control Buttons:** The "Scroll" and "Select" buttons are panel-mounted and connected via standard 2-wire leads to their respective headers on the PCB.

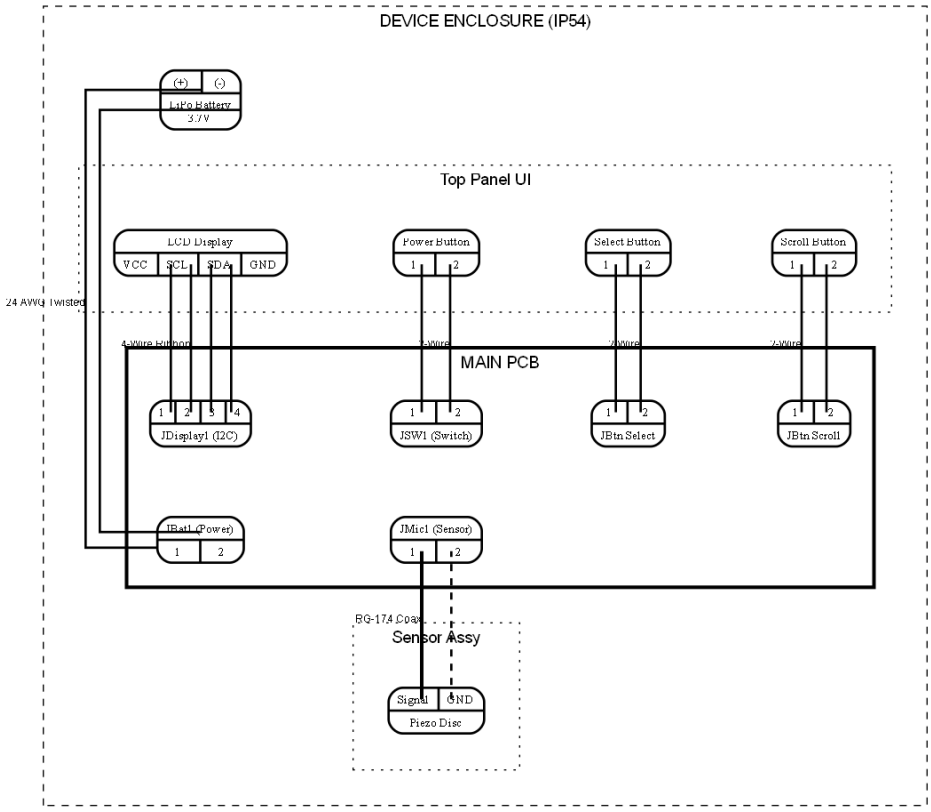


Figure: Wiring Diagram