Errata Note:

Corecell PCB #e539v01a
Reference Design

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1 Introduction

The original Corecell Reference Design, identified as PCB #e539v01a, was released before a power supply sequencing issue was identified. Semtech is actively working on a new version of the reference design, which will be called PCB #e539v02, to address the power sequencing issue and provide additional improvements on the power management. It is recommended that users implement the fix and improvements described in this application note in order to deliver an optimal solution.

It is recommended to read this application note in conjunction with the following documents:

• SX1302 Datasheet V1.1, issued in January 2020

• SX1302 Corecell reference design, PCB #e539V01a

Both are available on the Semtech website

2 Description of the Issue

The SX1302 LoRaWAN baseband IC requires two power supply rails:

- VCC_CORE = 1.2 V. This supplies the logic embedded in the chip
- VCC_IO = 3.3 V. This supplies the pad and pins, connecting the SX1302 to its companion devices, specifically the SX1250 from Semtech
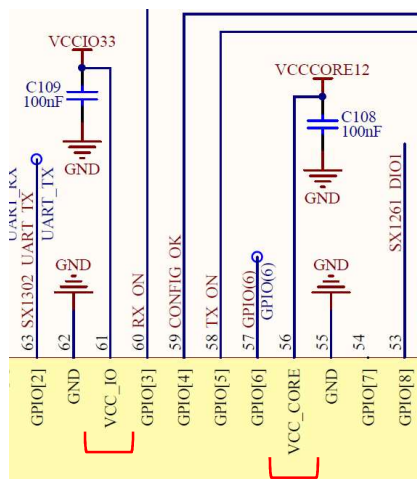

Figure 1: Dual Supply of the SX1302

The operation of SX1302 only starts when its logic is biased, and that only happens *after* VCC_CORE is available. Before then, no action is performed, and the entire SX1302 is kept in its default state.

Before VCC_CORE becomes available, all of the I/O pads would remain un-modified *at* logic level "0" until they are instructed otherwise by the core of the SX1302.

Due to some of the SX1302 I/Os which may be pulled-up externally on the reference design, *if* VCC_CORE is set *after* VCC_IO is settled, a conflict can happen on the corresponding I/O lines, leading to a short-circuit and uncontrolled in-rush current.

The in-rush current, which can be observed on the original PCB #e539v01a reference design, can peak at about 400 mA, and last only a few tens of microseconds. It may be an issue on gateway designs where the power supply cannot handle high-enough surges.

3 Recommended Corrections

The fix described below is implemented on PCB#e539V02a, and shall be applied to any design based on PCB#e539V01a.

3.1 Datasheet Recommendation

Section 5 of the SX1302 datasheet (Version 1.1) suggests the following VCC_CORE / VCC_IO sequence:

To ensure proper control of all digital IOs during the power-up and power-down sequences of the SX1302, VCC_CORE shall be enabled *before* VCC_IO at start-up, and disabled *after* VCC_IO at shut-down.
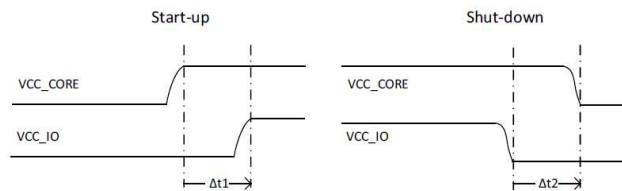
Figure 5-1: VCC_CORE and VCC_IO Sequencing

$\Delta t1$ and $\Delta t2$ must be equal to or greater than 0.

Figure 2: SX1302 Datasheet Extract

Note that the recommendation mostly concerns the start-up sequencing. At shut-down, energy storage will be quickly depleted, shutting down the complete board, so no specific measure is put in place to handle the shut-down process.

3.2 Proposed Correction

The power supply on the current reference design is implemented as follows:

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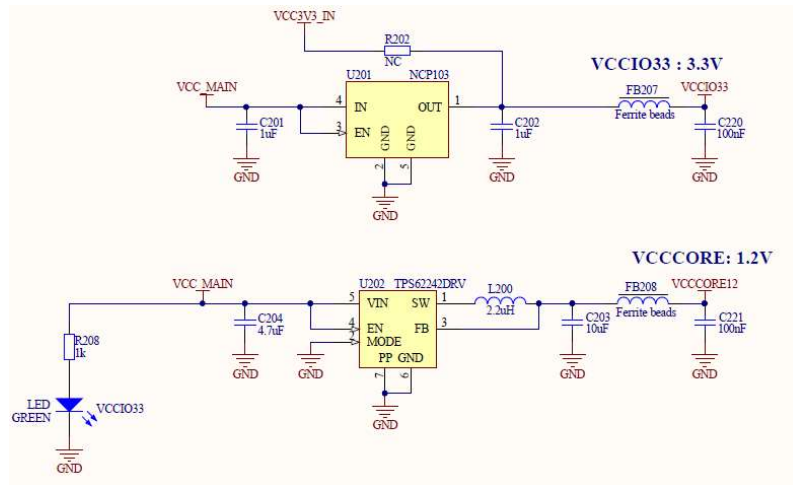Rev 1.0
April 2020

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Figure 3: PCB#e539V01a Power Supply

There are a few stuffing options, but the main idea is that both Regulators are supplied from VCC_MAIN, and therefore the time at which VCC_IO and VCC_CORE are available, isn't controlled as their EN pin is tied to VCC_MAIN, too.
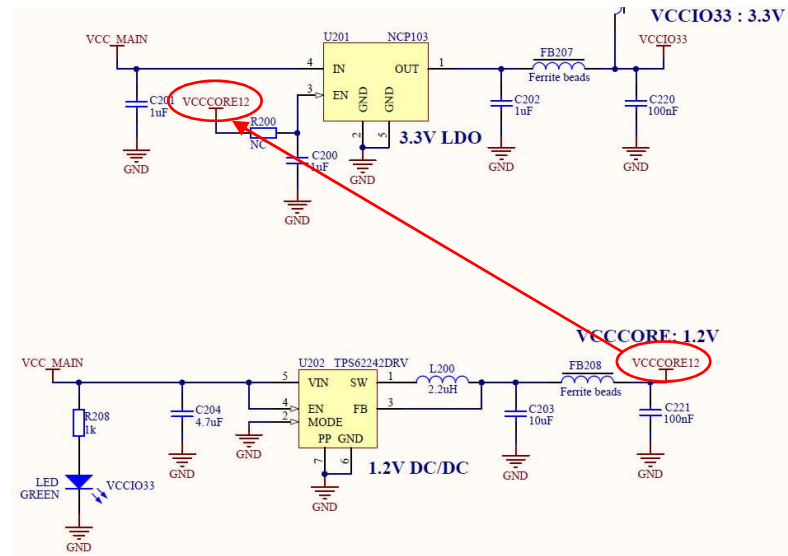

Figure 4: PCB#e539v02a Tentative Power Supply Change

The concept if the fix is fairly simple: ensure that VCC_CORE is available *before* the regulator used to generate VCC_IO is enabled (by its EN pin).

4 Revision History

Version	Date	Modifications
1.0	April 2020	First Release

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