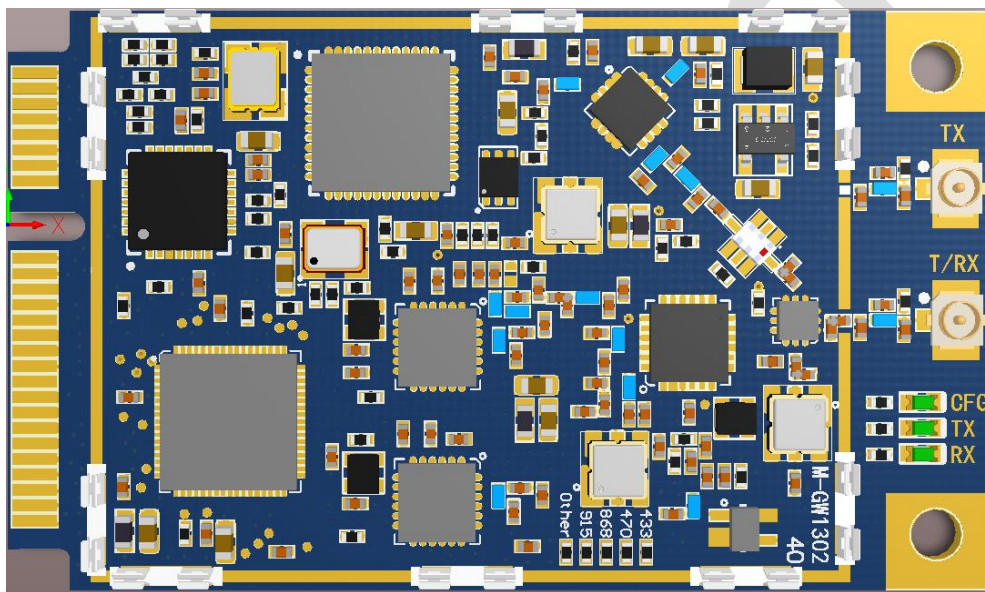


M-GW1302S PCI-e

Spec

V1.0



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1 General

1.1. Introduction

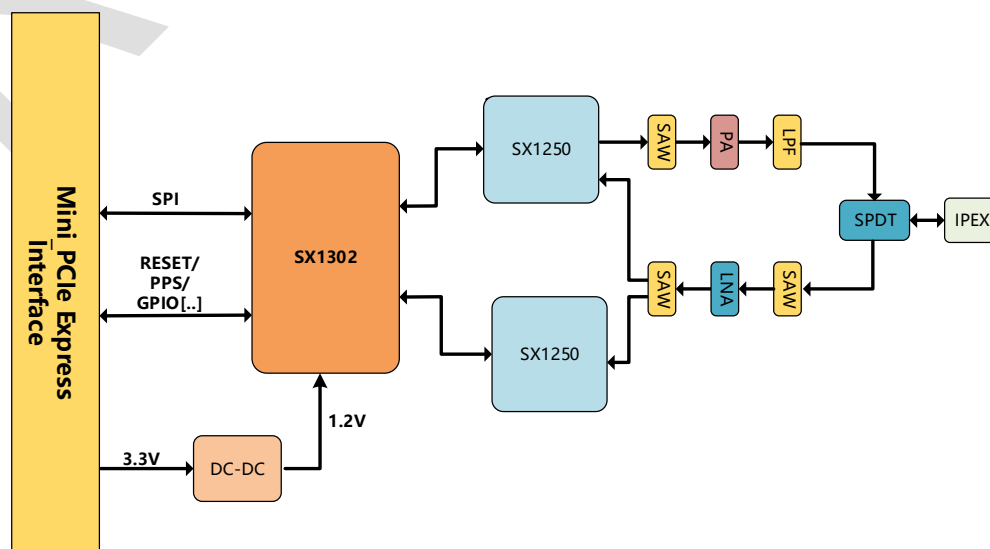
M-GW1302S is Mini PCI-e board based on SX1302, with SPI interface, internal PA and LNA, half-duplex design, for customer to develop LoRa gateway quickly.

SX1302 is the newest LoRa gateway chip that Semtech released, with SX1250 as RF front-end chip, supporting SF5-SF12, compared with SX1301, SX1302 has higher data communication speed rate and lower power consumption, simpler design and higher performance.

1.2. Main Features

- PCI Express Mini Card 1.2 standard interface
- Max TX 360mA, Max RX 60mA
- I-PEX Antenna, Harf-duplex Communication
- Standard SPI interface
- 8 RX channels, SF5~SF12, RX sensitivity down to -141dBm
- 1 TX channel, Max TX Power up to 26dBm
- ISM Frequency: EU433, CN470, EU868, US915
- Open-source Raspberry Pie-based evaluation test board is available

1.3. Diagram of the Module



Pic 1: Module Diagram

2. Interface

2.1. Interface Definition

M-GW1302S is based on standard Mini PCI Express interface as below:

Chart 1: IO parameter

Name	Description
DI	Data Input
DO	Data Output
IO	Bidirectional input-output
PI	Power In

Chart 2: Definition of main function pins

Name	Description
GND	4,9,15,18,21,26,27,29,34,35,37,40,43,50
3.3V	2,24,39,41,52
PPS	19
NRESET	22
RX_ON	42
TX_ON	44
CFG_ON	46
SX_SCK	45
SX_MISO	47
SX_MOSI	49
SX_CSN	51

Chart3: Pin Details

No.	Mini PCIe	M-GW1302S	I/O	Description	Note
1	WAKE#	RESERVED	DO	Pass through only, Keep dangling	
2	3.3Vaux	VCC_3V3	PI	3.3V DC power input	
3	COEX1	NC	—	Internal use, Keep dangling	

4	GND	GND	—	Ground	
5	COEX2	NC	—	Internal use, Keep dangling	
6	1.5V	NC	—	No use	
7	CLKREQ#	NC	—	Internal use, Keep dangling	
8	UIM_PWR	NC	—	No use	
9	GND	GND	—	Ground	
10	UIM_DATA	RESERVED	IO	Pass through only, Keep dangling	
11	REFCLK-	RESERVED	DI	Pass through only, Keep dangling	
12	UIM_CLK	RESERVED	IO	Pass through only, Keep dangling	
13	REFCLK+	RESERVED	DO	Pass through only, Keep dangling	
14	UIM_RESET	NC	—	No use	
15	GND	GND	—	Ground	
16	UIM_VPP	NC	—	Internal use, Keep dangling	
17	RESERVED	NC	—	Internal use, Keep dangling	
18	GND	GND	—	Ground	
19	RESERVED	PPS	DI	GPS time input	Dangling Optional
20	W_DISABLE#	NC	—	Internal use, Keep dangling	
21	GND	GND	—	Ground	
22	PERST#	NRESET	DI	Reset	High level reset
23	PERn0	RESERVED	DI	Reserved, keep dangling	
24	3.3Vaux	VCC_3V3	PI	3.3V DC power input	
25	PERp0	NC	—	No use	
26	GND	GND	—	Ground	
27	GND	GND	—	Ground	

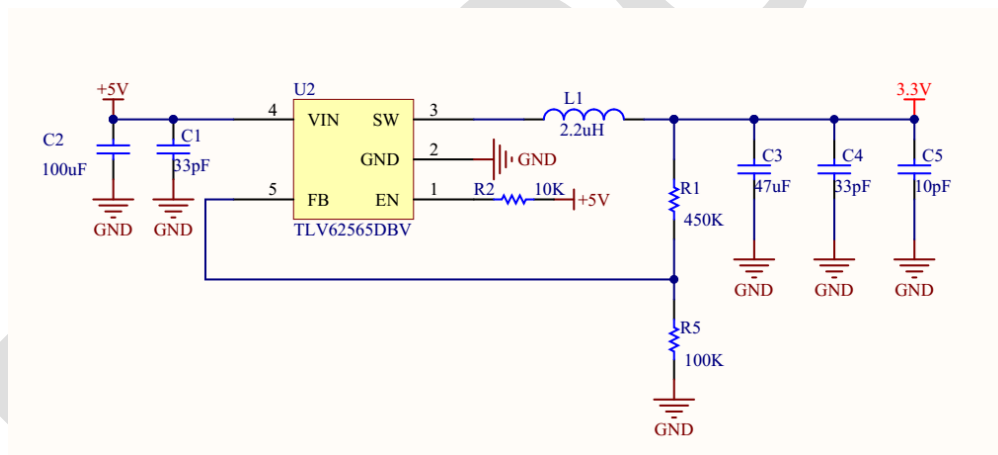
28	1.5V	NC	—	No use	
29	GND	GND	—	Ground	
30	SMB_CLK	NC	—	Internal use, Keep dangling	
31	PETn0	RESERVED	DO	Reserved, keep dangling	
32	SMB_DATA	NC	—	Internal use, Keep dangling	
33	PETp0	NC	—	No use	
34	GND	GND	—	Ground	
35	GND	GND	—	Ground	
36	USB_D-	RESERVED	IO	Pass through only, Keep dangling	
37	GND	GND	—	Ground	
38	USB_D+	RESERVED	IO	Pass through only, Keep dangling	
39	3.3Vaux	VCC_3V3	PI	3.3V DC power input	
40	GND	GND	—	Ground	
41	3.3Vaux	VCC_3V3	PI	3.3V DC power input	
42	LED_WWAN#	RX_ON	DO	RX indicator, connect LED	
43	GND	GND	—	Ground	
44	LED_WLAN#	TX_ON	DO	TX indicator, connect LED	
45	RESERVED	SX_SCK	DI	SPI time input	
46	LED_WPAN#	CFG_ON	DO	CFG indicator, connect LED	
47	RESERVED	SX_MISO	DO	SPI date output	
48	1.5V	NC	—	No use	
49	RESERVED	SX_MOSI	DI	SPI data input	
50	GND	GND	—	Ground	
51	RESERVED	SX_CSN	DI	SPI data input	
52	3.3Vaux	VCC_3V3	PI	3.3V DC power input	

2.2. Power Interface

Chart 4: Power Interface Definition

	Pin No.	IO	Description
GND	4,9,15,18,21,26,27,29,34,35,37,40,43,50		
3.3V	2,24,39,41,52	PI	3.3V Power Input

M-GW1302S power on with DC 3.3V, Max TX current can reach 400mA. In order to prevent voltage drop, the switching power supply or LDO used shall be able to provide sufficient current, and a tantalum capacitor or electrolytic capacitor with large capacitance value shall be added at the module power supply port. If the switching power supply is used to supply power to the module, the circuit wiring shall avoid the antenna as far as possible to prevent EMC interference.



Pic 2: DC-DC Reference Design

2.3. SPI Interface

M-GW1302S SPI interface definition as below:

Chart 5: SPI interface definition

Name	Pin No.	I/O	Description	Voltage
SX_SCK	45	DI	SPI time input	3.3V
SX_MISO	47	DO	SPI data output	3.3V
SX_MOSI	49	DI	SPI data input	3.3V
SX_CSN	51	DI	SPI signal input	3.3V

If you want full-duplex communication, please refer to SX1302 datasheet.

2.4. Signal Control

Chart 7: Signal control interface definition

Name	Pin No.	I/O	Description	Voltage
PPS	11	DI	GPS time input	3.3V
NRESET	13	DI	Reset	3.3V
RX_ON	42	DO	RX indicator	3.3V
TX_ON	44	DO	TX indicator	3.3V
CFG_ON	46	DO	CFG indicator	3.3V

2.4.1. PPS Signal

Support gps-pps input for receiving data packets with time stamps.

2.4.2. NRESET Signal

External control circuit can realize module reset. Pull up the NRESET interface level for 0.05 ~ 0.2S and release it to reset the module. NRESET signal is sensitive to interference. The routing on the module interface board shall be as short as possible and processed in a packet.

2.4.3. RX_ON Signal

When the module is in the receiving state, the pin outputs high level, and the on-board LED is on, which is connected to the GPIO of SX302.

2.4.4. TX_ON Signal

When the module is sending data, the pin outputs high level, and the on-board LED is on, which is connected to the GPIO of SX1302.

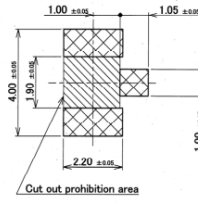
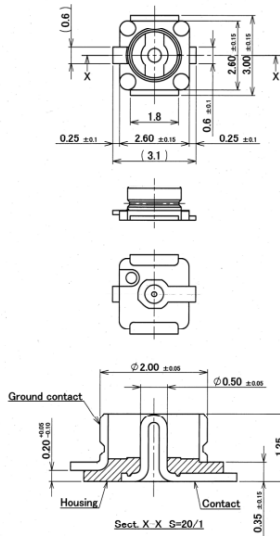
2.4.5. CFG_ON Signal

When the module successfully configures parameters, the pin outputs high level, and the on-board LED is on, which is connected to the GPIO of SX1302.

3. Antenna Interface

The antenna of this module is based on I-PEX 1 as below:

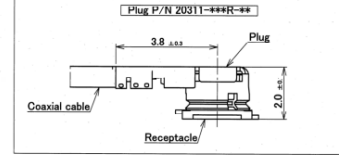
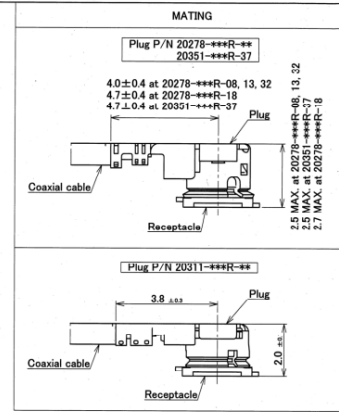
Recommended P/N	20279-001E-03	
PART No.	Packing reel	Quantity
20279-001E-01	Plastic reel	2,500
ZUZ19-001E-03	Plastic reel	5,000
20279-001E-05	Plastic reel	10,000



RECOMMENDED FOOTPRINT PATTERN

Notes.

- Material
 - Housing: Heat resisting plastics, UL94V-0, White
 - Contact: Copper alloy; Au plating
 - Ground Contact: Copper alloy; Au plating
- Coplanarity: 0.1mm MAX.
- Packing: Embossed taping
- Mating Partner Part No.:
 - 20279-***R-**
 - ZU331-***R-3/
 - ZU311-***R-**
- This is "Pb-free" connector.
- RoHS compliant.



PROJECTION	SERIES No.	CUSTOMER COPY
MHF [®] 1 RECEPTACLE	R0	
SCALE: 10:1 UNIT: mm		
DATE: 20279	A3	REV: 1/1 REV: 21

Pic 3: Size of RF Connector

4. Interface Electrical and RF Performance

4.1. Power Interface

M-GW1302S is powered on DC 3.3V, input voltage is 3.3V±9%, input current is min 500mA, power requirement as below:

Chart 8: Power input

Para	Description	Min	Typical	Max	Unit
VCC	Power voltage	3.0	3.3	3.6	V

4.2. IO Interface

M-GW1302S IO interface as below:

Chart 9: IO Interface

Parameter	Description	Min	Max	Unit
VIH	High voltage input	0.7*VCC	VCC+0.3	V
VIL	Low voltage input	-0.3	0.3*VCC	V
VOH	High voltage output	VCC-0.5	VCC	V

VOL	Low voltage output	0	0.4	V
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4.3. Working Currency

Chart 10: Working Currency

Parameter	Condition	Typical Value	Unit
RX	RX only, no TX	54	mA
TX/RX	RX and TX@25dBm	360	mA
IDLE	Idle mode	27	mA

4.4. RF Performance

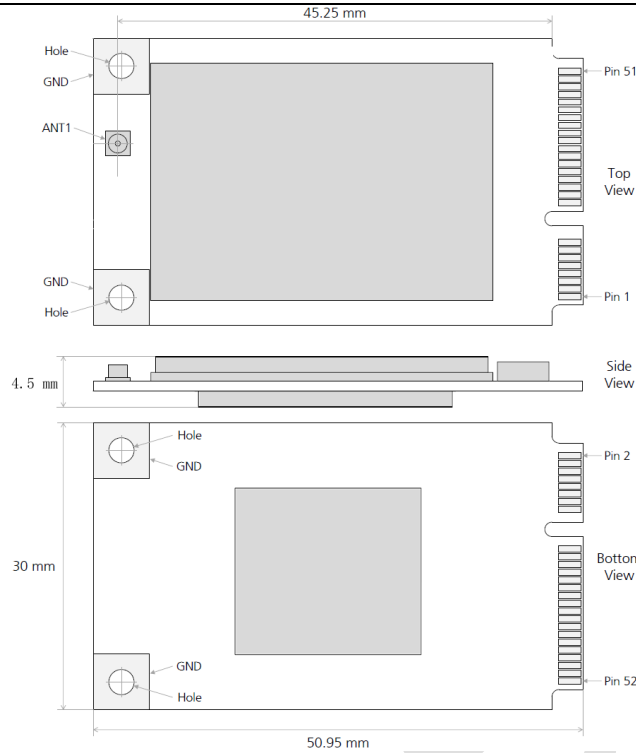
Chart 11: TX Power

ISM Frequency	Power	Unit
505.5MHz	26	dBm
868.5MHz	TBD	dBm
915.5MHz	TBD	dBm

Chart 12: RX Sensitivity

ISM Frequency	SF(BW=125KHZ)	RX Sensitivity(dBm)
475.5MHz	SF=5	-121
	SF=7	-127
	SF=12	-141
868.5MHz	SF=5	TBD
	SF=7	TBD
	SF=12	TBD
915.5MHz	SF=05	TBD
	SF=07	TBD
	SF=12	TBD

5. Size



Pic 4: M-GW1302S Size

Any connector based on standard PCI Express Mini Card can connect to this module M-GW1302S, below for your reference is 679100002 connector from Molex

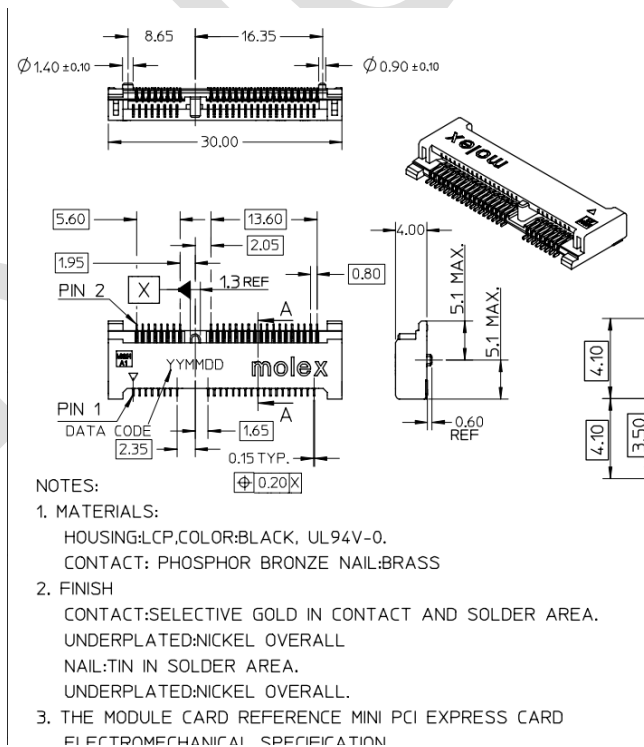
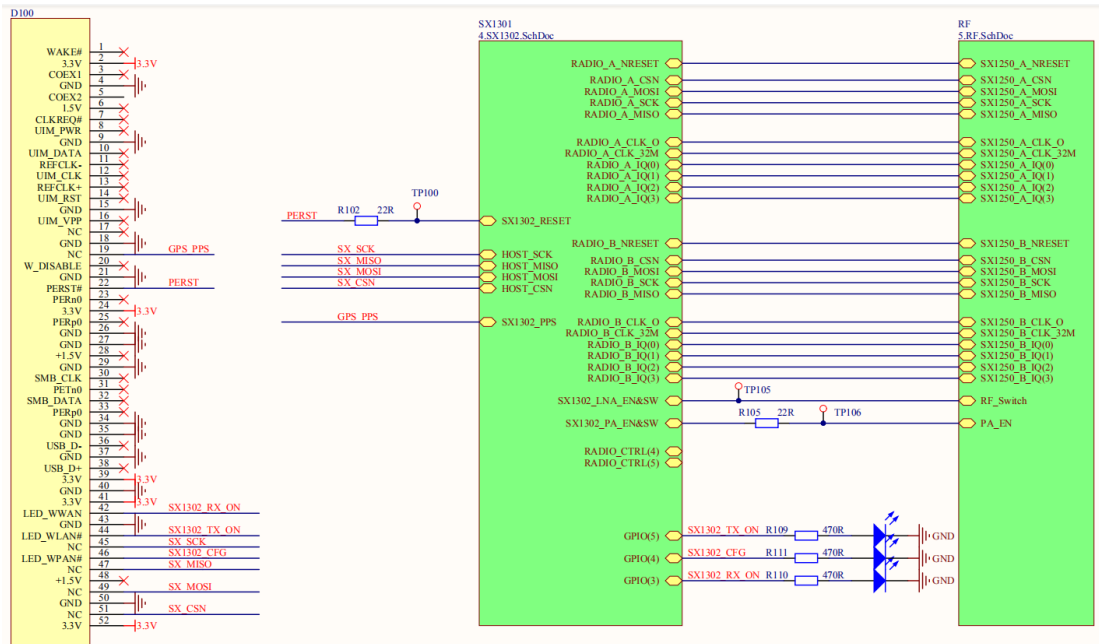


Chart 5: Mini PCI Express Connector

6. Internal Connection

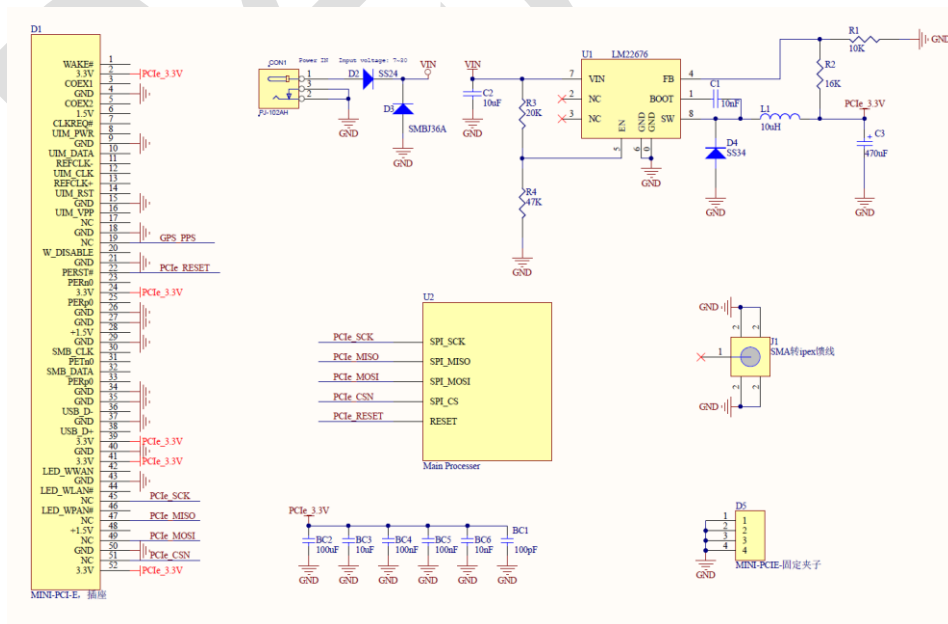
Below picture is the internal connection of M-GW1302S for reference:



Pic 6: M-GW1302S internal connection

7. Reference Design

M-GW1302S connect to main board through SPI interface, powered on through DC-AC module, customer can change accordingly to your applications.



Pic 9: M-GW1302S Reference Design