

Performance Results

In this section, you are required to configure your corrected code to run in the Quartus tool. Using the Timing Analyzer (as discussed during the training phase), you will need to create a clock and specify timing constraints suitable for your processor. You are free to apply any constraints you deem appropriate.

After completing the analysis, report the performance metrics and required data in the table below. Additionally, provide the necessary commands from the Synopsys Design Constraints (SDC) file.

Table 1 Performance Data

| | | Metric | Value | Description |
|-------|----------|------------------|------------|---|
| | | Clock Frequency | 29.41 Mhz | clock frequency you configured in the Quartus tool. |
| | | Design Size (LE) | 1910 | Size of design in terms of logic elements |
| model | Slow 85C | Fmax | 30.93 Mhz | Fmax : The highest frequency at which the processor can operate reliably. |
| | | Setup Slack | +0.835 ns | |
| | | Hold Slack | +1.118 ns | |
| | Slow 0C | Fmax | 32.81 Mhz | Setup Time : The time required to set up signals before the clock edge. |
| | | Setup Slack | +1.763 ns | |
| | | Hold Slack | +1.059 ns | |
| | Fast 0C | Fmax | 82.64 Mhz | Hold Time : The minimum time signals must remain stable after the clock edge. |
| | | Setup Slack | +10.950 ns | |
| | | Hold Slack | +0.388 ns | |

Provide the commands from your **SDC file** that define the clock and timing constraints.

```
set_time_format -unit ns -decimal_places 3
create_clock -name {clk} -period 34.000 -waveform { 0.000 17.000 } [get_ports {clk}]
set_clock_uncertainty -rise_from [get_clocks {clk}] -rise_to [get_clocks {clk}] 0.020
set_clock_uncertainty -rise_from [get_clocks {clk}] -fall_to [get_clocks {clk}] 0.020
set_clock_uncertainty -fall_from [get_clocks {clk}] -rise_to [get_clocks {clk}] 0.020
set_clock_uncertainty -fall_from [get_clocks {clk}] -fall_to [get_clocks {clk}] 0.020
```