Princess Sumaya University for Technology
Computer Engineering Department
Digital Logic Lab
Final Project – Fall 2023

Due Date: 14/1/2024

Project Description:

Implement the transmitter/receiver circuit shown in Figure 1 using Verilog. The circuit can be implemented using any type of model (Behavioral, structural …etc) and should meet the following requirements:

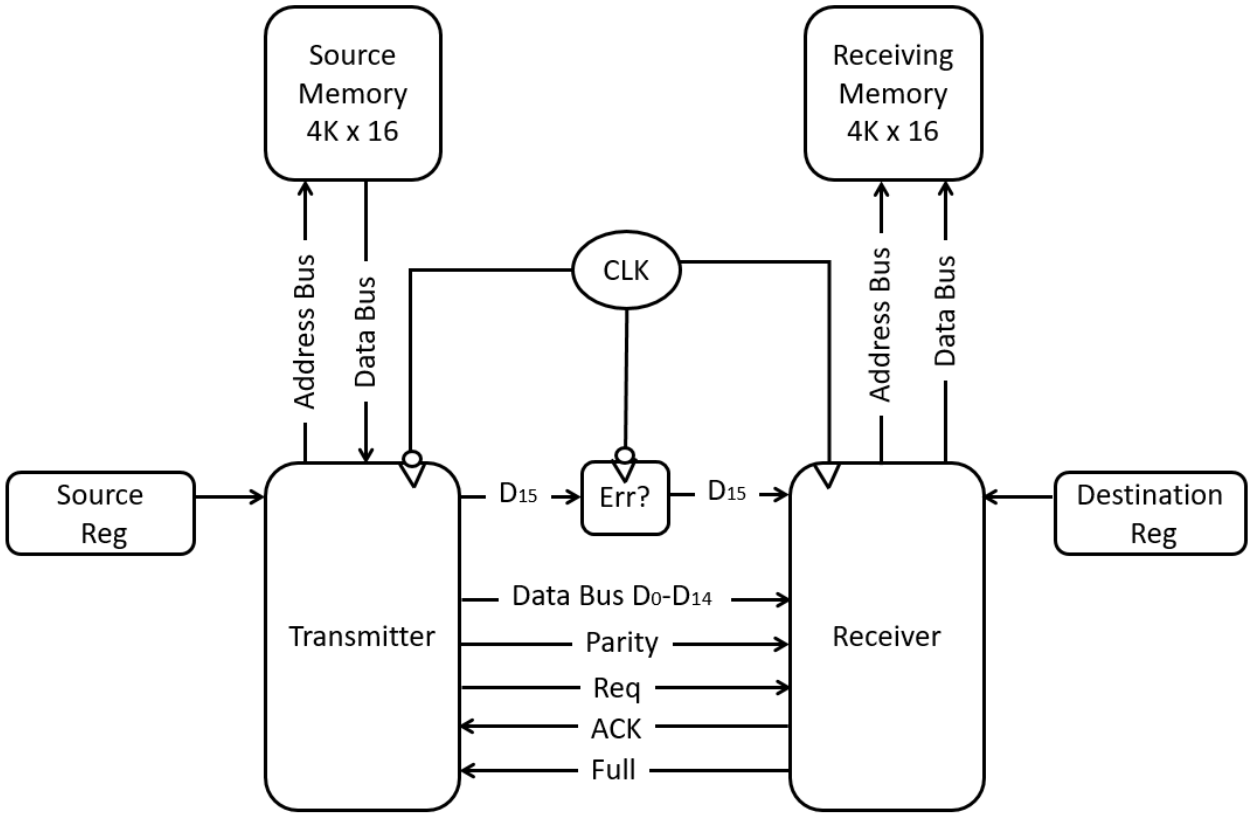

Figure 1. Circuit Diagram

The circuit's functionality: In this circuit, the transmitter reads data from the source memory and sends it to the receiver, which is responsible for storing the data in the receiving memory.

Design Requirements:

1. The starting address of where to read the data is stored in Source Reg.
2. The starting address of where to store the data is stored in Dest. Reg.
3. The copy should stop when it reaches this special data pattern = $FFFF_h$. It should copy it, then stop.

4. The transmitter operates on the negative edge, while the receiver operates at the positive edge.
5. The transmitter prepares an EVEN parity bit and sends it with the data.
6. The **Err?** Block receives one bit and outputs one bit immediately (i.e. it does not wait for the clock). The block **sometimes** flips the input bit to introduce error in the data transmission, while other times it does not. Students can pick whatever method to implement this. The clock connected to the block is just to change the state of the block.
7. If the transmitter reaches the last address (4095), it should stop.
8. The receiver should include a parity checker inside it.
9. If the receiver reaches the last address, it should raise the Full flag, and consequently, the transmitter would stop.
10. The circuit should follow the following transmission sequence:

    Transmission Sequence:

    - When there is no data, the REQ flag will be Zero.
    - When the transmitter sends data, it sets the REQ flag to 1.
    - At the positive edge, the receiver should check if there is data. It should also implement an even parity checker to see whether the data is valid.
        - If the data is valid, it is stored in the Destination memory, and the Ack is set to 1.
        - If the data is invalid, it is dropped, and the Ack is left at zero.
    - The transmitter needs to check the ACK and the full flag to decide if it needs to resend the old data, send new data, or stop if it is finished or the receiver is full.

What to submit:

- All Verilog Files and test bench(es).
    - The test bench(es) shall include all the functionality described above.
- A full Report detailing the design