A Literature Survey on CMOS Power Amplifiers

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Abstract: In this paper, various design techniques of CMOS power amplifiers are analyzed. For several highly integrated wireless Silicon CMOS transmitters and transceivers with many different configurations, the Power amplifier (PA) is an significant building block. For tight integration with other wireless building blocks, CMOS power amplifiers (PAs) can be built. The various design techniques are compared with respect to parameters like output power, technology used, gain obtained, frequency of operation, PAE (power added efficiency), and number of transistors and transformers used etc. The obtained parameters are then compared using a table and various parameters of different designs are plotted graphically for comparison. These comparison results would provide any designer with hands on data to select the best possible design of a CMOS amplifier suitable for the required application.

Keywords: Power amplifiers, CMOS, NMOS, transformer, transistors, power added efficiency

1. INTRODUCTION

Power amplifiers have become an important piece of most electronic equipment, which were generally being developed from pentavalent & trivalent doped silicon compound semiconductors because of the high linearity and breakdown voltage. Furthermore, because the compound semiconductor process provides a through-hole through which the back-metal layer can be used as a ground plane, a high-quality ground level may be accomplished using compound

semiconductor power amplifiers. Most conventional power amplifiers have been equipped with a single-ended configuration, thanks to the high-quality ground level in compound semiconductors.

CMOS technology allows operation at a lower power supply, resulting in reduced circuit power dissipation and a decreased manufacturing cost due to the compact chip size. CMOS provides the prospect of low-cost integration of radiofrequency (RF)/digital / analog functions into a single chip. The CMOS power amplifier is a promising approach to meet the demands of low-power and low-cost design for modern wireless devices. Throughout the years, CMOS power amplifiers have been commonly used in various wireless communications applications, including home control, radio frequency identification (RFID), industrial consumer electronics, TV broadcasts, telephones, and medical devices. To trigger ultrasonic transducers, it has been implemented in high-frequency medical ultrasonic applications to amplify high-voltage excitation signals, since ultrasonic imaging requires a higher contrast resolution, which can be provided by a highly linear power amplifier.

2. DIFFERENT DESIGNS OF CMOS POWER AMPLIFIER

2.1 Differential 2.4-GHz CMOS power amplifier using stacked NMOS, transformer, and PMOS structures to enhance reliability

In this study, a power amplifier is proposed to boost the efficiency of CMOS power amplifiers using a stacked NMOS, transformer, and PMOS structure. The amplifier's power stage is split into NMOS and PMOS amplifier stages to regulate the peak voltages at each NMOS and PMOS drains. In the transformer, which has 2 primary parts and 1 secondary component, the power produced at the 2 amplifier stages is combined. For IEEE 802.11n WLAN applications a 2.4-GHz differential CMOS power amplifier is built with a modulation of 64 quadrature amplitude, a peak

to average power ratio of 9.6 dB and a bandwidth of 20 MHz to control the functions of the system. The model power amplifier is manufactured using the RF CMOS method of 180-nm silicone-on-insulator. Since the PMOS mobility is lower than that of the NMOS, the PMOS' gate width is usually configured to be greater than that of the NMOS to equalize the PMOS DC current with the NMOS one. A power amplifier using a stacked NMOS, transformer, and PMOS system was proposed to increase the efficiency of the CMOS power amplifier. The power stage was split into 2 amplifier stages, which had been stacked using the proposed structure. One stage consisted of the transformer and NMOS, and the other, the transformer and PMOS. Additionally, constructed the transformer with 2 primary parts and 1 secondary part to divide the power stage into 2 amplifier stages independently. As a result, the efficient supply voltages of the 2 amplifier stages have been decreased and hence the voltage swings at the NMOS and PMOS drains have been decreased. Consequently the CMOS power amplifier's reliability improved.

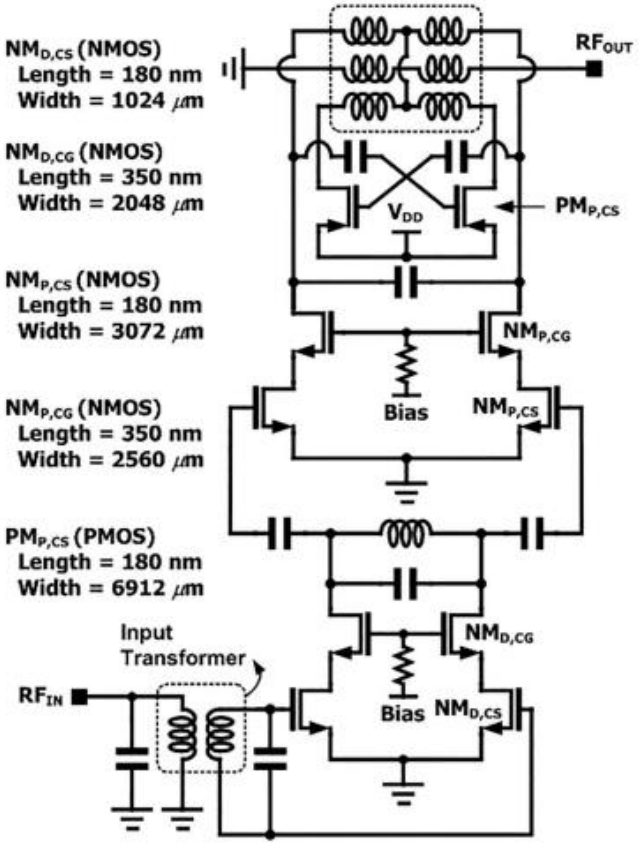

Figure 1: Schematic of the designed CMOS power amplifier

2.2 A CMOS power amplifier using a split cascode structure to enhance efficiency:

In this design, the efficiency of RF CMOS Power amplifiers is increased by using a cascaded structure. A common gate transistor was split into two parts to increase the efficiency in the low-output-power region. The feasibility of this design is tested by using the 180-nm RF CMOS method to build a 2.2-GHz CMOS power amplifier. During the low-output-power operation of the power amplifier, one of the common-gate transistors is turned off to realize the low-power mode and hence increase the efficiency. For a WCDMA modulated signal, an output power of 23.4 dBm (max) with an added efficiency (PAE) of 20.8% is obtained. At 16 dBm output power the PAE is improved by the engineered power amplifier's mode shift. Chip size of the designed amplifier is 2.1 x 0.86 mm^2. A WCDMA modulated signal at a carrier frequency of 2.2 GHz is used to measure the performance of the power amplifier. Obtained gain is 22dB for low power mode and 19dB for high power mode respectively. It gives good gain and output power and uses a comparable number of transistors when compared with other designs.

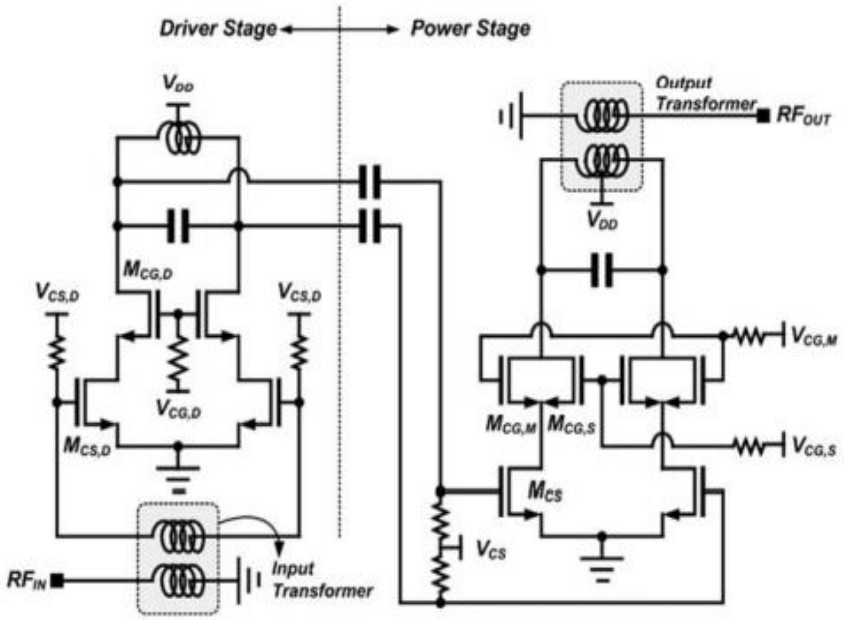

Figure 2: Simplified schematic of the designed split cascode CMOS power amplifier

2.3 An X-band CMOS power amplifier with a driver stage using a shot through rejection technique:

In this design, 0.13-lm RF CMOS process is used. The power amplifier is composed of power stages and drivers. This design mainly focuses on power consumption of the driver stage. A shot-through current rejection technique for the Class-D amplifier which is used as a driver stage of the CMOS power amplifier is proposed to reduce power consumption. The Class-D amplifier's NMOS and PMOS gate bias is split using DC-blocking capacitors to regulate the current from the shot through. The proposed class D amplifier is used as the driver stage of the power amplifier. 0.13-lm RF CMOS technology is used to design the amplifier.

Power added efficiency (PAE) obtained is 26%. The dimensions of the amplifier are 840 x 90 mm^2. Gain obtained is 17dB. The frequency at which results are measured is 12GHz. The measured results for the shot-through current of the proposed Class D amplifier is lower than that of the typical Class-D amplifier Hence, the proposed design fulfills our aim.

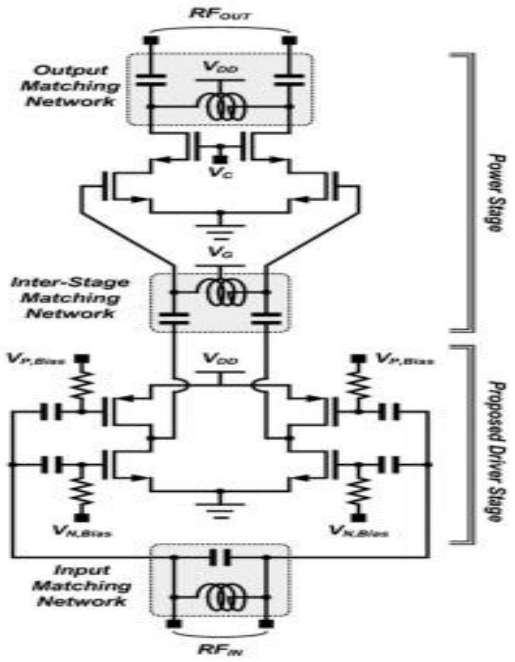

Figure 3: Schematic of the designed X-band CMOS power amplifier

2.4 A CMOS power amplifier using a balun embedded driver stage for IEEE 802.11N WLAN applications

In this design, a balun embedded driver stage is used to enhance the bandwidth and minimize the chip size of a differential CMOS power amplifier. For the function of the input balun we connect the the gate of the PMOS to the drain of NMOS. To verify the feasibility of the proposed balun embedded driver stage, a differential CMOS power amplifier for 5-GHz IEEE 802.11n WLAN applications is designed. The designed power amplifier is fabricated using process of the 180-nm SOI RF CMOS. The measured 3-dB bandwidth is obtained as 2.5 GHz. 0.885 mm^2 is the chip size of the designed fully integrated power amplifier including input and output matching networks and test pads. The measured maximum output power is 20.18 dBm with PAE of 10.16%. To improve amplifier bandwidth and to minimize the chip size, a CMOS power amplifier with an active balun is designed. The proposed balun embedded driver stage acts as a driver stage for the power amplifier as well as acting as the input balun. By removing the bulky input transformer, the chip size of the designed power amplifier can be reduced compared to that of a typical differential CMOS power amplifier. The bandwidth of the power amplifier with the proposed Balun embedded driver stage is also improved.

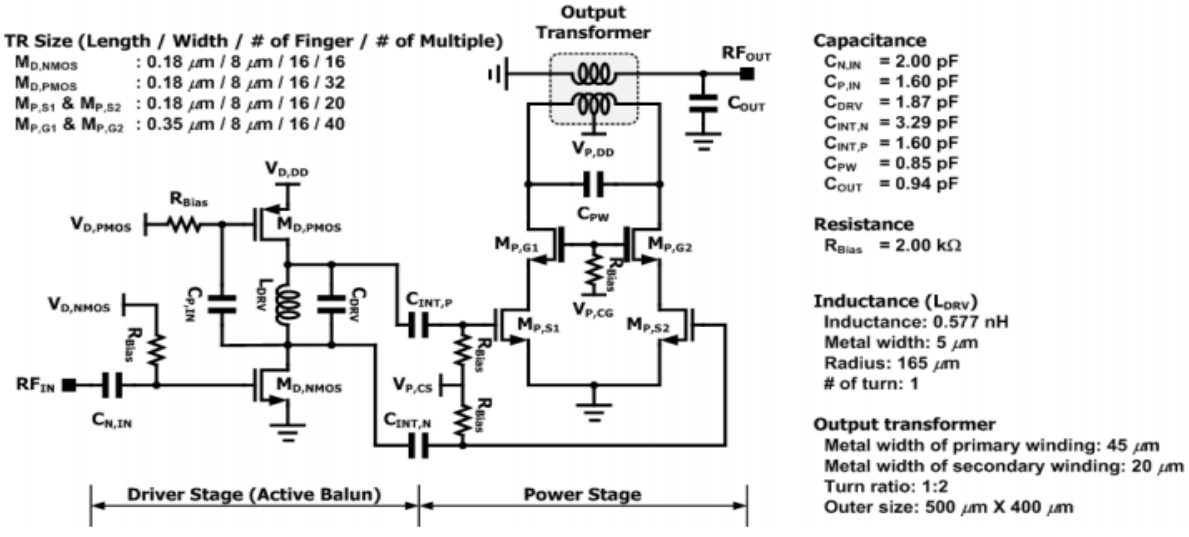

Figure 4: Schematic of the proposed differential CMOS power amplifier using a Balun embedded driver stage

2.5 Design of a 60-GHz High-Output Power Stacked FET Power Amplifier Using Transformer-Based Voltage-Type Power Combining in 65-nm CMOS

A 60-GHz transformer (TF)-based voltage-type-combined single-stage stacked field-effect transistor power amplifier is demonstrated using a 65-nm CMOS process. A stacked-FET structure is utilised in the PA design to overcome the low breakdown voltage limit of MOSFETs. The TF-based voltage-type combiner is used having 0.9-dB insertion loss and a compact size of 0.023 mm^2. The additional output balun is used to transform the differential output of the voltage-type combiner to the single-ended output for testing consideration. The TF-based voltage-type-combined structure is capable of multiple distributed push–pull circuits in a polygon geometry. It is an efficient method of impedance transformation and power combining to obtain a high-output power while maintaining an acceptable power efficiency. The stacked-FET topology can overcome the low breakdown voltage of short channel MOS transistors and increase the output power of PA by enhancing the supply voltage of the devices. It uses more transistors and has poor gain when compared with the rest.

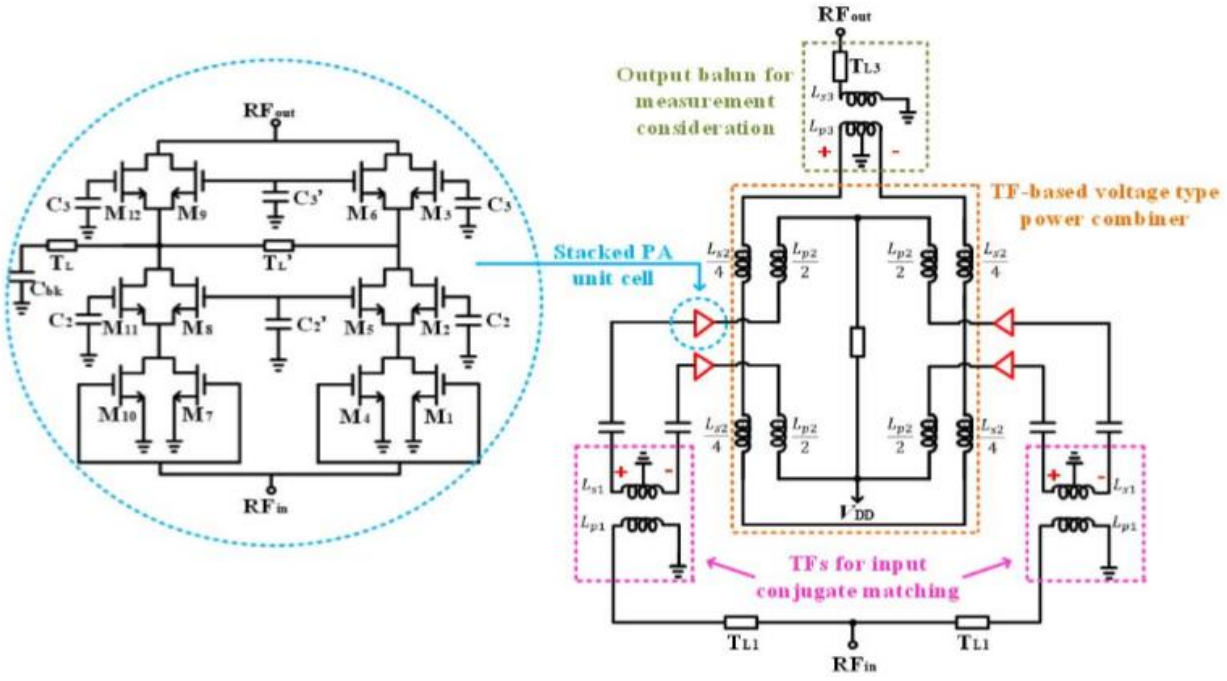

Figure 5: Complete circuit schematic of the proposed stacked-FET PA

2.6 Class-O: A Highly Linear Class of Power Amplifiers in 0.13µm CMOS for WCDMA/LTE Applications

A conceptual block diagram of the Class-O PA is shown in figure below. The Class-O PA consists of two power-amplifying devices, a linearizing device and a gain-boosting device. Their output currents are summed in-phase into the common load of the Class-O PA. Depending on the type and configuration of the used power devices, their drive signals can be either differential or common mode. The output voltage signal in a Class-O PA is fed back to the first amplifying device, adjusting in real-time the magnitude and the phase of its own current according to the difference between its input and output voltage signals. The second device acts as an efficient power and power-gain booster, so that the parallel configuration of power-amplifying devices 1 and 2 can achieve the required power, gain and linearity even at high average power (P_{avg}). Compared to a canonical feedback amplifier, the advantage of the proposed Class-O operation is a considerably reduced voltage stress across the power-amplifying devices. The implemented circuit, without any predistortion or additional linearization circuitry, demonstrates the potential of the proposed Class-O operation mode, which provides high linearity together with improved ruggedness for compact sized high-power CMOS PAs. It uses less transistors and has a very good power added efficiency as well as high output power compared with the rest. The only downside is it has a small gain without the use of power and power gain boosters but nevertheless has very high output power in the end.

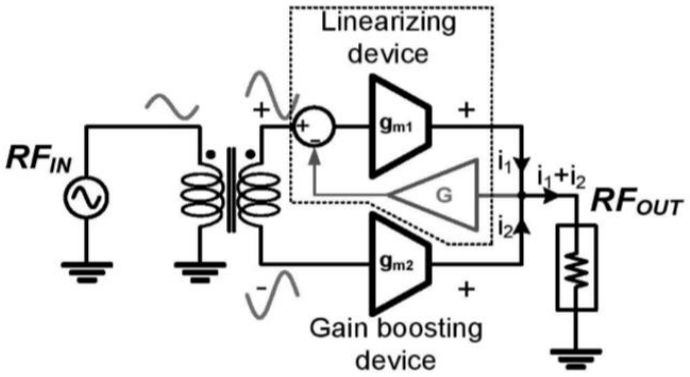

Figure 6: Conceptual Class-O power-amplifier block diagram

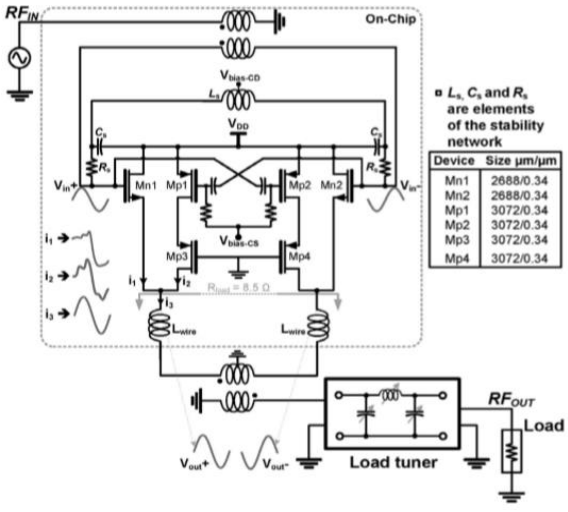

Figure 7: Schematic of the Class-O power-amplifier implementation in CMOS

2.7 60 GHz CMOS Amplifiers Using Transformer Coupling and Artificial Dielectric Differential Transmission Lines for Compact Design

In this design, we utilize 57–65 GHz differential and transformer-coupled power and variable-gain amplifiers using a commercial 90 nm digital CMOS process. On-chip transformers combine bias, stability and input/inter stage matching networks to construct compact designs. Also, balanced transmission lines having artificial dielectric strips help in providing substrate shielding and in increasing the effective dielectric constant up to 54 which in turn reduces the size. Thus, the designed three-stage power amplifier occupies only an area of only 0.15 mm^2. The power amplifier is implemented in differential circuit architecture, and utilizes on-chip transformers and artificial dielectric transmission lines to accomplish a compact design. The design is shown to be stable and repeatable and has less gain when compared with the rest.

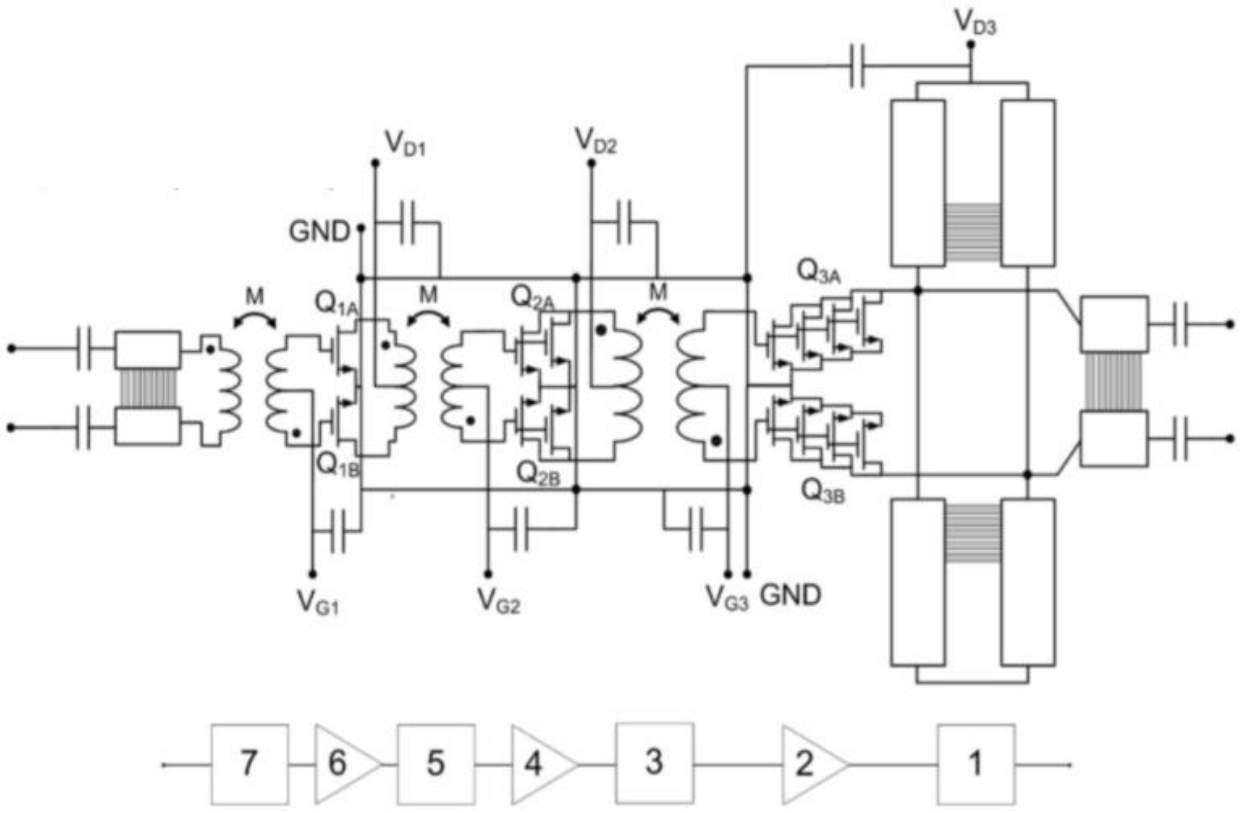

Figure 8: Circuit schematic of differential, transformer coupled CMOS power amplifier

2.8 Linear CMOS power amplifier using continuous gate voltage control

A linearization technique using a gate voltage adaptation of a common gate stage for a cascade CMOS power amplifier (PA) is presented. The tracking of minimum in-band third-order intermodulation distortion by controlling with respect to instantaneous power level enhances the linearity of CMOS PA over a wide range of operation levels. The results show that the CMOS PA with proposed scheme has an overall efficiency of 34.6% and a gain of 25.8 dB at an average output power of 27 dBm.

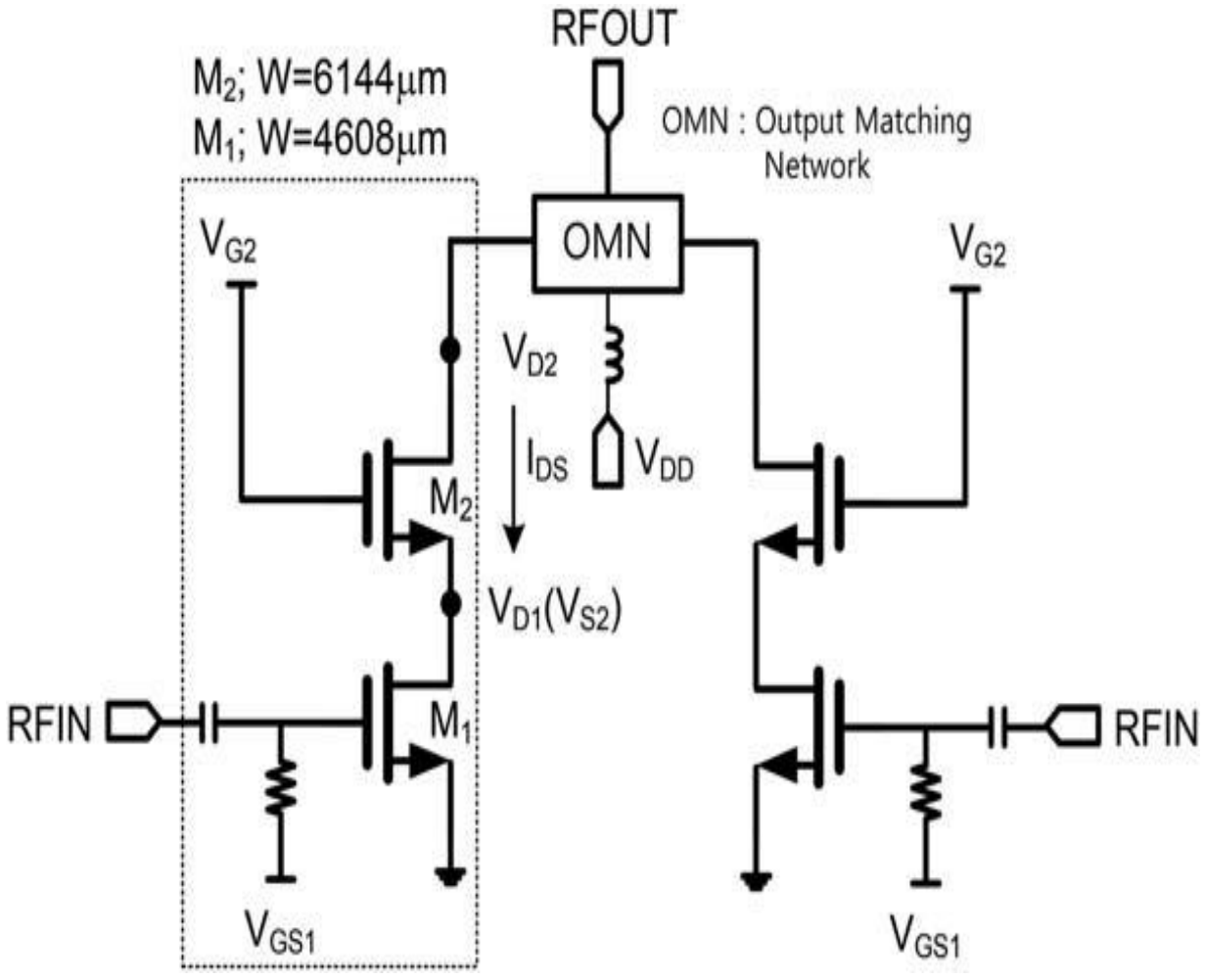

Figure 9: Schematic of the cascode amplifier stage

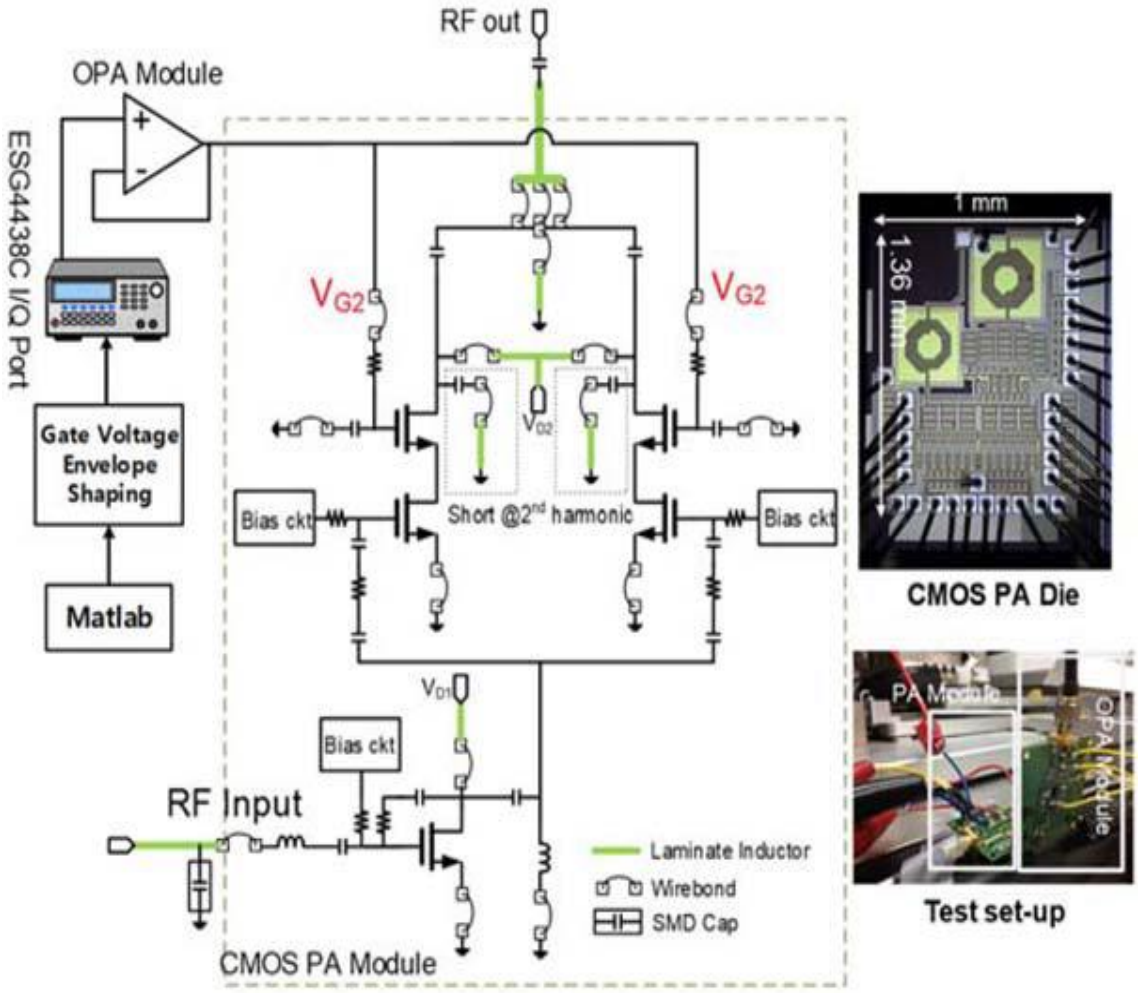

Figure 10: Photograph of proposed CMOS PA and test set-up

2.9 2.4 GHz CMOS LINEAR POWER AMPLIFIER FOR IEEE 802.11N WLAN APPLICATIONS

We design a linear CMOS power amplifier for IEEE 802.11n WLAN applications in this research, with a spiral-type output transformer. For linear CMOS power amplifiers, we conduct studies to determine the correct output of transformers and power stage structures. The power amplifier consisting of a single differential-pair for the power stage to exacerbate the problems of stability that often occur in linear power amplifiers with high gain. Alternatively, a spiraltype output transformer is used to investigate output matching network to mitigate the loss of output return. An IEEE 802.11n WLAN signal is used to test the built power amplifier. The power

amplifier achieves peak power of 21.28 dBm while the calculated EVM follows the standard for applications with 802.11n.

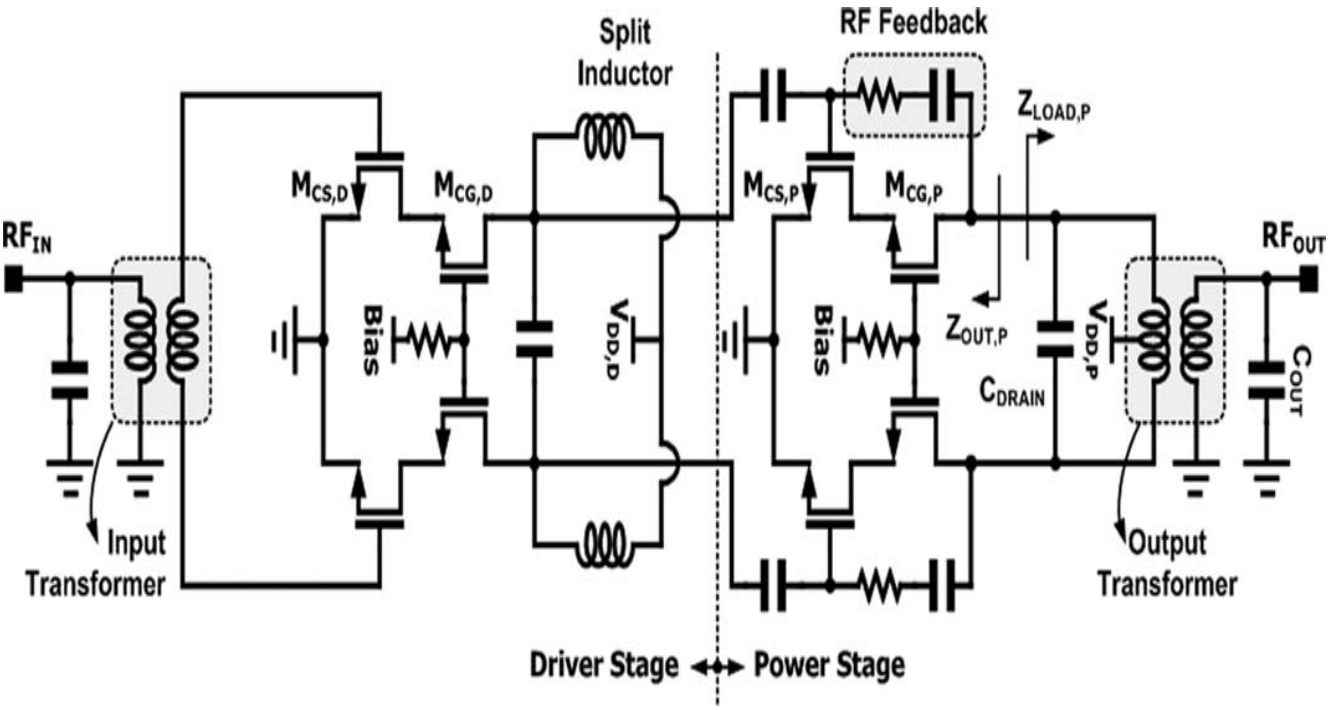

Figure 11: Simple schematic of the proposed power amplifier

Figure 11 shows a simple schematic of the proposed linear CMOS power amplifier according to the structure. In this work, the power stage is designed with a single differential-pair. Accordingly, to obtain watt-level output power, the output matching network should provide a sufficient impedance transformation ratio. The turn-ratio of the output transformer is designed to be 1:2. To mitigate reliability problems, a 320-nm RF CMOS is used as a common-gate transistor. To simplify the output matching network, the total gate widths of the common-source and common-gate transistors of the power stage for the ZOUT, P and ZLOAD, P is designed to be in a nearly conjugate relationship.

2.10 Multigate-Cell Stacked FET Design for Millimeter-Wave CMOS Power Amplifiers

The implementation of stacked CMOS circuits using a compact multi-gate layout technique is achieved in this design, rather than the traditional series connection of individual transistors. A unit multi-gate FET unit consists of a single transistor with single source and drain contact and multiple (four) gate connections. Capacitances are implemented in a distributed manner that makes

close proximity to the individual gate fingers using metal layers accessible within the CMOS back-end-of-line stack (BEOL Multi-gate-cell millimeterwave power amplifiers are given to operate across the 25–35 GHz band and achieve a saturated output power of 300 mW and peak power-added efficiency (PAE) at 30% in 45 nm CMOS SOI technology.

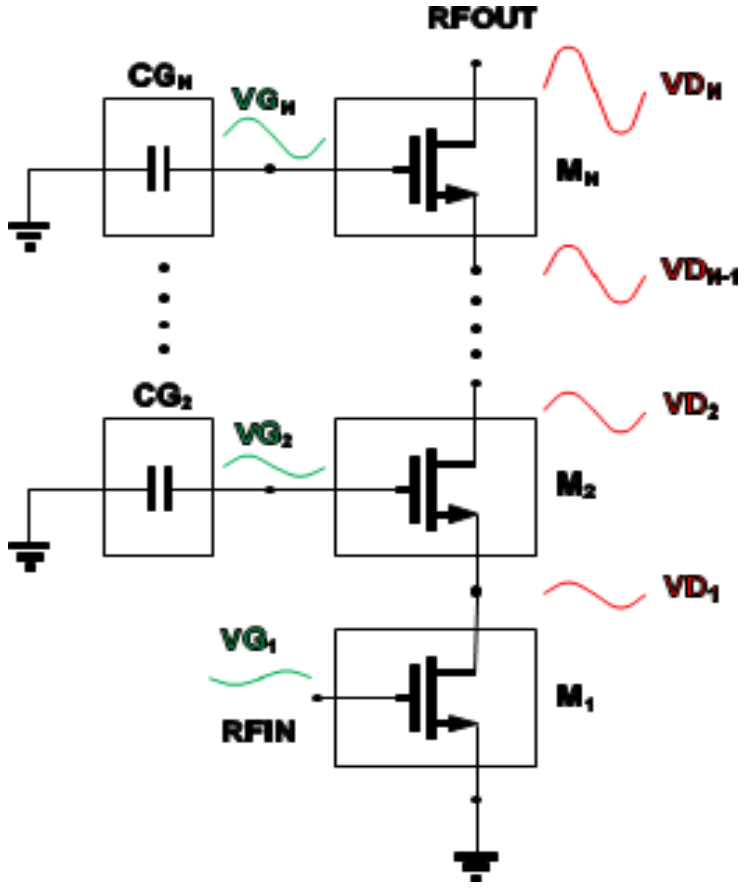

Figure 12: Representative schematic of a stacked FET PA with gate capacitors

2.11 A 5-GHz WLAN RF CMOS Power Amplifier with a Parallel-Cascode Configuration and an Active Feedback Linearizer

Within this design, a parallel-cascode configuration is proposed to cancel distortions of third and fifth intermodulation and third harmonic distortion (HD) due to the current nonlinearity of the drain – source. This also eliminates distortions at both common source (CS) and common gate (CG) levels due to the drain – source and gate – source nonlinear capacitances. The

configuration allows the amplifier linear characteristics to be robust against gate node voltage variations of CG transistors compared to previous multi-gated transistor linearization methods, because the CG transistors often remain in the saturation region and capability nonlinearities associated with CG transistors cancel each other under a wide range of performance capabilities.

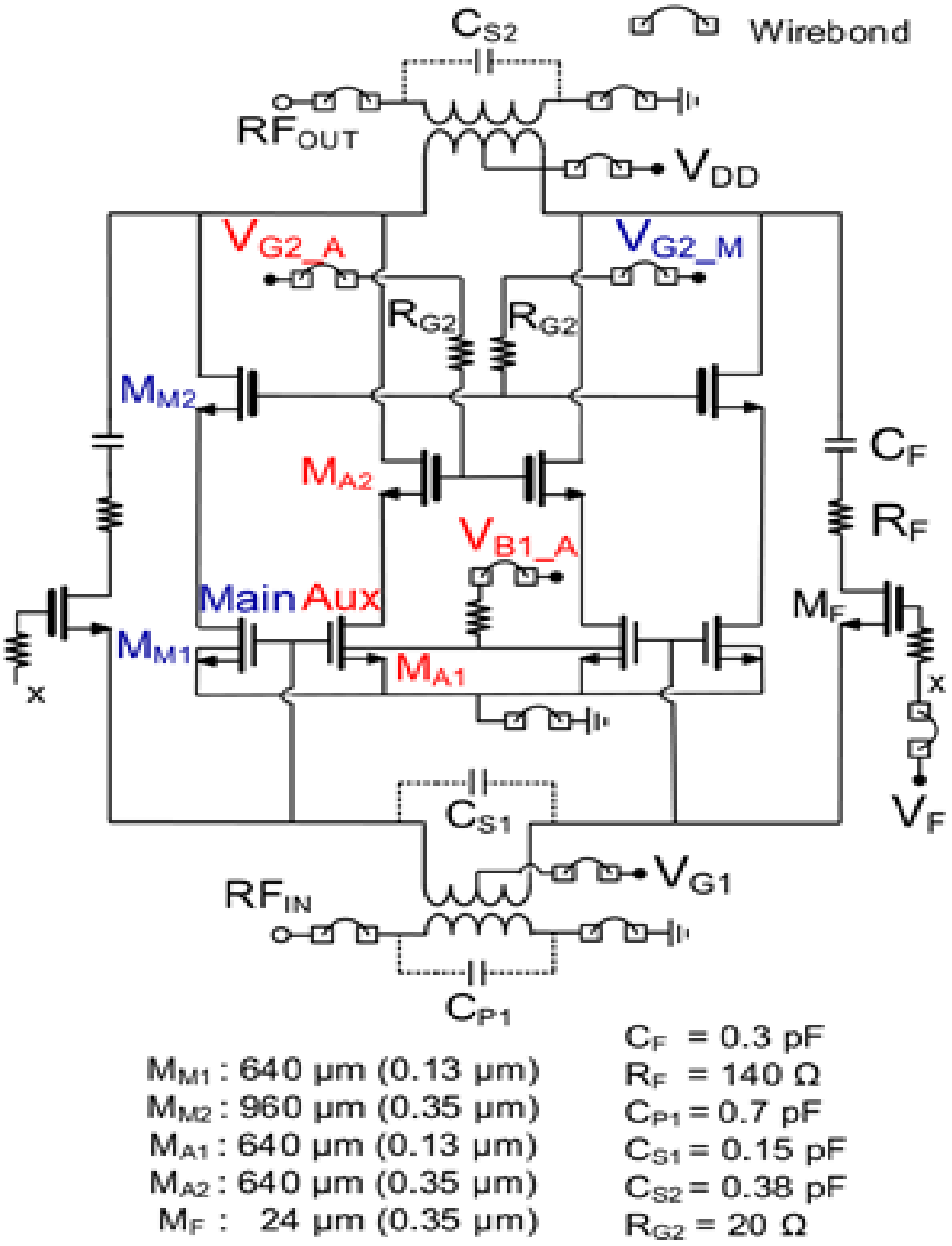

Figure 13: Overall schematic of the fully integrated CMOS PA

2.12 A 1.8-GHz CMOS Power Amplifier Using Stacked NMOS and PMOS Structures for High-Voltage Operation

A Class-E power amplifier is proposed in this design. It uses both NMOS and PMOS as the switching devices to reduce each transistor's voltage tension. A voltage-combining scheme with NMOS and PMOS is proposed, and this scheme is used to build a transformer. The power amplifier is implemented in a method with 0.18-m RF CMOS. The power amplifier allows a transmission voltage of up to 3.9 V. Only the proposed power-combining transformer can combine the voltages between the NMOS and the PMOS devices in a configuration where the transformer is spatially separated from the active devices.

The proposed power amplifier is designed and optimized to have less drain–source voltage under a supply voltage. The designed power amplifier uses stacked structures of thin gate–oxide NMOS and PMOS devices.

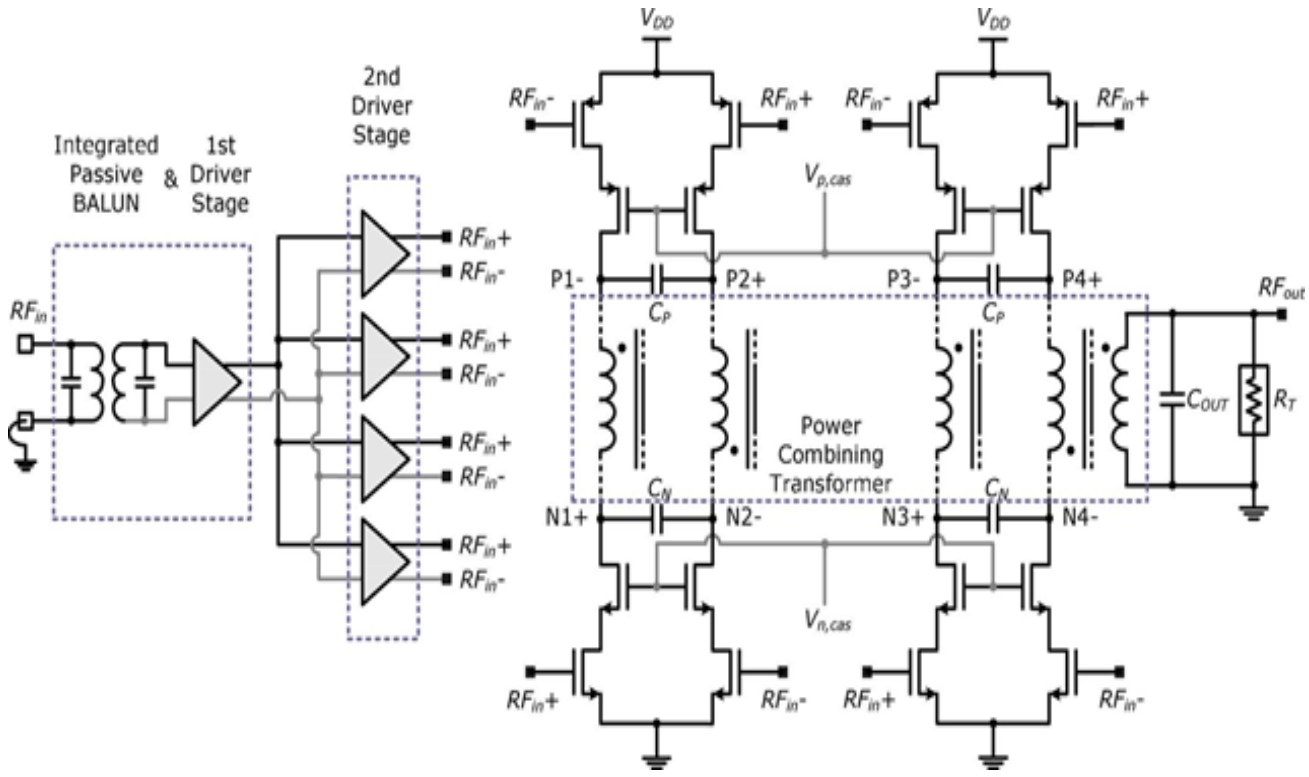

Figure 14: Overall schematic of the power amplifier. Some bias circuits are omitted

3. COMPARISON OF DIFFERENT CMOS POWER AMPLIFIERS

Table 1: Comparison of different CMOS Power Amplifiers

Design	Output power (dBm)	PAE (power added efficiency%)	Gain (dB)	Number of transistors
Class-O: A Highly Linear Class	31.6	39.6	9.6	6
Transformer Coupling and Artificial Dielectric Differential Transmission	12.5	19.50	15	14
Continuous gate voltage control	27	34.20	25	2
Linear Power Amplifier for IEEE 802.11N WLAN Applications	21.28	23.50	26.6	4
Transformer-Based Voltage-Type	21.8	12.40	8.7	48
Split cascode structure	23.4	20.8	19	10
Shot-through current rejection technique	14	26	17	8
Balun embedded driver stage	20.18	10.16	15.8	6
Parallel-Cascoded Configuration and an Active Feedback Linearizer	18.5	13.30	32	10
Multigate-cell stacked FET	24.77	30	13	N no of transistors connected in series
Stacked NMOS and PMOS Structures	30.2	36.80	9.8	16
Stacked NMOS, transformer PMOS	23.4	15.1	25.34	10

3.1 Output Power Comparison

Class O linear class power amplifier produces highest output power because of the use of power and power-gain boosters. The CMOS power amplifier based on transformer coupling and artificial dielectric differential transmission produces least output power. The rest produce a decent output power ranging from 20-30 dBm except for PA using shot through rejection technique and parallel Cascoded configuration.

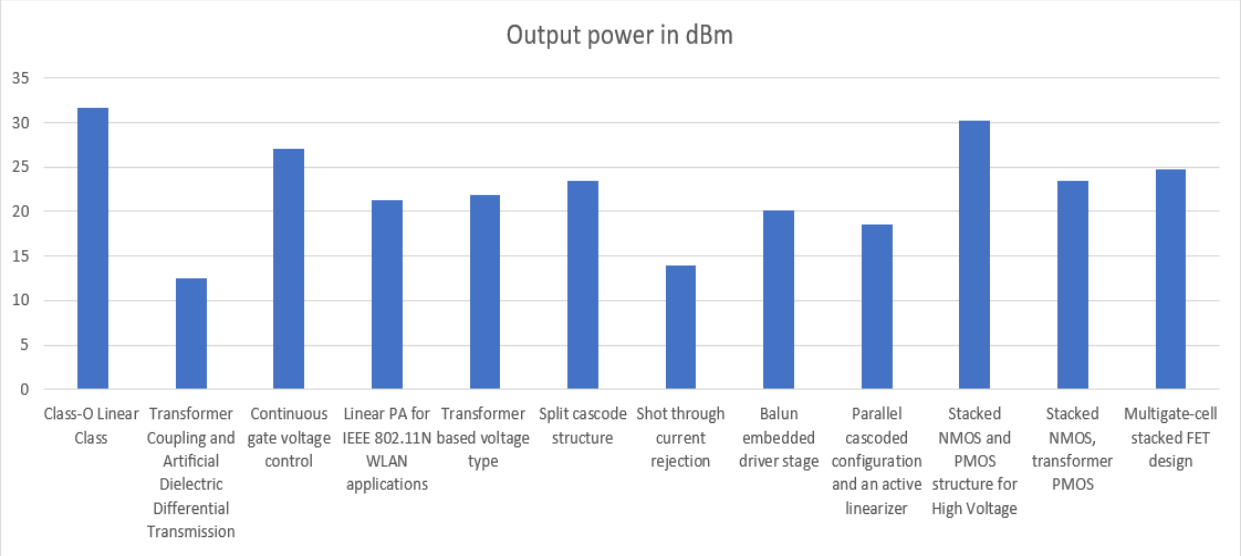

Figure 15: Different types of CMOS PA vs Output Power (dBm)

3.2 Power Added Efficiency (PAE) Comparison

The power added efficiency percentage was highest for Class O linear PA. It was lowest for the Balun embedded driver stage PA.

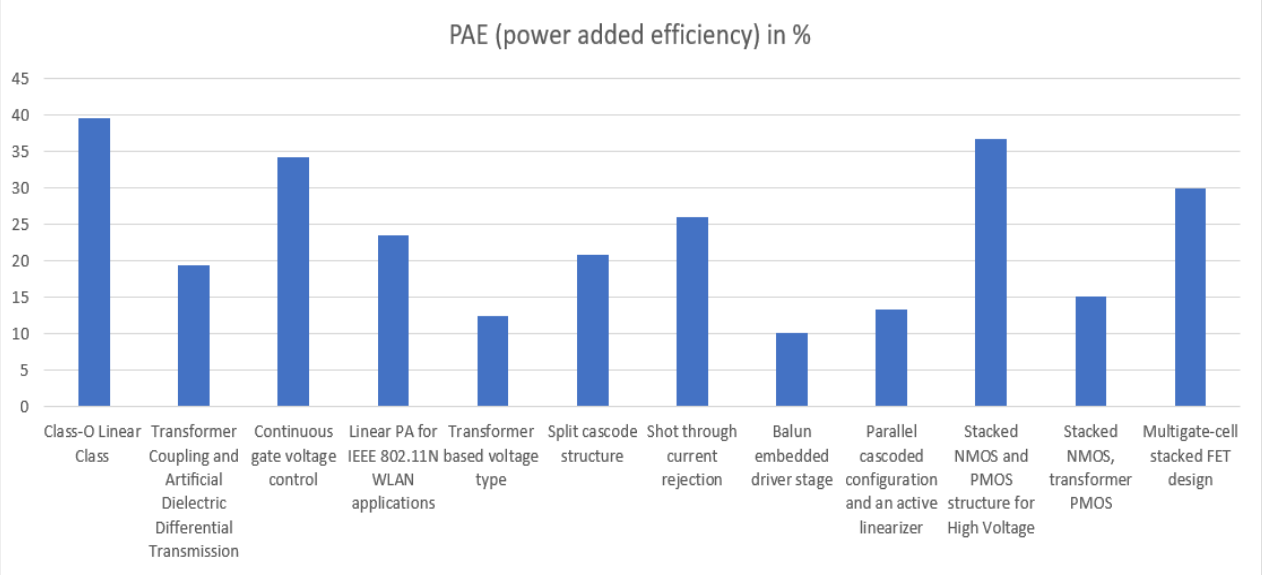

Figure 16: Different types of CMOS PA vs Power Added Efficiency (PAE %)

3.3 Gain comparison

The gain of 32 dB was highest for CMOS PA with parallel Cascoded configuration and an active linearizer. It was lowest (8.7 dB) for transformer-based voltage type PA.

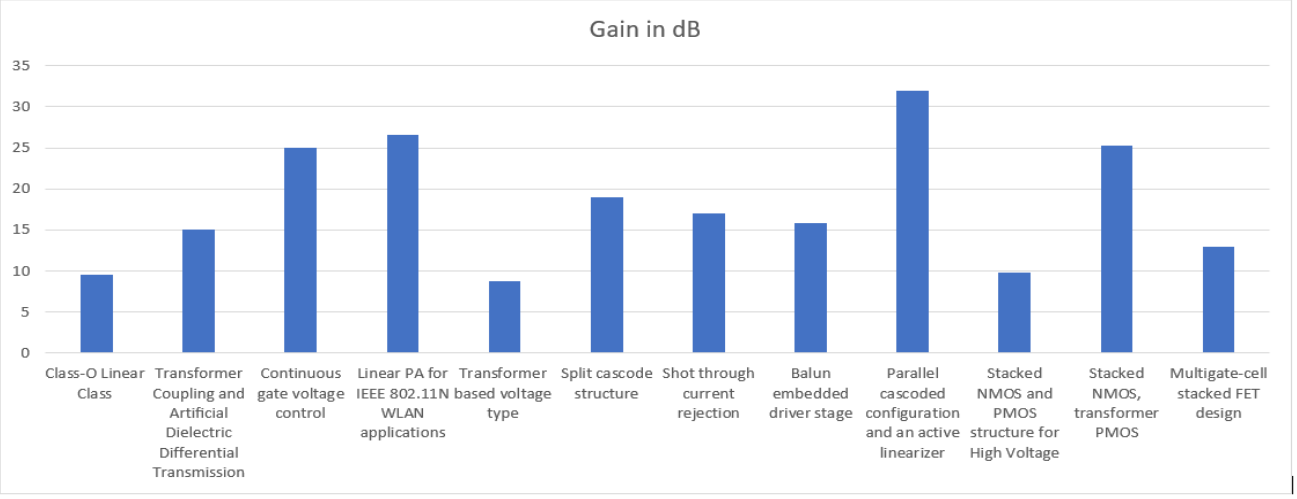

Figure 17: Different types of CMOS PA vs Gain in dB

3.4 Number of transistors comparison

The number of transistors used by transformer-based voltage type PA is maximum (48) when compared with the rest. The least number of transistors (2) are used in continuous gate voltage control PA. The rest of the PAs nearly use similar amounts of transistors lying in the range of 4-16.

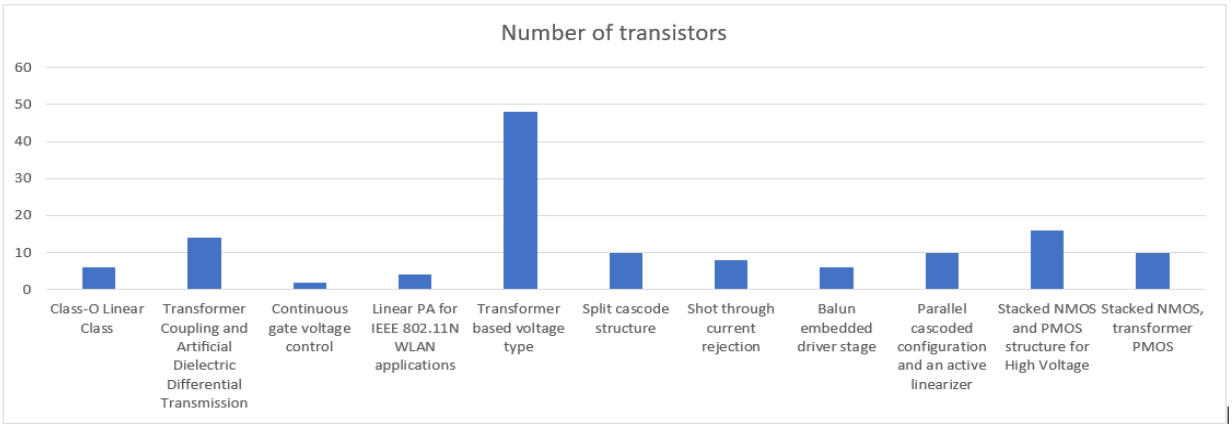

Figure 18: Number of transistors used vs Different types of CMOS PA

4. CONCLUSION

Different designs of CMOS power amplifiers are introduced and analyzed in a different fabrication technology and comparison of different designs of CMOS power amplifiers with parameters such as output power, gain, frequency, number of transistors and transformers is done. Output power, power added efficiency are the main performer's parameter of the CMOS power amplifiers. Comparison showed that the general cascode architecture is highly suitable for designing a 2.4GHz CMOS PA and can address the demand for high power added efficiency, output power and low-cost solutions by modern wireless communication systems. This CMOS power amplifier can be used in application where in high transconductance, high frequency and high efficiency .is required as well as highly integrated transceivers for many types of communication.

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