

Neelanjan Goswami

Quartus Prime Lite Edition - C:/Altera/pipemultQP16_1/Schematic/pipemult - pipemult2

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Project Navigator Hierarchy Entity/Instance MAX 10: 10M08DAF484C8GES > pipemult2

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Flow Summary

Flow Status: Successful - Mon May 25 19:14:03 2020

Quartus Prime Version: 16.1.0 Build 196 10/24/2016 SJ Lite Edition

Revision Name: pipemult2

Top-level Entity Name: pipemult

Family: MAX 10

Device: 10M08DAF484C8GES

Timing Models: Preliminary

Total logic elements: 6 / 8,064 (< 1 %)

Total registers: 21

Total pins: 44 / 250 (18 %)

Total virtual pins: 0

Total memory bits: 512 / 387,072 (< 1 %)

Embedded Multiplier 9-bit elements: 1 / 48 (2 %)

Total PLLs: 0 / 2 (0 %)

UFM blocks: 0 / 1 (0 %)

ADC blocks: 0 / 1 (0 %)

IP Catalog

- Installed IP
- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

Tasks Compilation Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- TimeQuest Timing Analysis
- EDA Netlist Writer

Messages

System Processing (143)

Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings

293000 Quartus Prime Full Compilation was successful. 0 errors, 23 warnings

81.6 100% 00:01:10

Windows Taskbar: Type here to search, 19:14, 25-05-2020

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 - Fmax Summary
 - Setup Summary
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width Summary

Slow 1200mV 85C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	128.21 MHz	128.21 MHz	clk1	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are

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