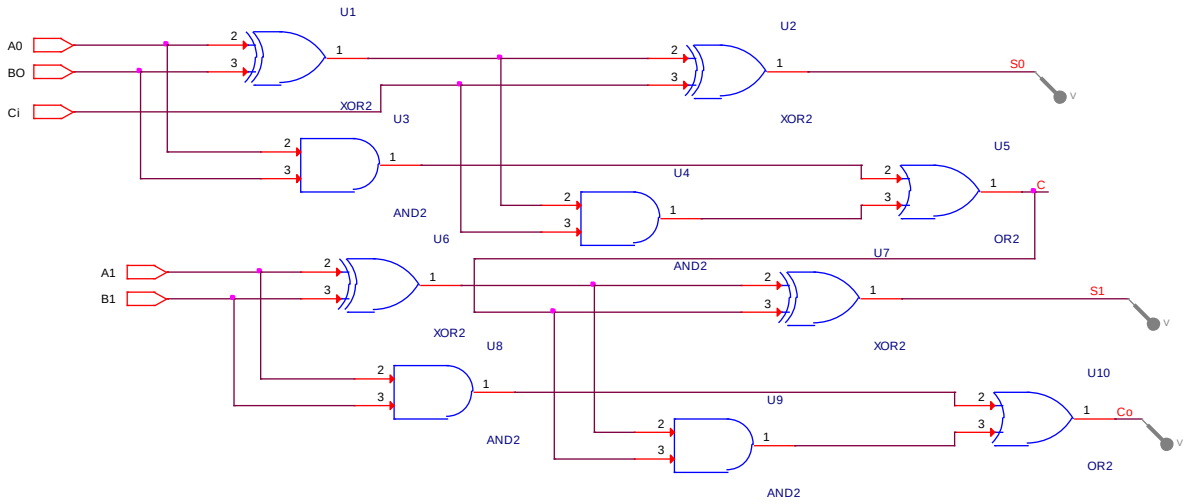
1) A 2-bit full adder with carry.

S0=(A0^B0)^Ci

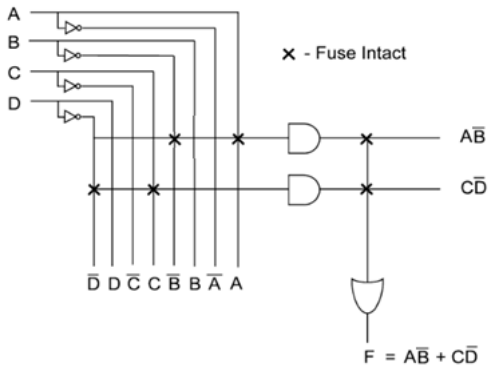
C=(A0&B0)+(Ci&(A0^B0))

S1=(A1^B1)^C

Co=(A1&B1)+(C&(A1^B1))



2) The logic equation **(A AND NOT(B)) OR (C AND NOT(D))**



Design explanation is that at and gate stage, 1st AND gate's inputs are from A and not (B) wires giving AB', similarly 1st and gate's inputs are from C and not (D) wires giving CD'. Now both are inputs to an OR gate, giving output as AB'+CD'

And it's LUT:-

RAM CONTENTS				
Address				Output Data
A	**B**	**C**	**D**	**F**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0