Neelanjan Goswami

Flow Status	Successful - Mon May 25 01:04:50 2020
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	pipemult2
Top-level Entity Name	pipemult
Family	MAX 10
Device	10M08DAF484C8GES
Timing Models	Preliminary
Total logic elements	6 / 8,064 (< 1 %)
Total registers	21
Total pins	44 / 250 (18 %)
Total virtual pins	0
Total memory bits	512 / 387,072 (< 1 %)
Embedded Multiplier 9-bit elements	1 / 48 (2 %)
Total PLLs	0 / 2 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	168.41 MHz	168.41 MHz	clk1	

Slow 1200mV 0C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	180.47 MHz	180.47 MHz	clk1	