Part A: DRAM Traces [50 pts]

Write a C/C++ program that takes as input the following parameters:

```
-w [address_width] -m [address_mapping] -n [num_requests] -p
[address_pattern] -t [type_pattern]
```

And generate a DRAM trace with the specified patterns. The trace should look like `Address: type`, where address is in hex and type is either R (for read) or W (for write).

Ans.

Code file is attached with this document. The output trace file is slightly different to match the MCsim format.

No. of bits for rows = 15
No. of bits for Columns = 10 (6 are offset bits)
No. of bits for banks = 3

For address pattern use (all lower case):

- sequential
- random
- row-hit
- row-conflict

For type patterns use:

- R for read
- W for write
- Anything else will be considered switching R/W

For Address Mapping use:

- row-bnk-col
- row-col-bnk
- bnk-col-row

PS. There are some compile time errors when using gcc from cmd to compile. I have used an IDE called devC++ to compile and create an executable.

Part B: Simulating Off-chip Memory [50 pts]

1) [10 pts] Use your tool from Part A to generate the following traces, where each trace should have 10K requests and the address mapping should be row:bank:column (assume a single channel and single rank).

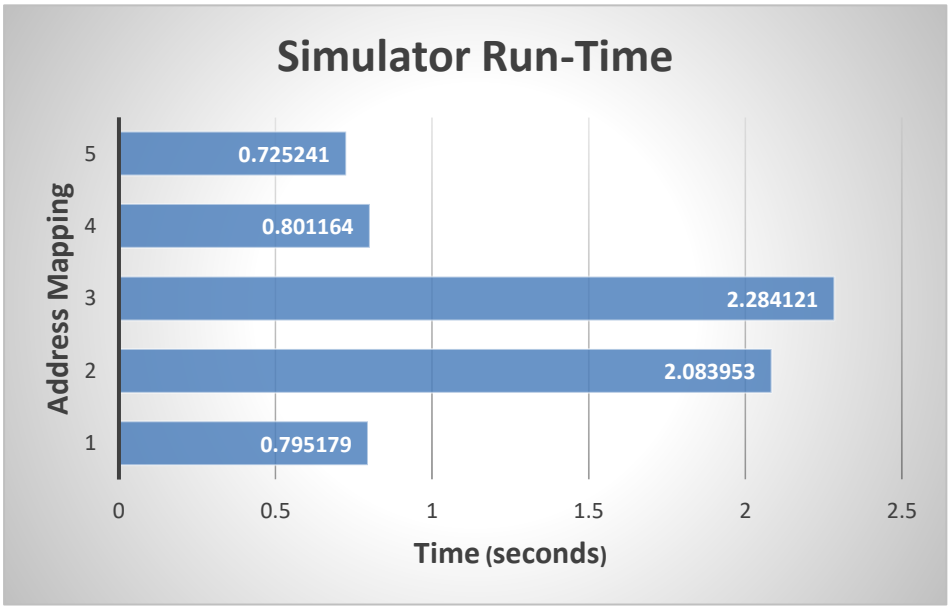
- • All Read, Sequential Trace
- • All Read, Random Trace
- • All Read, Conflict Trace
- • All Read, Hit Trace
- • Switching, Hit Trace

2) Familiarize yourself with MCsim simulator. Start with getting MCSim from here: https://github.com/uwuser/MCsim and read the README file.
Ans. Traces files attached

3) [15 pts] Configure MCsim to use FR-FCFS and run all the 5 traces from step 1. Make sure that the address mapping in MCsim are set correctly. In MCsim the address mapping is determined in the ini file where each segment is coded as follows: Rank[0], BankGroup[1], Bank[2], SubArray[3], Row[4], Col[5]. So, AddressMapping=425 means row:bank:column.
Draw a graph that compares the execution time of all the five traces.

Ans:

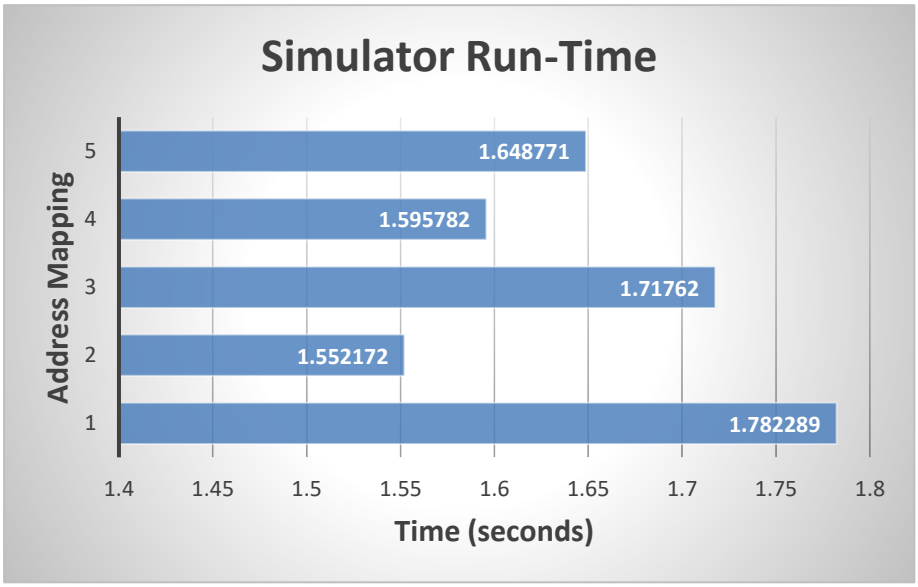
label	Address Pattern	open read	close read	open write	close write	Bandwidth (MB/s)	cycles	clicks	time (sec)=clicks/10^6
1	All Read Sequential	9375	625	0	0	3624.96	141244	795179	0.795179
2	All Read Random	0	10000	0	0	1383.83	369988	2083953	2.083953
3	All Read Row-Conflict	3	9997	0	0	1384.17	369898	2284121	2.284121
4	All Read Row-Hit	9999	1	0	0	3938.13	130012	801164	0.801164
5	Switching Row-Hit	4999	1	5000	0	3303.1	155007	725241	0.725241



4) [10 pts] Change the FR-FCFS ini file to use close-page policy and repeat the experiments and redraw the graph similar to part 3.

Ans.

label	Address Pattern	open read	close read	open write	close write	Bandwidth (MB/s)	cycles	clicks	time (sec)=clicks/10^6
1	All Read Sequential	0	10000	0	0	1383.83	369988	1782289	1.782289
2	All Read Random	0	10000	0	0	1383.83	369988	1552172	1.552172
3	All Read Row-Conflict	0	10000	0	0	1383.83	369988	1717620	1.71762
4	All Read Row-Hit	0	10000	0	0	1383.83	369988	1595782	1.595782
5	Switching Row-Hit	0	5000	0	5000	1296.26	394983	1648771	1.648771

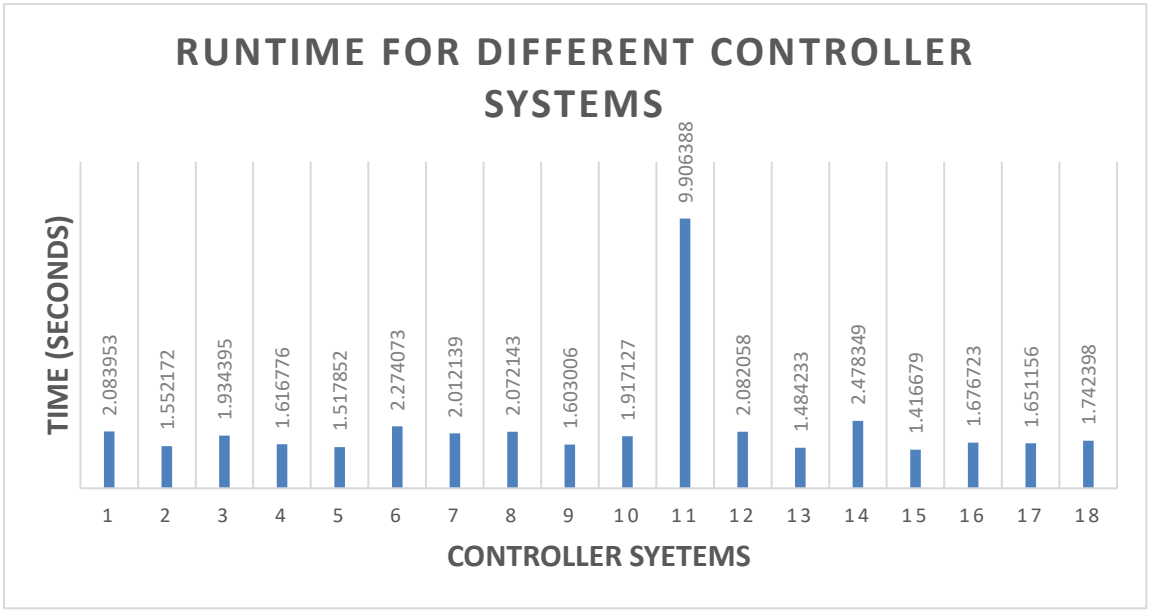


As you can see from the graphs, run-time is similar for all the Address patterns in close-page, whereas in the open page policy the run-time varies, with sequential and Row-hit patterns have considerably less run-time as compared to others (less than 50 %). Whereas Random Trace pattern works best for the close page policy

5) [15 pts] Use the trace “All Read, Random Trace” to compare all the controller systems supported by MCsim. Plot the results in a bar-chart.

Ans.

Labels	Controller System	open read	close read	open write	close write	Bandwidth (MB/s)	cycles	clicks	time (sec)=clicks/10^6
1	FR-FCFS (open)	0	10000	0	0	1383.83	369988	2083953	2.083953
2	FR-FCFS (close)	0	10000	0	0	1383.83	369988	1552172	1.552172
3	AMC (open)	0	10000	0	0	1219.07	419992	1934395	1.934395
4	AMC (close)	0	10000	0	0	1219.1	419983	1616776	1.616776
5	BLISS	0	10000	0	0	1383.83	369988	1517852	1.517852
6	DCmc	0	10000	0	0	1383.83	369988	2274073	2.274073
7	FCFS	0	10000	0	0	1383.83	369988	2012139	2.012139
8	MAG	0	10000	0	0	1765.55	289996	2072143	2.072143
9	MCMC (mcmc)	0	10000	0	0	1280.02	399994	1603006	1.603006
10	MEDUSA	0	10000	0	0	1383.83	369988	1917127	1.917127
11	ORP	0	10000	0	0	1383.83	369988	9906388	9.906388
12	PAR-BS	0	10000	0	0	1383.83	369988	2082058	2.082058
13	PipeCAS	0	10000	0	0	1383.83	369988	1484233	1.484233
14	PMC (open)	0	10000	0	0	1089.39	469987	2478349	2.478349
15	PMC (close	0	10000	0	0	1089.42	469978	1416679	1.416679
16	ROC	0	10000	0	0	1383.83	369988	1676723	1.676723
17	RTMem (open)	0	10000	0	0	1219.07	419992	1651156	1.651156
18	RTMem (close)	0	10000	0	0	1219.1	419983	1742398	1.742398


RUNTIME FOR DIFFERENT CONTROLLER SYSTEMS
TIME (SECONDS)
2.083953
1.552172
1.934395
1.616776
1.517852
2.274073
2.012139
2.072143
1.603006
1.917127
9.906388
2.082058
1.484233
2.478349
1.416679
1.676723
1.651156
1.742398
1
2
3
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14
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17
18
CONTROLLER SYETEMS