STUDY OF TUNNELING CURRENT THROUGH ULTRA-THIN GATE OXIDE MOSFET AND ITS EFFECT ON CMOS CIRCUITS

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ABSTRACT

A numerical model is constructed to study the tunneling current through ultra-thin gate oxide MOSFET and the effect of this tunneling current on the MOSFET and on CMOS circuits' performance. This model is used to calculate the characteristics of MOSFET under tunneling effect by solving the equations that governing the current transportation through the semiconductor (current density equations, continuity equations and Poisson's equation) numerically in conjunction with those describing the tunneling between the gate and the semiconductor. Through this model, the effects of various device parameters such as the insulator thickness, doping concentration, gate material work function and temperature can be studied. However, in this paper we concern our self with the effect of the oxide thickness on the tunneling current through MOSFET and its effect on CMOS circuits.

KEYWORDS: Ultra-thin gate oxide MOSFET, Tunneling current and CMOS circuits.

1. INTRODUCTION

CMOS transistors with conventional processing technologies have been encountering performance limits as the device dimensions and operating voltages are scaled down. To overcome these limits while maintaining compatibility with conventional processes, new technologies continue to be developed. Figure (1) illustrates important features of a state of the-art CMOS technology [1 and 2].According to International Technology

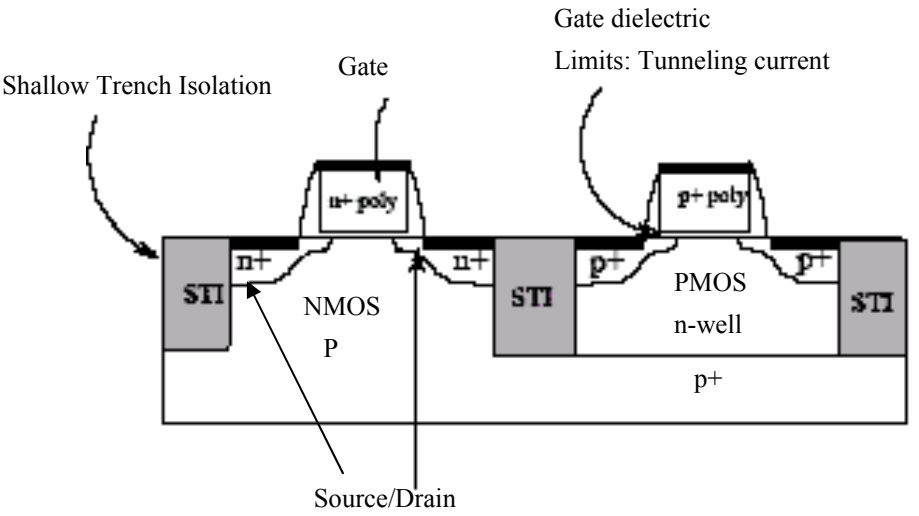


Fig.1 A cross section of state-of-the-art CMOS [1,2]

Roadmap Semiconductors (ITRS); CMOS with channel length sub-100nm needs a gate oxide thickness of around 1.2-1.5nm [3]. With such thin oxide thickness direct tunneling occurs, resulting in increasing the gate leakage current. This gate leakage current increases the power dissipation and deteriorates device performance and circuit stability for ULSI. In the ultra-thin gate oxide regime the gate leakage current can contribute significantly to off-state leakage, which may result in fault circuit operation since designers may assume there is no gate current. A recent study has shown that direct tunneling current appears between the source–drain extension (SDE) and the gate overlap, so-called the edge direct tunneling (EDT) [4]. This results from the fact that the ratio of the gate overlap to the total channel length becomes large in the short-channel device compared to that of the long-channel device. However, even though there were many reports concerning the effect of gate leakage current to MOS transistor operations, fewer studies have been made regarding impacts of gate current to circuit operations due to the absence of circuit simulation model for gate tunneling current. In this paper a numerical model has been constructed to study the tunneling current through ultra-thin gate oxide MOSFET and the effect of this tunneling current on the MOSFET and on the performance of CMOS circuits.

2. FORMULATION OF THE NUMERICAL MODEL

MOSFET transistor, may along its conducting channel between source and drain, be considered as a sequence of elementary MIS controlled diodes and with different bias Voltages $(0 \le \mathbf{V_Y} \le \mathbf{V_{DS}})$.The MOSFET transistor with a non-uniform doped substrate, is composed of a number of units of controlled MIS diodes as shown in Fig.3 , which are one-dimensional in the direction x perpendicular to the semiconductor surface. The quasi-Fermi levels of the MIS device are separated near the surface by a quantity $\mathbf{qV_Y}$ as shown in Fig.4, according to the current along the channel; constant quasi Fermi levels E_{F_P} and E_{F_n} are assumed within the surface space charge region. The MIS controlled diode can, along the x-direction, be considered to compose of a strong inversion layer near the surface ($0 \le x \le w_i$), a depletion layer ($w_i \le x \le x_d$), and quasi-neutral region ($x_d \le x$).The strong inversion occurs by definition at the point $x = w_i$, where the minority carrier concentration is equal the doping impurity concentration at the boundary x_d of the depletion region [5].

$$n(w_i) = N(x_d). \qquad (1)$$

The following set of nonlinear equations was taken as the starting point in the analysis of the MOSFET. The set of equations was solved numerically to a pre-specified accuracy using iterative techniques. In order to compute the response of the MOSFET, a numerical solution of the equations that govern the transportation in the semiconductor in conjunction with those describing the tunneling between the gate and the semiconductor has been established.

2.1 Current Transportation In The Semiconductor Region

The semiconductor region of the MOSFET is characterized by the following set of differential equations [6 and 7]

(a) Poisson's equation is given by:

$$-\frac{d^2\psi}{dx^2} = \frac{dF}{dx} = \frac{q}{\varepsilon}\left[p(x) - n(x) + N(x)\right] \qquad (2)$$

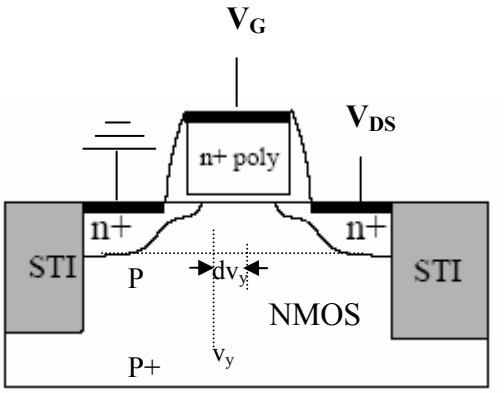


Fig.2cross-section of non-uniformly doped n-channel MOSFET

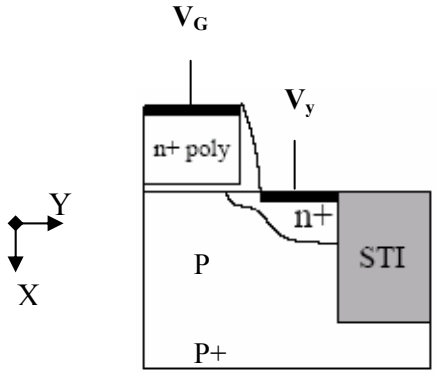


Fig.3 cross-section of the controlled MOS structure corresponding the Quasi-equilibrium situation at the Conducting channel of the transistor

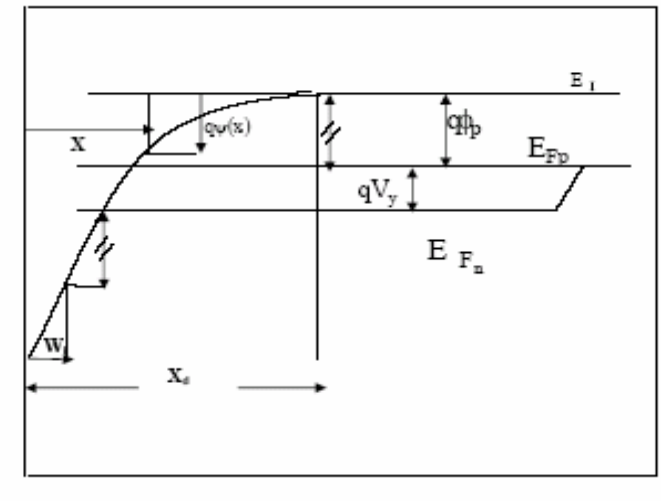


Fig.4 Energy band diagram for controlled MOS structure shown in Fig.2

Where $\psi(x)$ resembles the electric potential within the semiconductor and F denotes the built-in electric field at the position x and $N(x)$ is the non-uniform impurity distribution at any distance x. Note that x begins at the insulator-semiconductor interface along the semiconductor.

$$p(x) = n_i \exp\left(\frac{E_i - E_{Fp}}{KT}\right) \tag{3}$$

$$n(x) = n_i \exp\left(\frac{E_{Fn} - E_i(x)}{KT}\right)$$

(b) The current density equations are:

$$J_n = q(\mu_n nF + D_n \frac{dn}{dx}) \tag{4}$$

$$J_p = q(\mu_p pF - D_p \frac{dp}{dx})$$

where μ_n and μ_p as a function of impurity concentration are given by (*Zambuto,1989*).

$$\mu_n = \frac{1330 - 65}{1 + [\frac{N(x)}{8.5 \times 10^{16}}]^{0.76}} + 65.5 \tag{5}$$

$$\mu_p = \frac{495 - 47.7}{1 + [\frac{N(x)}{6.3 \times 10^{16}}]^{0.72}} + 47.7$$

(c) The electrons and holes continuity equations are:

$$\frac{dn}{dt} = G - U + \frac{1}{q}\frac{dJ_n}{dx} \tag{6}$$

$$\frac{dp}{dt} = G - U - \frac{1}{q}\frac{dJ_p}{dx}$$

where U is the net thermal generation-recombination rate which is usually given by *Shockley-Read-Hall* equation:

$$U = \frac{pn - n_i^2}{\tau_n (n + n_1) + \tau_p (p + p_1)} \tag{7}$$

where τ_n and τ_p as a function of impurity concentration are given by (*Weber et al., 1997*)

$$\tau_n = \frac{\tau_{no}}{1 + \frac{N(x)}{N_{ref}}} \qquad \tau_p = \frac{\tau_{po}}{1 + \frac{N(x)}{N_{ref}}} \tag{8}$$

where N_{ref} =2×10^{16} cm^{-3} , τ_{no} and τ_{po} are the minority carrier lifetime for electrons and holes at lightly doped semiconductor and G is the number of electron-hole pairs (EHPs) generated per unite volume at a distance x from the insulator-semiconductor .

2.3 Characterization Of The Tunneling Through The Insulator

According to the energy band diagram shown in Fig.5 there are net current J_{CT} and J_{VT} flowing from the conduction and from the valence bands of the semiconductor to the gate contact. The tunneling current J_{CT} and J_{VT} can be evaluated using the independent electron approach outlined by Harison [8] for (100)-oriented silicon and, employing the expression given by *Green* and *et al* [9].

$$J_{CT} = 4\pi e \frac{m_{Ti}}{h^3} \int_{E_C}^{E_{\max}} dE (f_m - f_n) \int_0^{\frac{m_{TS}}{m_{TI}}(E - E_C)} dE_T \exp(-\beta) \tag{9}$$

$$J_{VT} = 4\pi e \frac{m_{Ti}}{h^3} \int_{E_{\min}}^{Ev} dE (f_m - f_p) \int_0^{\frac{m_{TS}}{m_{TI}}(E_V - E)} dE_T \exp(-\beta)$$

where β is given by

$$\beta = \frac{4\pi}{h} \sqrt{2 m_{TI}} \int_{X_{SC}}^{X_m} \sqrt{E_T - (E - E_{ci})(1 + \frac{E - E_{ci}}{E_{gi}})}\, dx \tag{10}$$

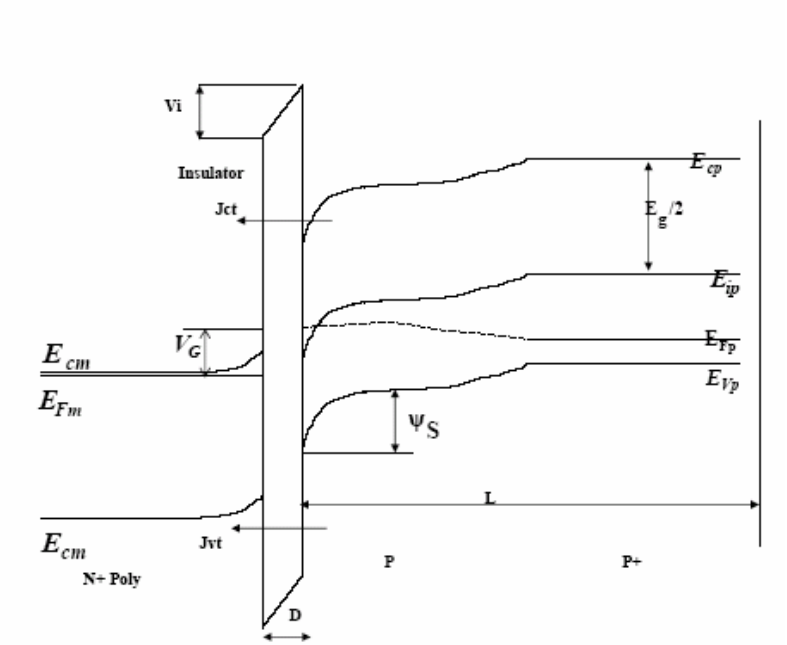


Fig.5 Energy band diagram of MOS structure

2.4 Voltage Relationship

In addition to the above relationships, the following relationship relates the gate voltage of the device (V_G) to the semiconductor surface potential, ψ_s, and the voltage drop across the insulator V_I. As shown in Fig.5, V_G is the difference between the gate Fermi-levels of the front surface and the back surface for the device, and it is given by:

$$V_G = -\left[V_I + \psi_s + \frac{\phi_{me} - \phi_{si}}{q} + \frac{\psi_{si} - \frac{E_g}{2}}{q} + \delta \right] \qquad (11)$$

where ϕ_{me} is the effective gate work function, which is related to the actual gate work function ϕ_{mi} by:

$$\phi_{me} = \phi_{mi} - \frac{Q_{eff} D_{eff}}{\varepsilon_i} = \phi_{mi} - \frac{Q_s D}{\varepsilon_i} \qquad (12)$$

where Q_{eff} is the fixed charge (positive or negative) in the insulator layer at a distance D_{eff} from the metal. To calculate the voltage V_I across the insulator, it is assumed that the electric field in the insulator F_i is constant, which is related to F_S (using *Gauss's low*) by:

$$-\varepsilon_i F_i + \varepsilon_s F_s = Q_{ss} \qquad (13)$$

where F_S represents the electric field at the insulator-semiconductor interface and Q_{SS} represents the charge stored in the surface states. F_S and Q_{SS} depend upon the surface voltage ψ_S.

$$V_I = DF_i = \frac{D}{\varepsilon_i}(\varepsilon_s F_s - Q_{ss}) \qquad (14)$$

Substituting from 12 and 14 into 11, the gate voltage can be expressed by:

$$V_G = -\left[\psi_s + \frac{\varepsilon_s}{\varepsilon_i} DF_s - \frac{D}{\varepsilon_i}(Q_s + Q_{SS}) + \frac{\phi_{mi} - \phi_{si}}{q} + \frac{\psi_{si} - \frac{E_g}{2}}{q} + \delta \right] \qquad (15)$$

where ϕ_{Si} is the semiconductor affinity, ψ_{si} is the difference between the E_{fp} and E_i and δ is the difference between E_{fp} and E_{fm} of the metal at the backside.

2.2 Drain Current Formulation

The drain current I_D of the MOSFET is given by[10] :

$$I_D = q\mu_n \frac{W}{L} \int_0^{V_{DS}} \int_0^{w_i} n(x)\,dx\,dV_y \qquad (16)$$

and may be written as

$$I_D = q\mu_n \frac{W}{L} \int_0^{V_{DS}} Q_i(V_y)\, dV_y \qquad (17)$$

where μ_n is the mobility along the conducting channel .

$$Q_i(V_y) = -q \int_0^{w_i(V_y)} n(x, V_y)dx = \varepsilon_S(\phi_s' - \phi_i') \qquad (18)$$

where $Q_i(V_y)$ represents the inversion charge along the conducting channel, where the applied voltage is $0 \le V_y \le V_{DS}$.

3. NUMERICAL RESULTS

The numerical results are restricted to P-type silicon substrate MOSFET (n-channel) with a polysilicon for gate contact, although the calculations are generally valid for any other semiconductor materials for the substrate and any other materials for gate contact. The numerical values assigned to the model parameters are listed in Table (1).

3.1 THE EFFECT OF OXIDE THICKNESS ON THE GATE CURRENT

Figure (5) shows that, decreasing the oxide thickness will lead to an increase in the gate current, because as the oxide thickness decreases the probability of the carriers to tunnel through the gate insulator will increase, leading to an increase in the tunneling current. To compare the numerical result with the real measurements [12], Fig.6 shows the gate current as a function of gate voltage at different oxide thicknesses. The simulated gate currents using the numerical model agree well with those from measurements for oxide thicknesses of 1.5 and 1.3 nm. Discrepancies between the measured and simulated data in Fig.6 are probably caused by surface roughness, uncertainty in determining the effective oxide thickness, and the voltage drop at the poly gate due to the gate leakage current.

Parameter	**standard symbol**	**Numerical values**
Temperature	T	300 ^{o}K
Metal-Insulator work function	ϕ_{mi}	4.1 eV
Insulator parameters Dielectric constant Band gap	 ε_i E_{gi}	 3.82×ε_o 8 eV
Semiconductor parameters Dielectric constant Band gap	 ε_s E_{gs}	 11.7×ε_o 1.1 eV
Electron affinity	ϕ_{si}	3.2 eV
Intrinsic carrier concentration	n_i	1.5×10^{16} m^{-3}
Effective density of state ratio	N_c/N_v	1.73
Recombination parameters	n_1,p_1	n_i
Effective mass of electron and hole in insulator and in semiconductor	m_{Ti}, m_{Ts}	0.65m_o
Surface charge concentration	Q_s	1×10^{16} m^{-2}

Table 1: The basic input parameters for MOSFET device

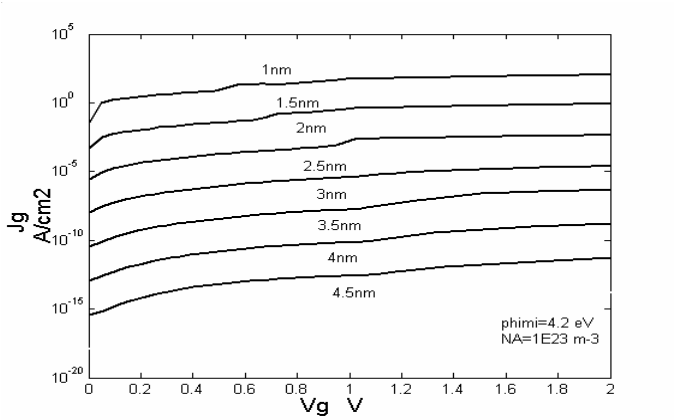


Fig.5 Tunneling current as function of V_G at different values of t_{ox}

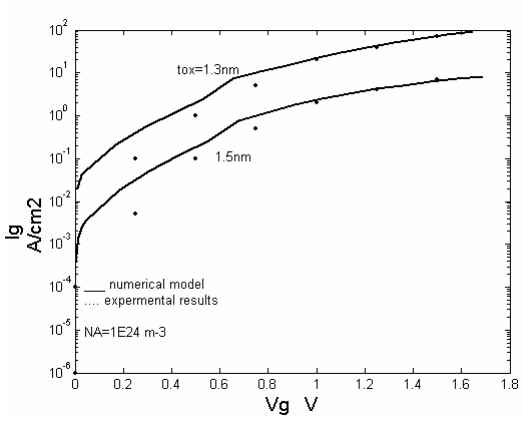


Fig.6 Tunneling current as function of V_G at different values of t_{ox}

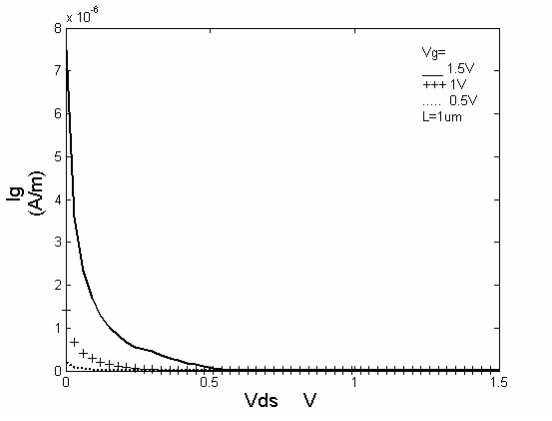


Fig.7 tunneling current as function of V_{DS}

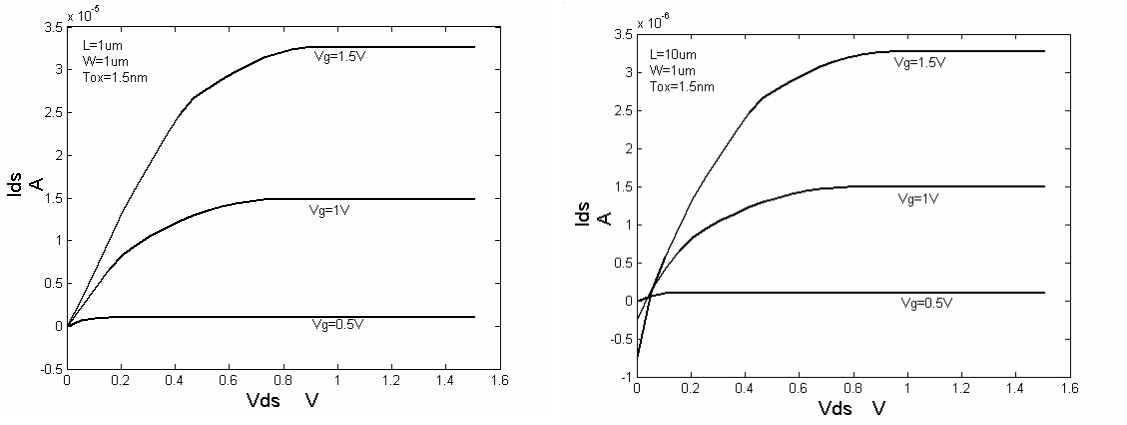
3.2 THE EFFECT OF DRAIN VOLTAGE ON THE GATE CURRENT

In order to consider the effect of drain voltage on the gate tunneling current, the gate tunneling current is calculated as a function of drain voltage for different values of gate voltages as shown in Fig.7. The simulated gate current decreases as the drain bias increases due to the increase of surface potential at the drain, which leads to a reduction in the voltage across the insulator. The direction of gate current near the drain region can even become reversed when the potential of the drain is higher than that of the gate. Hence, total gate tunneling current becomes lower as the drain bias moves from the linear to saturation region operation; the gate current effect is dominant at high V_{GS} and low V_{DS} bias conditions.

3.3 THE EFFECT OF TUNNELING CURRENT ON DRAIN CURRENT

The effect of the gate tunneling current on the drain current for different channel lengths is shown in Fig.8 (a) and (b) .It is obvious that effect of gate tunneling current on the drain current becomes less problematic for the short channel MOSFETs because the channel current is much higher than gate current and gate current decreases as the channel length is reduced. However,

even though these gate currents for an individual transistor may not be significant, the sum of all gate currents for the entire chip will become a serious problem for applications with battery operation.



(a) (b)

Fig.8 the drain current as function of V_{DS} for different channel length (a)L=1 μm (b) L=10 μm.

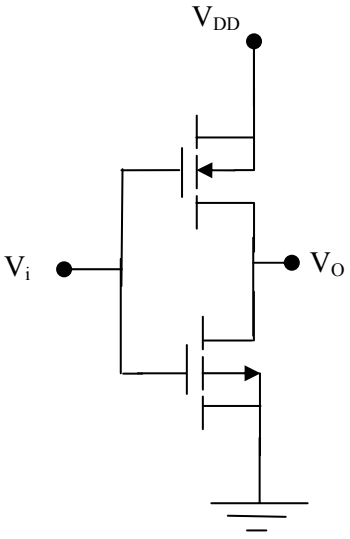


Fig.9 Schematic of CMOS inverter

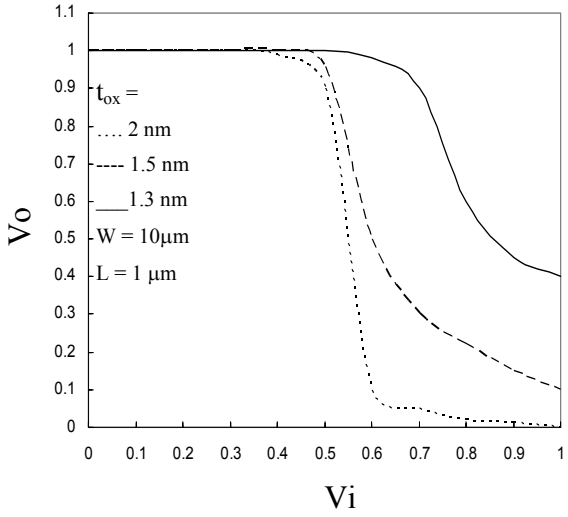


Fig.10 Transfer characteristics of CMOS Inverter for gate oxide thinner than 2nm

3.4 CIRCUIT SIMULATIONS

The numerical data obtained are used to simulate the effect of gate current on the transfer characteristics of the CMOS inverter shown in Fig.9. The results are shown in Fig.10. Scaling down the oxide thickness lower than 2nm leads to a significant increase in the output low–level voltage, which worsens the noise margin and result in faulty operation for the CMOS inverter.

4. CONCLUSION

A numerical model is constructed to study the tunneling current through ultra-thin gate oxide. The simulated gate current from this model demonstrates a good agreement with the previously measured data. The effect of the gate current on the functionality of CMOS inverter has been investigated. It has been found that, the output low-level voltage increases for gate thickness thinner than 2nm; this worsens the noise margin and result in faulty operation for the CMOS inverter.

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الملخص العربى

دراسة تاثير تيار الاختراق خلال عازل بوابة ذو تخانة رقيقة جدا لترانزستورتأثير المجال ذو البوابة المعزولة وتاثيرذلك التيار على دوائرCMOS

تم بناء أ نموذج عددى لدراسة تاثير تيار الاختراق خلال عازل بوابة ذو تخانة رقيقة جدا لترانزستورتأثير المجال ذو البوابة المعزولة وتاثيرذلك التيار على دوائر CMOS. باستخدام هذا الانموذج *أمكن حساب خواص الترانزستور تحت تاثير تيار الاختراق عن طريق* حل المعادلات التى تحكم انتقال التيار خلال شبه الموصل مع تلك التى تحكم عملية الاختراق خلال العازل الرقيق ما بين البوابة وشبة الموصل واستخدم هذا الانموذج فى دراسة تاثير المعاملات المختلفة مثل*تخانة العازل على اداء الترانزستور وكذلك على اداء عاكس CMOS.*