10.1
(a)

	Setup time	clk to Q Delay	D to Q Delay	Combi -Delay	Hold time
F/F	65 pS	50 pS	n/a	35 pS	30 pS
Latches	25 pS	50 pS	40 pS	35 pS	30 pS

maximum logic propogation Delay < 500 ps
Clock skew = 0

maximum logic propogation delay
$$= \text{clock cycle} - (\text{setup time} + \text{clk to Q})$$

$$= 500 - (65 + 50)$$
$$= 500 - (115)$$
$$= \underline{\underline{385 \, pS}}$$

10.2 clock skew between two Elements
$$= 50 \, pS$$
max logic propogation Delay $\leq 500 \, pS$

max logic propogation Delay
$$= \text{clock cycle} - [\text{setup time} + \text{clk to Q} + \text{clock skew}]$$

$$= 500 - [65 + 50 + 50]$$
$$= 500 - (115 + 50)$$
$$= 500 - 165$$
$$\simeq 335 \, pS$$

10.3

(a) To find :

minimum logic contamination delay

= Hold time - combination Delay

for F/F

Hold time = 30 pS

combination Delay = 35 pS

minimum logic contamination

= 30 - 35 = -5

But, t cannot be negative

thus, t = 0 pS

10.4

clock skew ≤ 50 ps

minimum contamination delay

= Hold time - (combination Delay) + (clock skew)

= 30 - (35) + (50)

= 30 35 = -5 + 50 = 45 ps.