VLSI DESIGN

(3EC601CC24)

Special Assignment

Parity Checker For 3-Bit Data Word

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1.Introduction

1.1 Abstract:

Basic concepts about the parity checker are presented in the project introduction, considering a 3-bit data word. A parity checker can be considered in digital systems where error detection is required during data transmission. The purpose of the parity-checker project was to present a design and realization of a parity checker using a very important software tool for VLSI design called Microwind. This project, therefore, has relevance to VLSI design principles since Microwind is employed in the practical realization of reliable circuits useful in error detection.

In this project, we are going to design a parity checker circuit for 3-bit data words using the Microwind tool, one of the prominent tools in VLSI design. The checking of parity is among the simplest yet powerful techniques for digital communication systems assurance of integrity of data, potentially finding single-bit errors. By implementing a 3-bit parity checker, we want to illustrate the principles lying beneath error detection and basic steps of the VLSI circuit design process. The project leads the reader through design steps, simulation, and verification of the parity checker, underlining how Microwind is helpful in designing efficient digital circuitry.

1.2 Keywords:

- Parity Checker
- 3-Bit Data Word
- VLSI Design
- Microwind Tool
- Error Detection
- Digital Communication
- Circuit Simulation

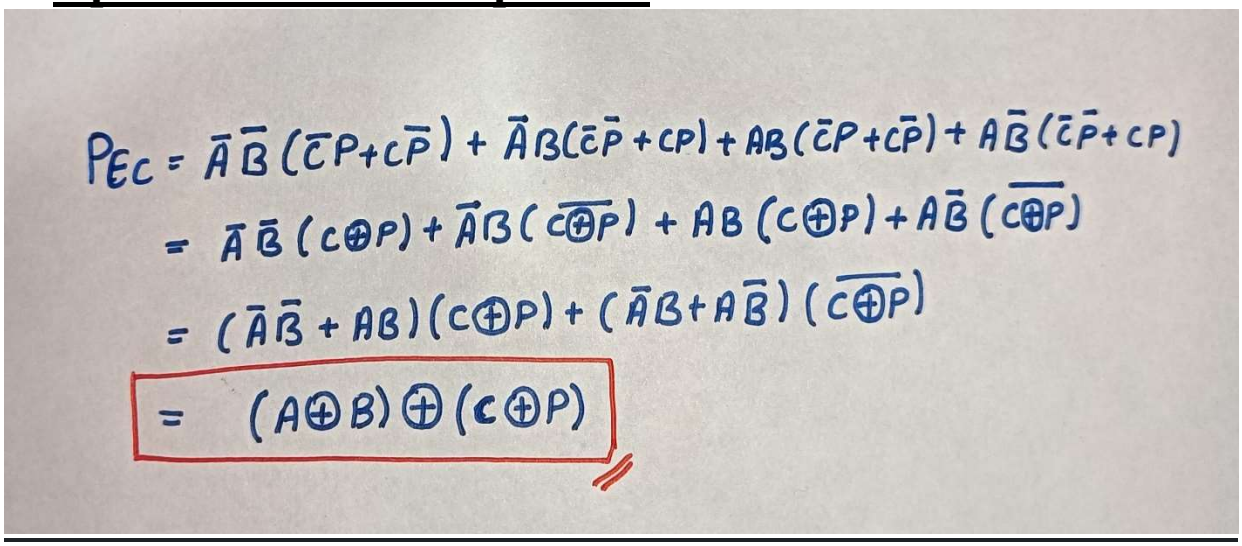
1.3 Objective:

This project aims to design, simulate, and analyze a parity checker for a 3-bit data word using the Microwind tool. Herein, the specific aims will be:To understand how parity checking plays a role in error detection and data integrity.To apply the principles of VLSI design in implementing a 3-bit parity checker.To use the Microwind tool for designing, simulation, and in the validation of the parity checker circuit. The following solution is aimed at understanding the working of the above circuitry for checking the occurrence of an error in a digital system.

1.4 Motivation:

Digital communication systems have seen rapid growth, for which reliable data transmission has also emerged as a key demand. Mechanisms for error detection, such as parity checkers, therefore, have become extremely important in ascertaining data integrity. The work here could well be inspired by an urge to investigate how VLSI design finds practical applications in developing appropriate error-detection circuits. Besides, Microwind is a very easy platform on which to design and simulate VLSI circuits; thus, it will be very suitable for students and professionals who would like to develop their knowledge in digital circuit design. The project will provide us with hands-on experience in using Microwind and enhance our knowledge in VLSI-based error detection.

2. **Optimised Boolean equation.**



Even Parity Checker

Consider any three input messages along with an even parity bit generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit, which then checks for the possibility of an error on the data. Since the data is transmitted with even parity, four bits received at the circuit must have an even number of 1s.

If any error has occurred then the received message contains odd number of 1s. The output of the parity checker is represented as PEC or Parity Error Check.

A	B	C	P	PEC Cp
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

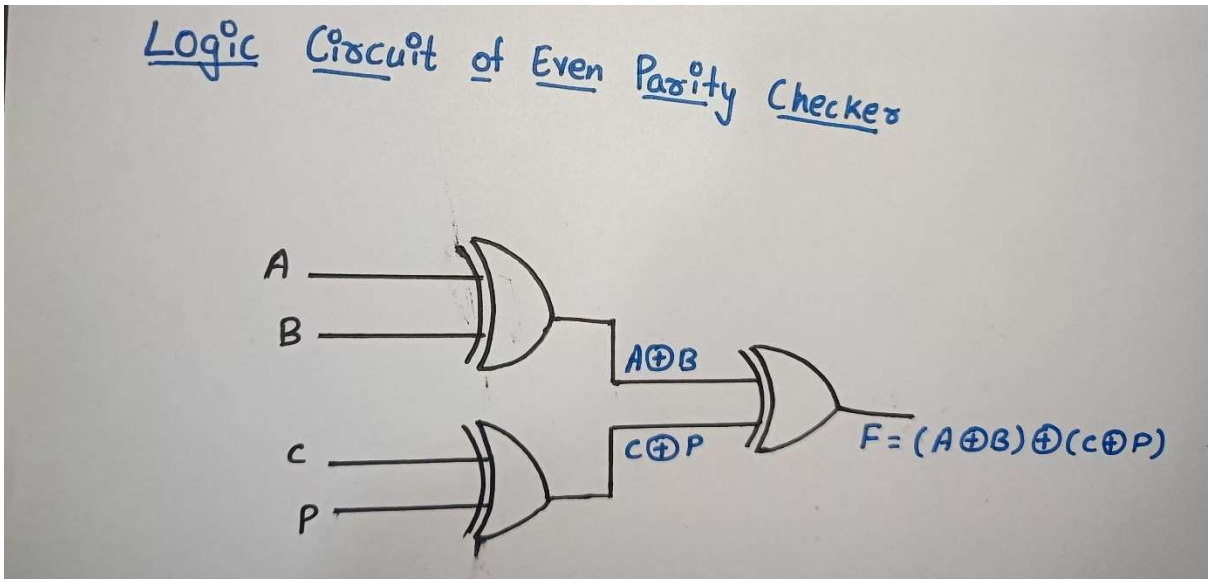
Odd Parity Checker

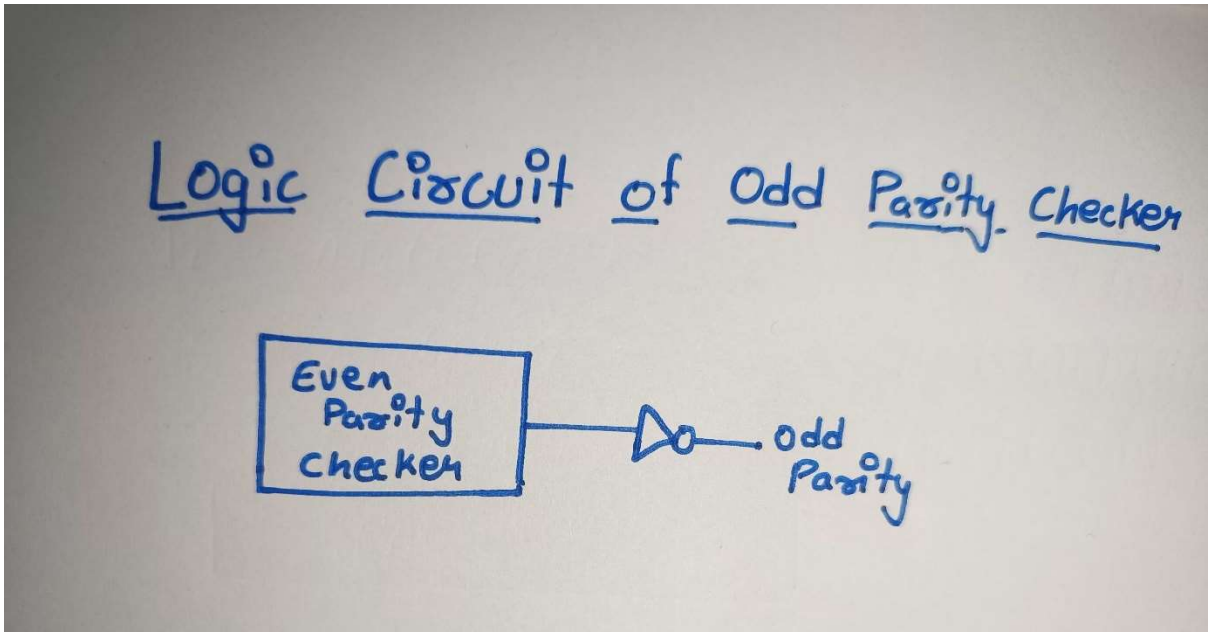
Assume that a three-bit message with an odd parity bit is transmitted from the transmitting end. The odd parity checker circuit receives these 4 bits and checks whether any error is present in the data.

If the total number of 1s in the data is odd, then it indicates no error, but if the total number of 1s is even, then it indicates the error since the data is transmitted with odd parity at the transmitting end.

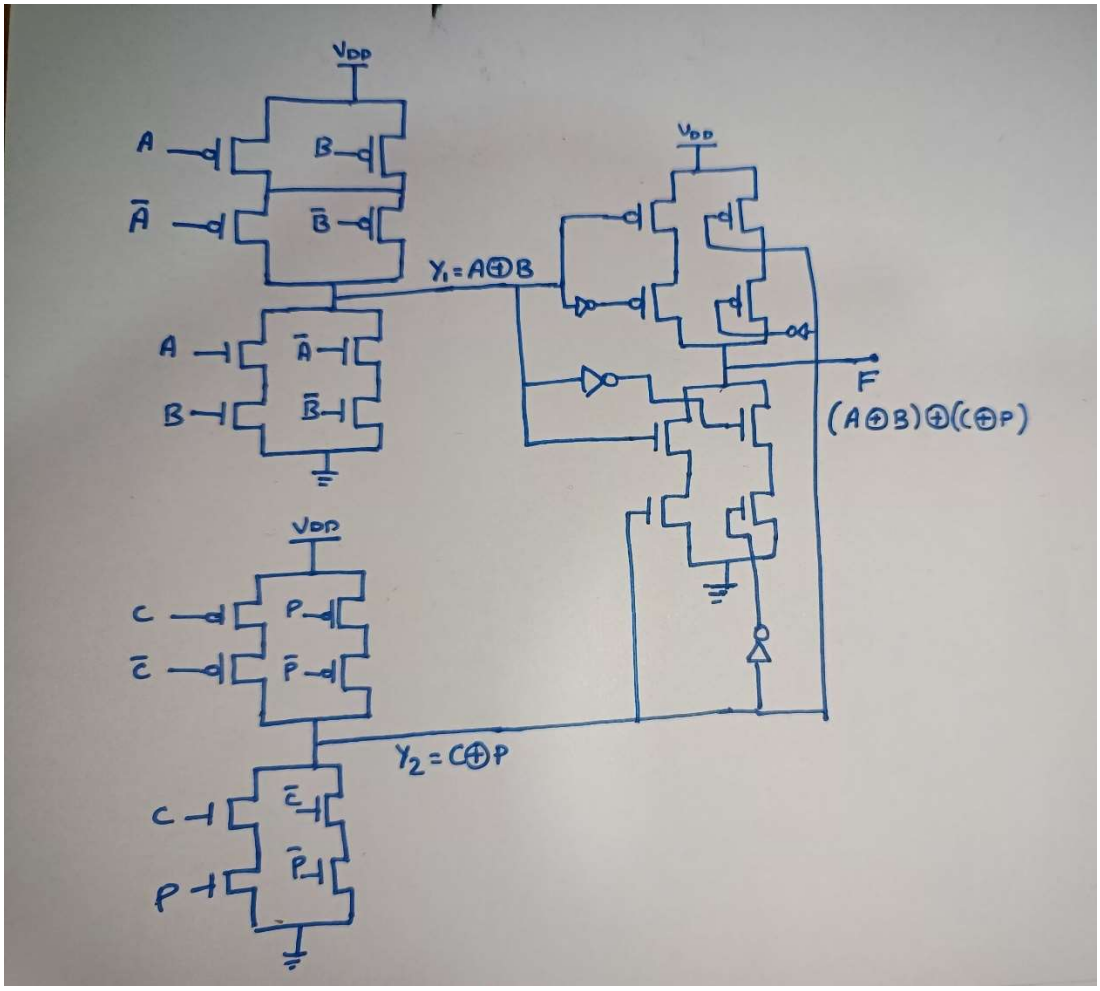
A	B	C	P	PEC Cp
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

3. Optimized gate-level circuit diagram.

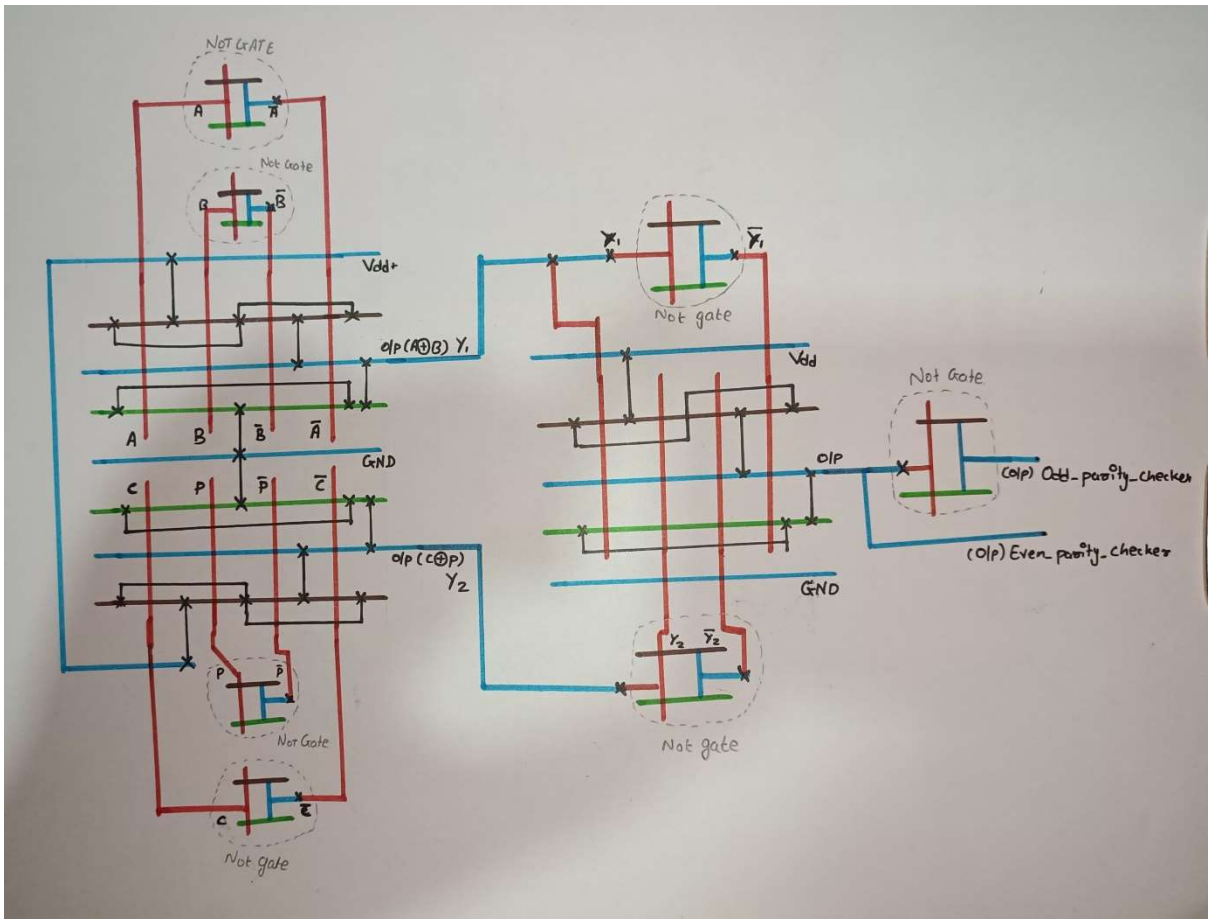




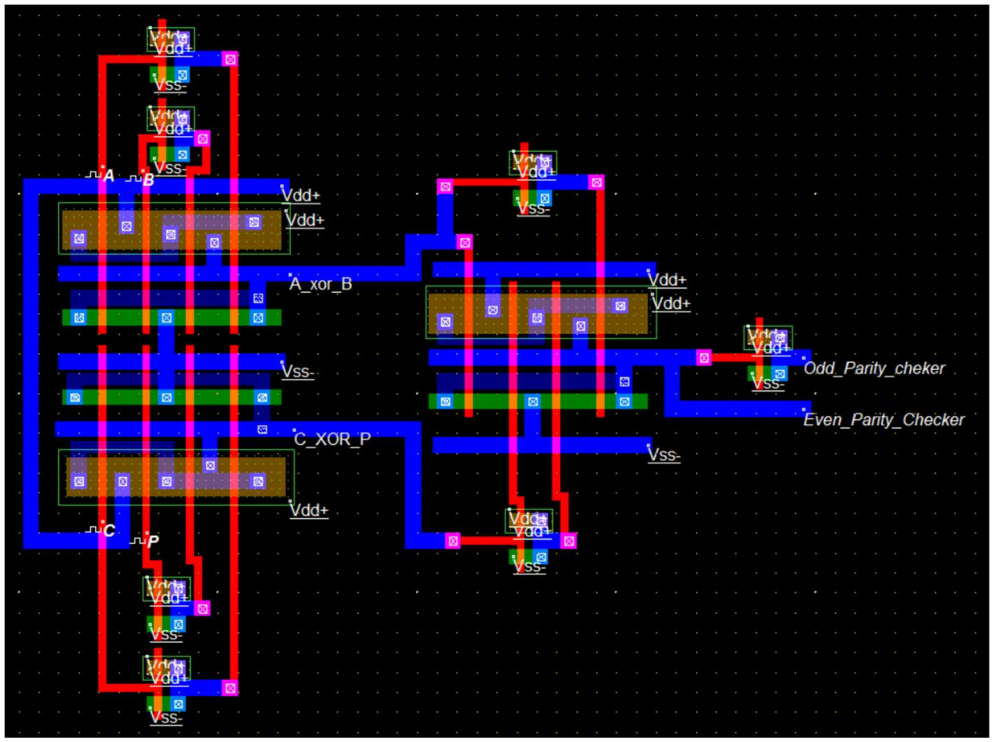
4. Transistor level CMOS circuit for down counter:

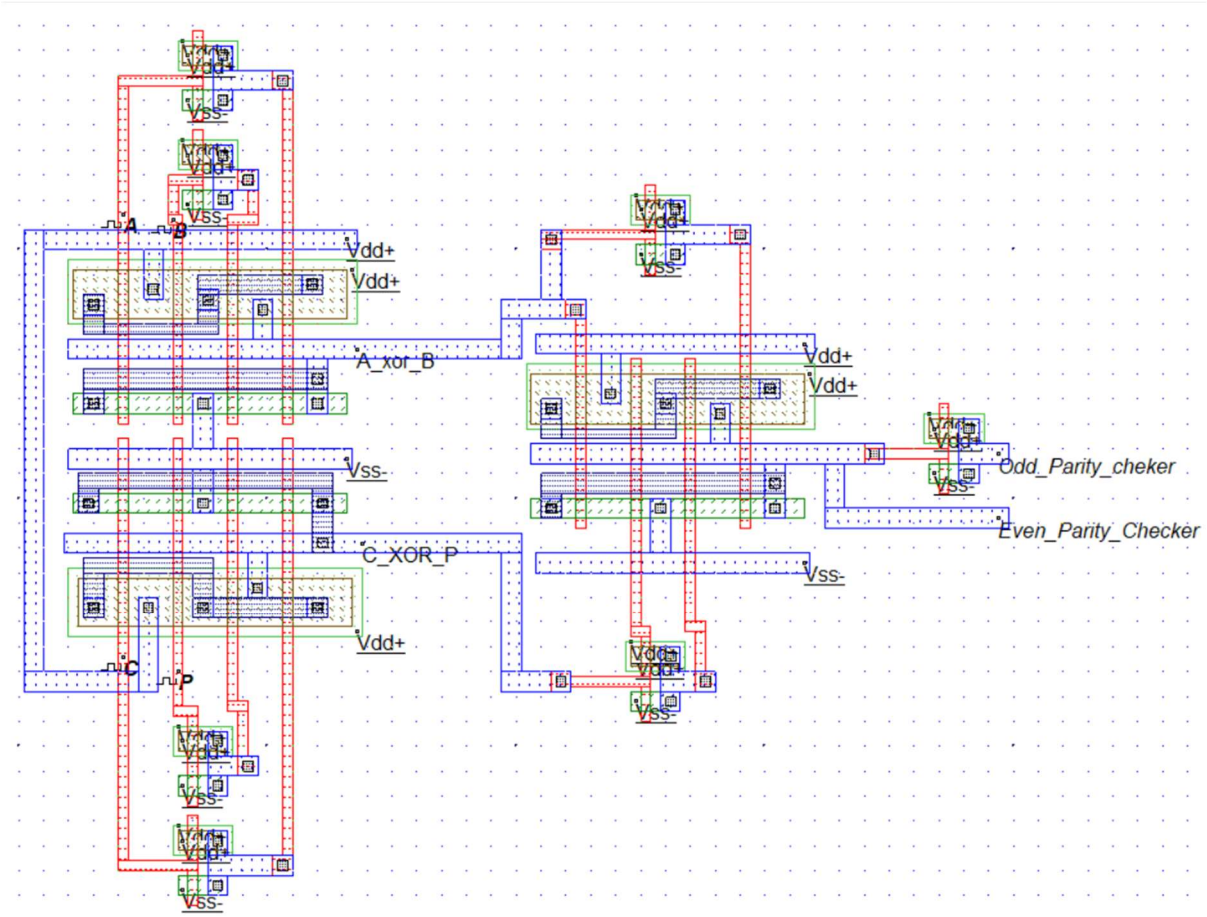


5. Stick diagram

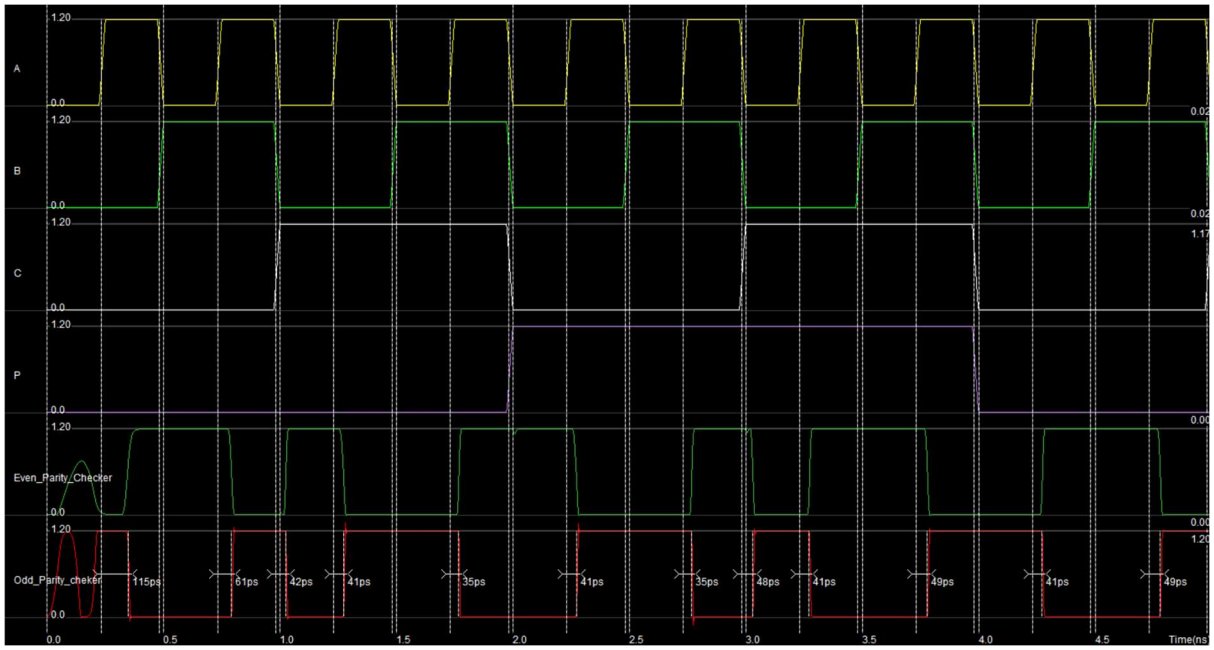


6. Prepare the layout using micro-wind.





7. Simulation of the layout.



8. Measure the rise time, fall time

Sr no	Technology	tphl	tplh	Parity
1	120nm	41	49	ODD PARITY
2	180nm	83	135	
3	350nm	50	184	
4	120nm	49	41	EVEN PARITY
5	180nm	135	83	
6	350nm	184	50	

Conclusion

The project takes into consideration the design and implementation of a parity checker for a 3-bit data word using the Microwind tool within the VLSI design framework. We have followed the VLSI design principles to come up with a functional and efficient circuit capable of detecting single-bit errors on transmitted data. Therefore, we underscored how crucial this process of error detection in digital systems can get and gained some valued experience with Microwind, a powerful tool in VLSI circuit design and simulation.

The project focused on the practical challenges and considerations of the design of the error detection circuits while keeping in mind circuit complexity and optimization of its performance. In conclusion, the project laid very good groundwork on the methodologies of VLSI design and proved a simple technique of parity checking but very important in ensuring that data integrity is ensured during digital communications. Knowledge of such would be very important for subsequent work as we go further to explore more complex VLSI designs and other applications dealing with error detection and correction.

References

[1]CMOS digital integrated circuit by Sung-Mo Kang

[2]Internet sources