

VHDL Codes For OR gate and X-OR gate

THEORY:

VHDL:-

It stands for very High speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). It is a language that describes the behaviour of electronic circuits, most commonly digital circuits. VHDL is used as a design entry format by a variety of EDA tools, including synthesis tools such as quartus prime integrated synthesis, simulation tools, and format verification tools.

The basic concepts of VHDL are:-

- interfaces
- Modeling (Behaviour, Dataflow, structure)
- Test Benches.
- Analysis, elaboration, simulation.
- synthesis.

OBSERVATION:

VHDL Code for OR gates:

```
library IEEE;  
use IEEE.STD_LOGIC_1164.all;  
entity OR_GATE is  
    port (A: in STD_LOGIC;  
          B: in STD_LOGIC;  
          Y: out STD_LOGIC);
```

```
end OR_GATE;
```

architecture beh. OR_GATE of OR_GATE is
begin

$y \leq A \text{ or } B;$
end beh. OR_GATE;

VHDL code for X-OR gates:

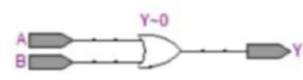
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity X-OR_gate is
 port (a: in STD_LOGIC;
 b: in STD_LOGIC;
 y: out STD_LOGIC;

 ← end X-OR_gate
architecture beh of X-OR_gate is
begin
 $y \leq a \text{ xor } b;$
end beh;

DISCUSSION AND CONCLUSION:

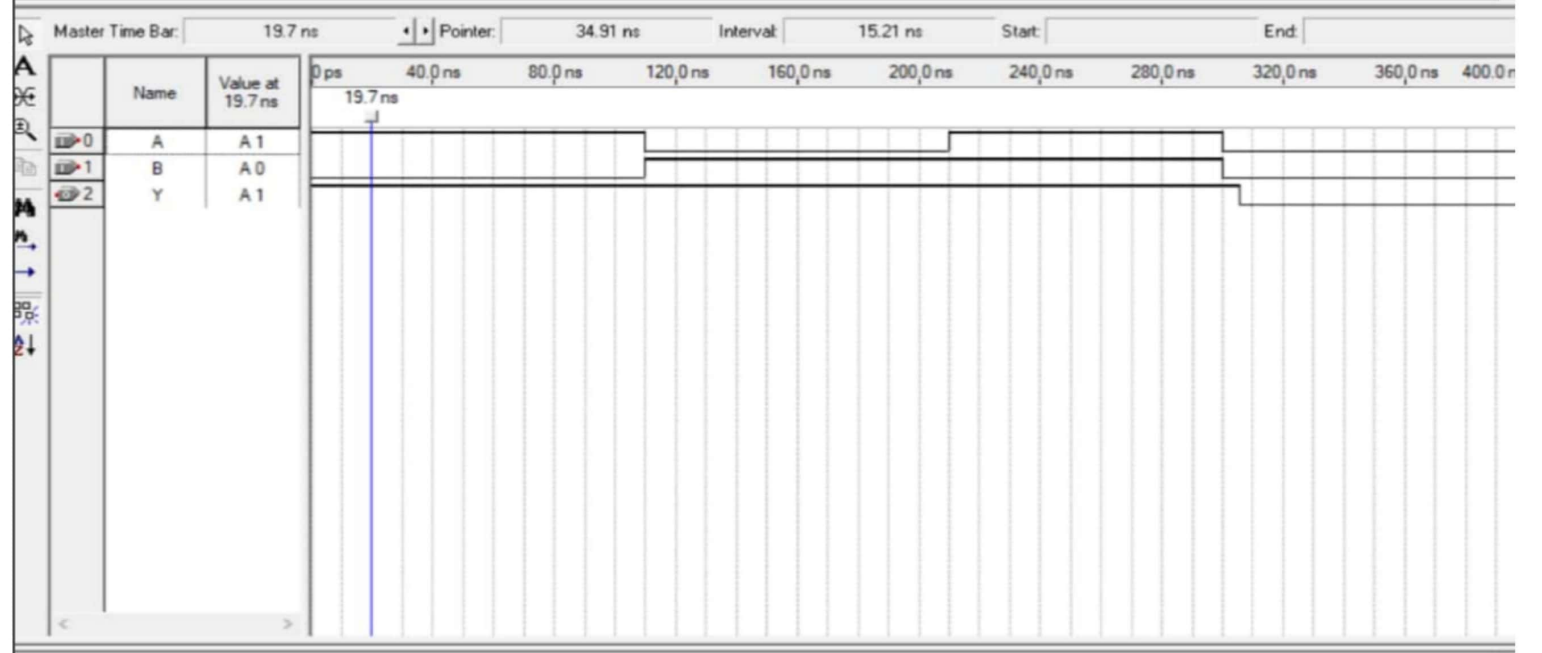
In this way, we are familiarized with OR and X-OR gates in VHDL.

- Hierarchy List
- project1_OR_GATE
 - Primitives
 - Pins
 - Nets



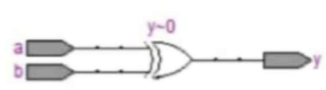
Simulation Waveforms

Simulation mode: Timing



Hierarchy List

- x_or_gate
- Primitives
- Pins
- Nets



[Compilation Report - Flow Summary](#)
[x_or_gate.vwf](#)
[Simulation Report - Simulation Wave...](#)

Simulation Waveforms

Simulation mode: Timing

