VHDL Codes For OR gate and X-OR gate

THEORY:

VHDL:-

It stands for very High speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). It is a language that describes the behaviour of electronic circuits, most commonly digital circuits. VHDL is used as a design entry format by a variety of EDA tools, including synthesis tools such as quartus prime integrated synthesis, simulation tools, and formal verification tools.

The basic concepts of VHDL are:-

- interfaces
- Modeling (Behaviour, Dataflow, structure)
- Test Benches.
- Analysis, elaboration, simulation.
- synthesis.

OBSERVATION:

VHDL code for OR gates:

```
Library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity OR_GATE is
        port (A: in STD_LOGIC;
              B: in STD_LOGIC;
              Y: out STD_LOGIC);

end OR_GATE;
```

```
architecture beh. OR_GATE of OR_GATE is
begin
        Y <= A or B;
      end beh. OR_GATE;
```

VHDL code for X-OR gates:

```
library IEEE;
use IEEE. STD_LOGIC_1164. all;
entity X_OR_gate is
        port (a: in STD_LOGIC;
              b: in STD_LOGIC;
              y: out STD_LOGIC;
  ⟵ end X_OR_gate
architecture beh of X_OR_gate is
begin
      y <= a  xor b;
      end beh;
```

DISCUSSION AND CONCLUSION:

In this way, we are familiarized with OR and X-OR gates in VHDL.