

Name of the Subject:

Name of the Faculty: C. Ashok Kumar

Topic:

Unit No: 4

Lecture No:

Link to Session

Planner (SP): S.No.... of SP

Book Reference:

Date Conducted:

Page No: 1

CONSTRUCTION:

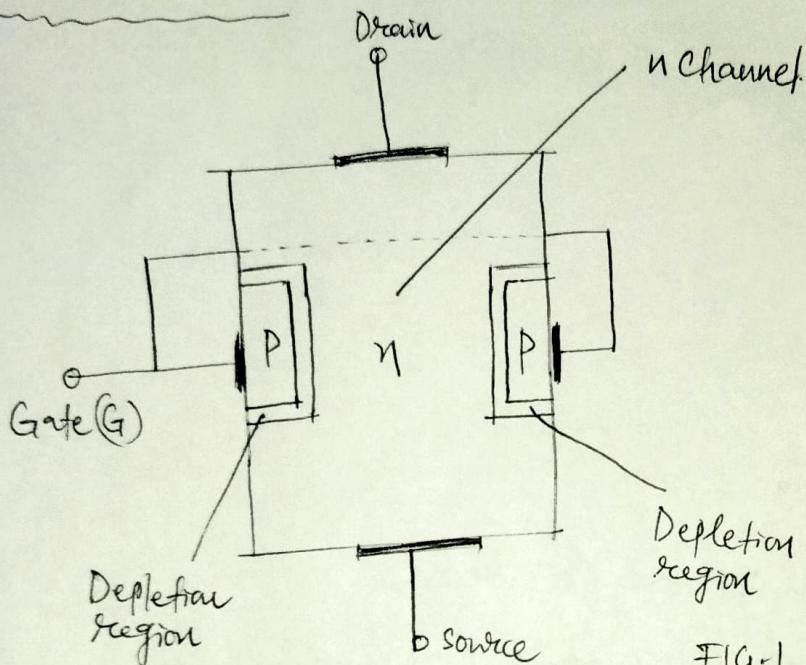
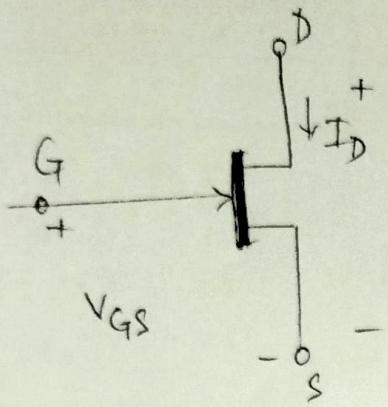


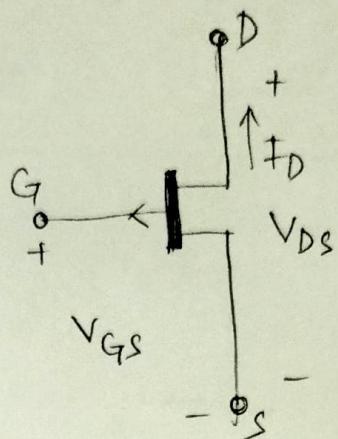
FIG-1

- Major part of structure is the n-type material, which forms the channel between the embedded layers of P-type material.
- Top of n-type channel is connected through an ohmic contact to a terminal referred as the drain(D), whereas lower end of same material is connected through an ohmic contact to a terminal referred to as the source(S).
- The two P-type materials are connected together and to the Gate(G) terminal.
- In the absence of any applied potentials the JFET has two p-n junctions under no-bias condition. The result is depletion region at each junction as shown in figure.

JFET Symbols



n- channel JFET



p- channel JFET

JFET operating Characteristics

There are three basic operating conditions.

- ① $\rightarrow V_{GS} = 0$, V_{DS} increasing to some positive value
- ② $\rightarrow V_{GS} < 0$, V_{DS} at some positive value.
- ③ \rightarrow voltage controlled resistor.

① $V_{GS} = 0$, V_{DS} increasing to some positive value

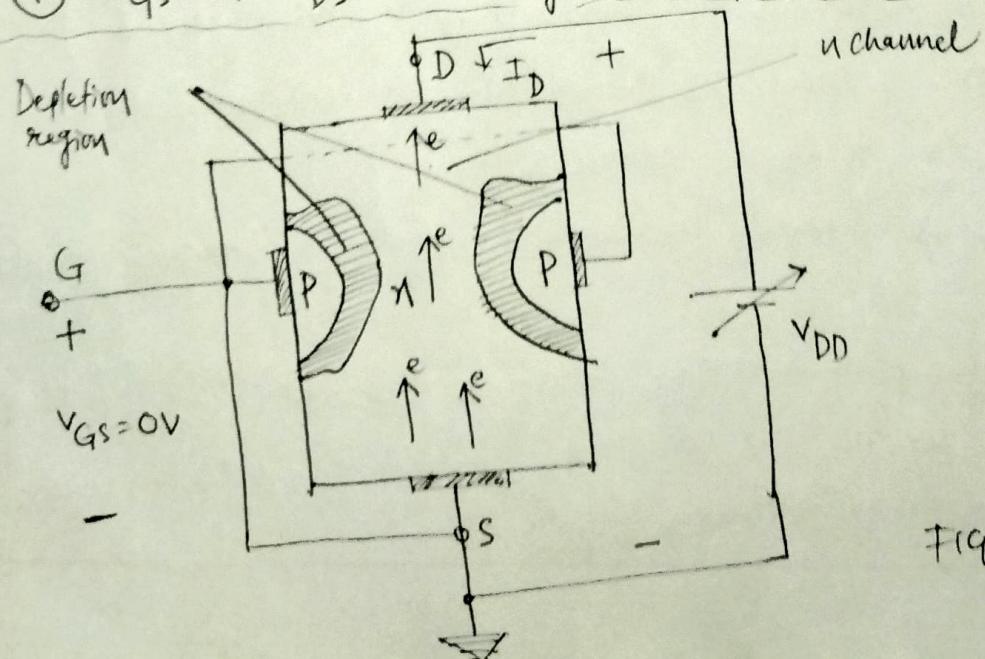


FIG. 2

Name of the Subject:
Name of the Faculty:
Topic:

Unit No:
Lecture No:
Link to Session
Planner (SP): S.No.... of SP
Book Reference:
Date Conducted:
Page No: 2

As shown in Fig, a Positive Voltage V_{DS} is applied across the channel and gate is connected directly to the source to establish the condition $V_{GS} = 0V$. V_{DS} increased from 0V to few volts, Then,

- The depletion region between P-gate and n-channel increases
- Increasing the depletion region, decreases the size of n-channel which increases the resistance of n-channel.
- Even though, n-channel resistance is increasing, the current (I_D) from source to drain through the n-channel is increasing. This is because V_{DS} is increasing

Pinchoff : If $V_{GS} = 0$ and V_{DS} is further increased to a more positive voltage, then it appears that two depletion regions would touch as shown in fig. 3 , a condition referred to as Pinchoff will result. The level of V_{DS} that establishes this condition is referred to as Pinch-off voltage and denoted by V_p .

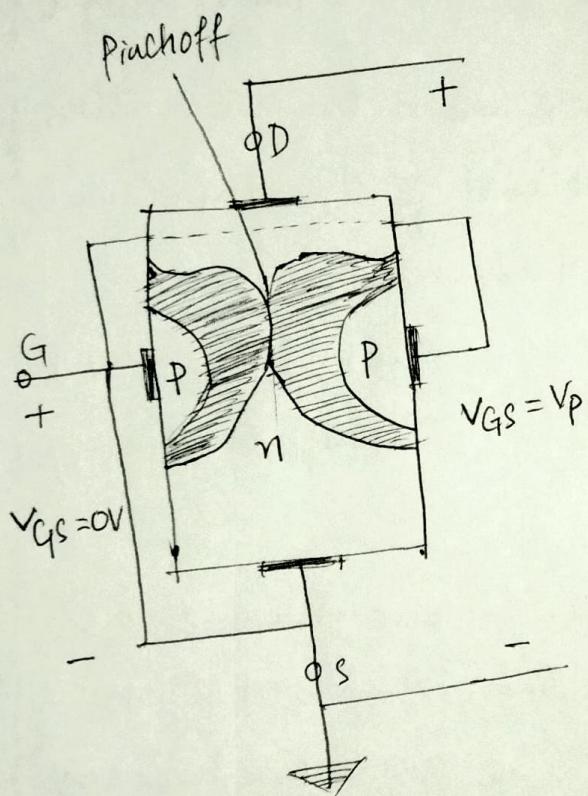
Depletion regions pinches off the n-channel. Hence, I_D does not drop off to zero but instead it maintains the saturation level.

When $V_{DS} > V_p$, level of I_D remains constant (same).

As shown in Fig 4, current is fixed at $I_D = I_{DSS}$.

I_{DSS} = Drain to source current with short circuit -
- connection from gate to source.

I_{DSS} is maximum drain current for a JFET defined by
conditions $V_{GS} = 0V$ and $V_{DS} > |V_p|$



Pinch off ($V_{GS} = 0V, V_{DS} = V_p$)

Fig. 3

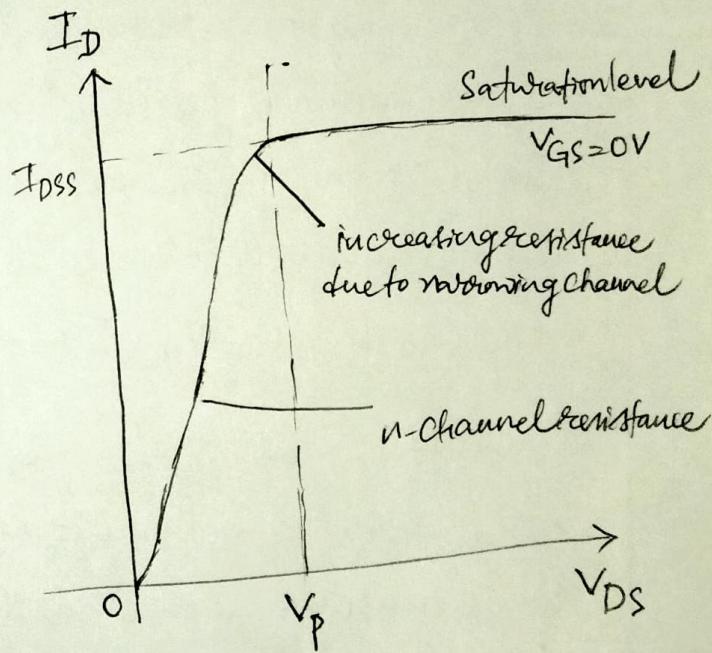
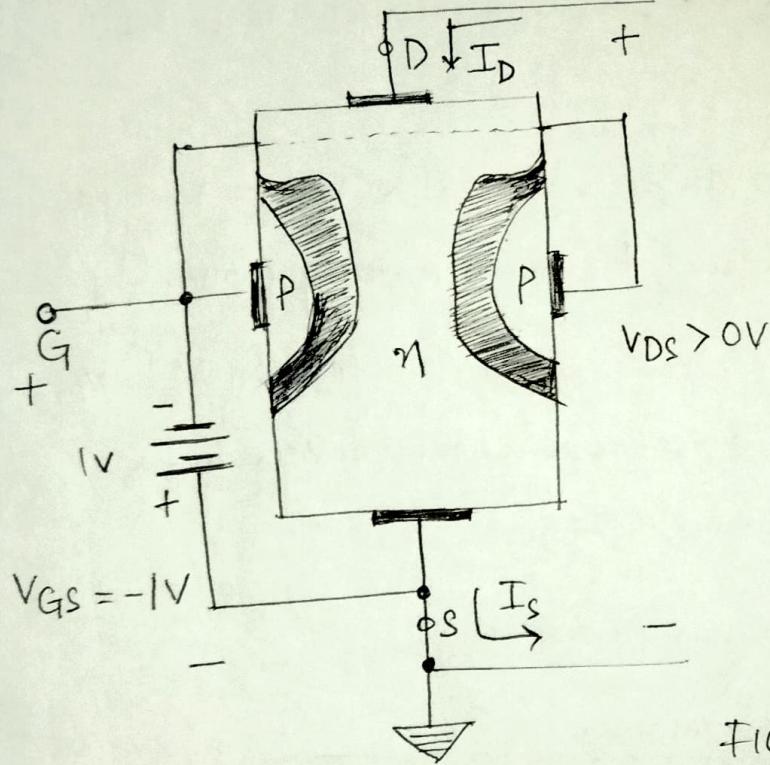


Fig. 4

Name of the Subject:
Name of the Faculty:
Topic:

Unit No:
Lecture No:
Link to Session
Planner (SP): S.No... of SP
Book Reference:
Date Conducted:
Page No: 3

② $V_{GS} < 0$, V_{DS} at some positive value.



A negative voltage of $-1V$ is applied between gate and source terminals for a lower level of V_{DS} .

FIG.5

The effect of applied negative bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0V$ but at lower levels of V_{DS} .

The result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS} as shown in fig.

Example : If $V_p = 4V$, $V_{DS} = 4V$ when $V_{GS} = 0V$

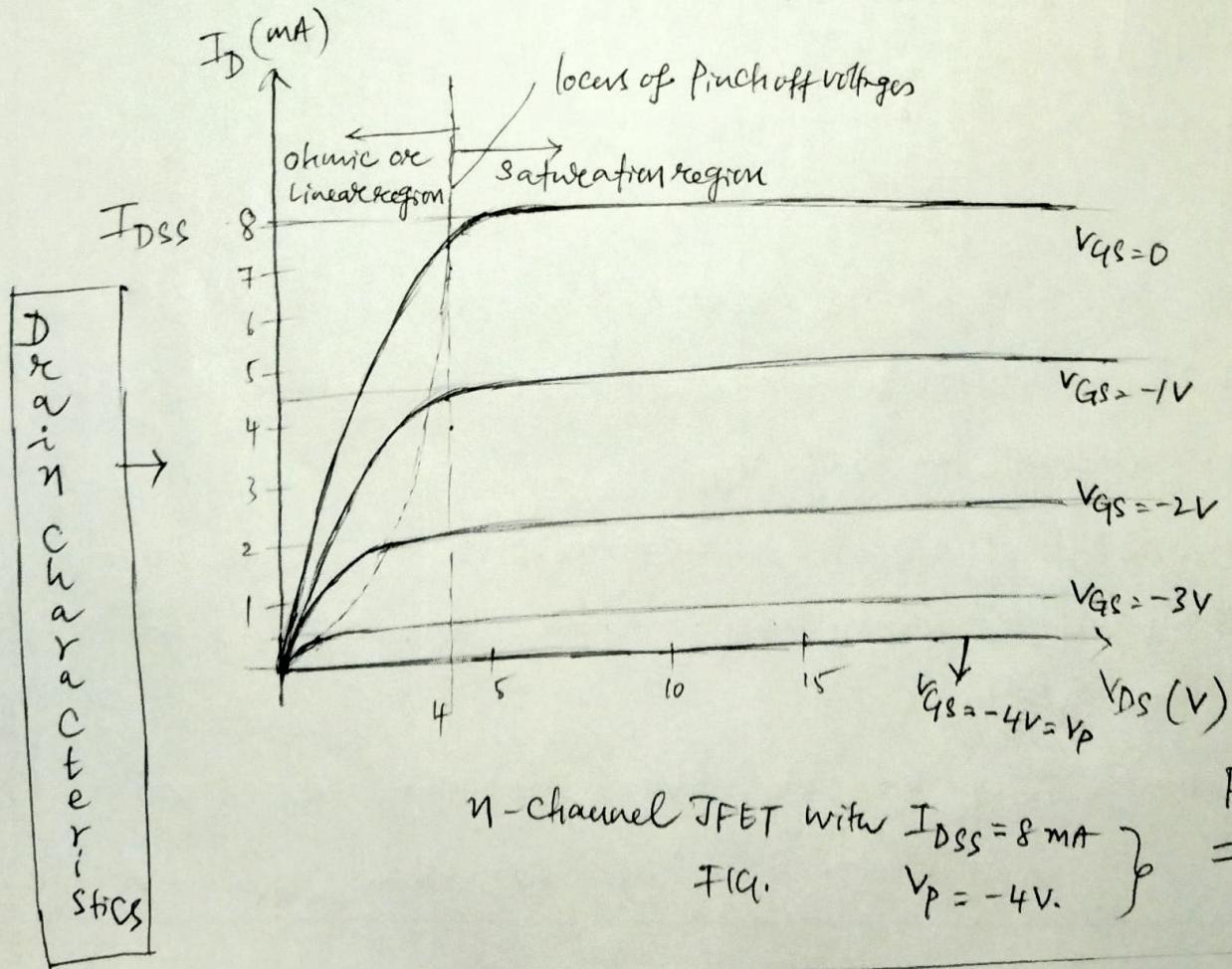
$V_{DS} = 3V$ when $V_{GS} = -1V$

The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative.

From the Fig. 6, we see that Pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative.

Finally, when $V_{GS} = -V_p$, sufficient negative voltage enough to establish a saturation level that is essentially 0 mA. (I_d)

- * The level of V_{GS} that results in $I_D = 0 \text{ mA}$ is defined by $V_{GS} = V_p$, with V_p being a negative voltage for n-channel devices and a positive voltage for P-channel JFETs.



Name of the Subject:
Name of the Faculty:
Topic:

Unit No:
Lecture No:
Link to Session
Planner (SP): S.No.... of SP
Book Reference:
Date Conducted:
Page No: 4

Transfer Characteristics

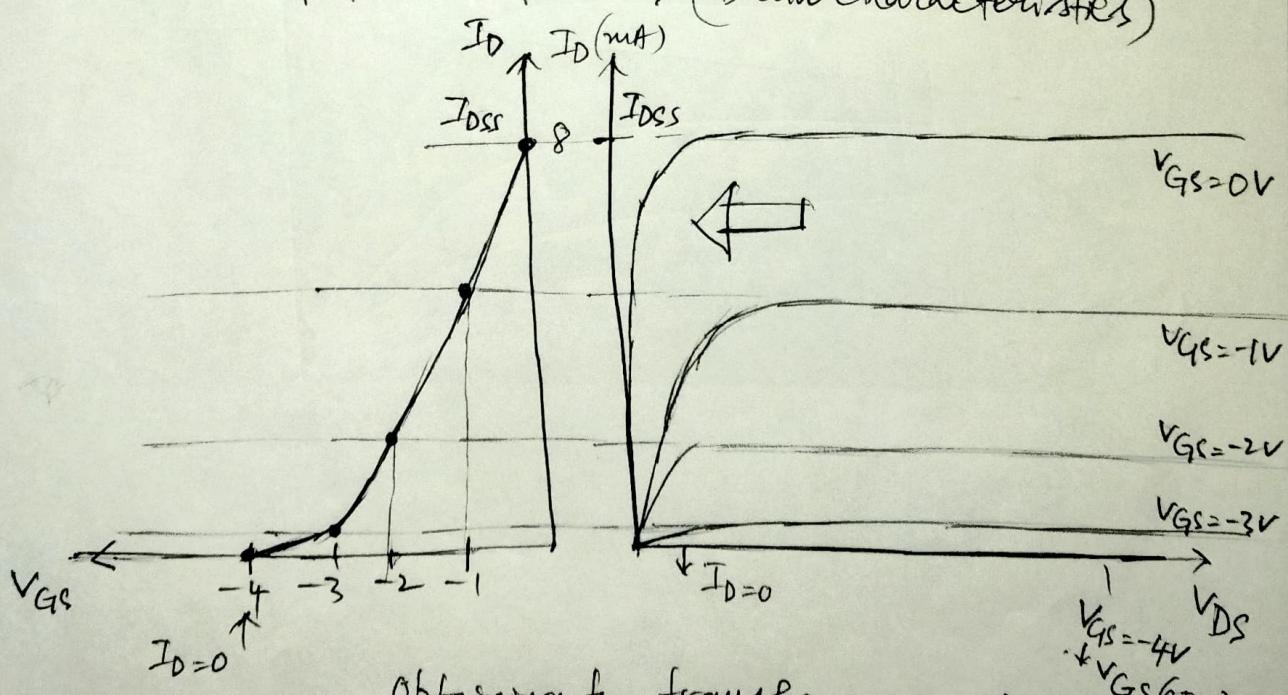
The relationship between I_D & V_{GS} is defined by Shockley's equation.

control variable.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

↑
Constant

The transfer curve can be obtained using Shockley's equation or from output characteristics (Drain characteristics)



Obtaining the transfer curve from Drain Characteristics.

When $V_{GS} = 0V$, $I_D = I_{DSS}$

When $V_{GS} = V_p = -4V$, $I_D = 0 \text{ mA.}$

* Gate cut off voltage:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)$$

After a certain gate-to-source voltage (V_{GS}), the drain current I_D becomes zero. This voltage is known as Cutoff Voltage $\underline{V_{GS(\text{off})}}$

Name of the Subject:

Name of the Faculty:

Topic:

Unit No:

Lecture No:

Link to Session

Planner (SP): S.No.... of SP

Book Reference:

Date Conducted:

Page No: 5

(3) Voltage-controlled resistor

- The region to the left of Pinch off locus of Fig. is referred as the Ohmic or voltage controlled resistance region.
- In this region, JFET can be employed as Variable Resistor, whose resistance is controlled by applied gate-to-source voltage.
- As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding to an increasing resistance level.

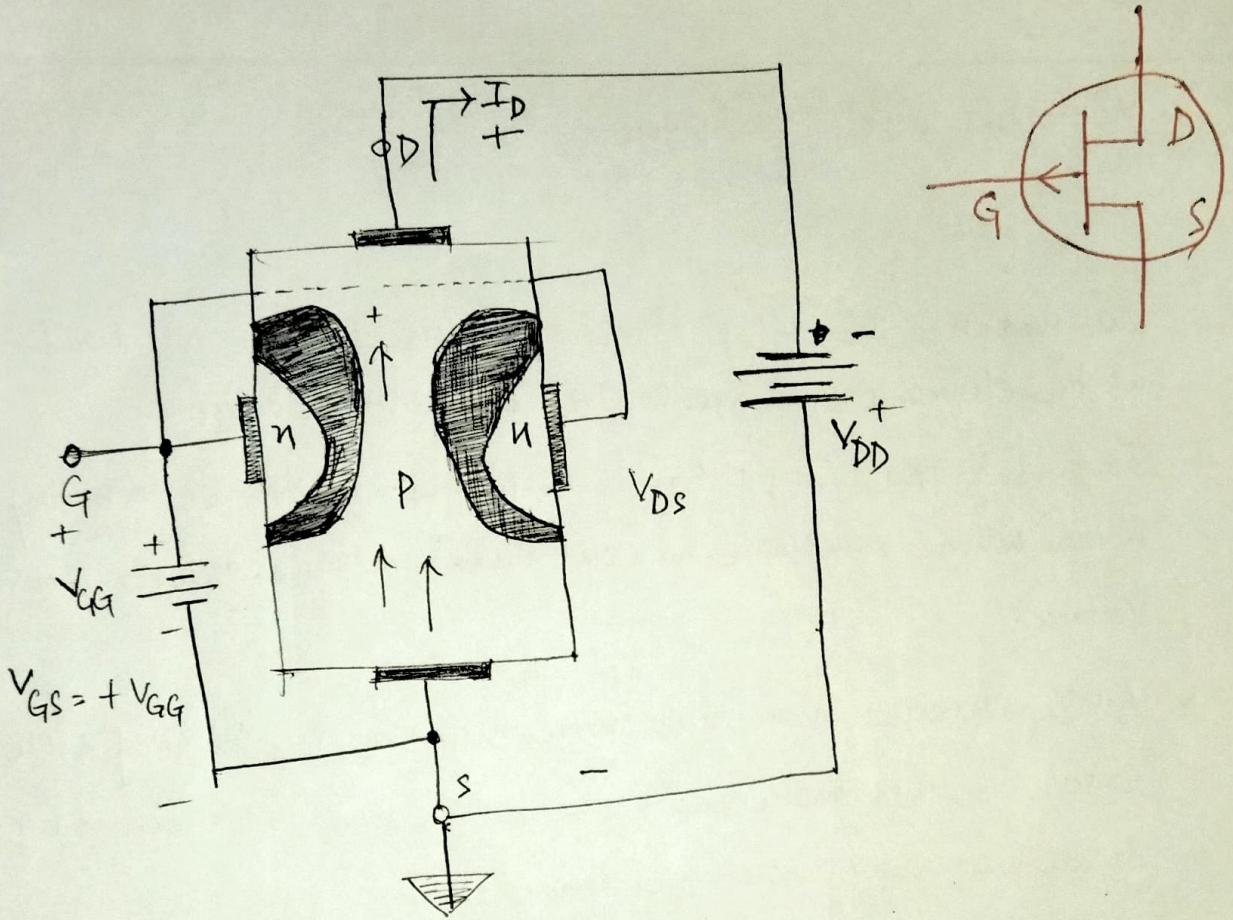
$$\rightarrow R_d = \frac{R_0}{\left(1 - \frac{V_{GS}}{V_p}\right)^2} \quad \text{--- (1)}$$

Where R_0 is the resistance with $V_{GS} = 0$ V

& R_d is the resistance at particular level of V_{GS}

$$\rightarrow \text{At } V_{GS} = V_p \Rightarrow R_d = \infty, I_d = 0$$

P-Channel JFET

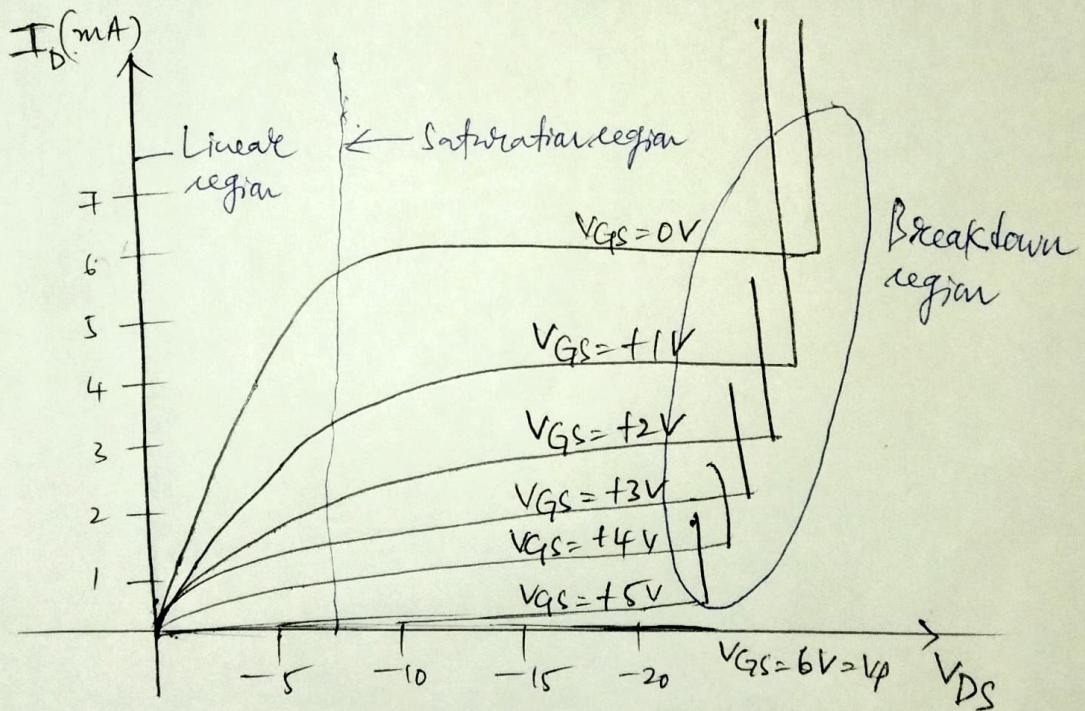


- It is constructed in exactly same manner as n-Channel JFET but with reversal of P- and n-type materials as shown in fig.
- Polarities of voltages V_{GS} & V_{DS} are reversed, I_D direction reversed.
- Channel width is reduced by increasing positive voltages from gate to source and negative voltages for V_{DS} .

Name of the Subject:
Name of the Faculty:
Topic:

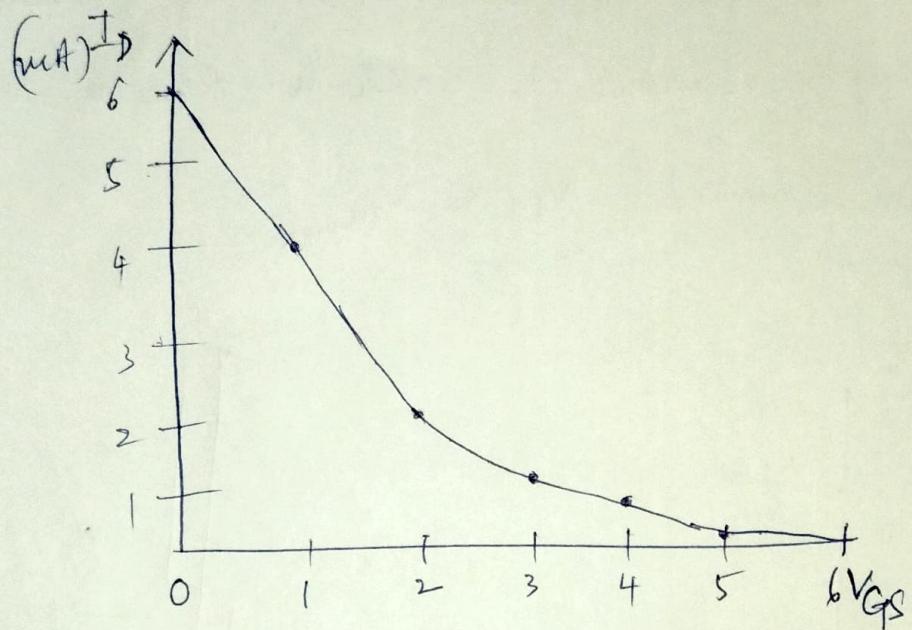
Unit No:
Lecture No:
Link to Session
Planner (SP): S.No.... of SP
Book Reference:
Date Conducted:
Page No: 6

- At high levels of V_{DS} the curves suddenly rise vertically indicating the occurrence of breakdown. (rise in current I_D)
- This can be avoided if $V_{DS} < V_{DS_{max}}$



P-Channel JFET characteristic with $I_{DSS} = 6\text{mA}$
and $V_p = +6\text{V}$

Transfer Characteristics of P-Channel JFET



$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Name of the Subject:

Name of the Faculty: C. Ashok Kumar

Topic:

Unit No:

Lecture No:

Link to Session

Planner (SP): S.No.... of SP

Book Reference:

Date Conducted:

Page No: 7

Characteristic Parameters of JFET

① Transconductance

It is ratio of change in drain current ΔI_D to change in the gate-to-source voltage (ΔV_{GS}) at a constant drain-to-source voltage ($V_{DS} = \text{constant}$)

$$\left. \begin{aligned} g_m &= \frac{\Delta I_D}{\Delta V_{GS}} \text{ at Constant } V_{DS} \\ &= \frac{\frac{dI_D}{dV_{GS}}}{\text{at } V_{DS} = \text{constant}} \end{aligned} \right\} \quad \textcircled{1}$$

We have $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$

$$g_m = \frac{\frac{dI_D}{dV_{GS}}}{\text{at } V_{DS} = \text{constant}} = -2 \frac{I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p} \right)$$

At $V_{GS} = 0$, g_m becomes max value as g_{m0}

$$\left. \begin{aligned} \therefore g_{m0} &= -2 \frac{I_{DSS}}{V_p} \end{aligned} \right\}$$

② Drain resistance (r_d): This is the ratio of change of drain-to-source voltage (ΔV_{DS}) to change of drain current (ΔI_D)

$V_{GS} = \text{constant}$.

$$\left. \begin{aligned} r_d &= \frac{\Delta V_{DS}}{\Delta I_D} \text{ at Constant } V_{GS} \end{aligned} \right\} \quad \textcircled{2}$$

③ Amplification factor (μ):

It is defined as ratio of change of drain voltage (ΔV_{DS}) to change of gate voltage (ΔV_{GS}) at a constant drain current ($I_D = \text{constant}$)

$$\boxed{\mu = \left| \frac{\Delta V_{DS}}{\Delta V_{GS}} \right| \text{ at constant } I_D} \quad \text{--- (3)}$$

Relation among μ , r_d , g_m :-

We know that

$$\begin{aligned} \mu &= \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \\ &= r_d \times g_m \end{aligned}$$

$$\left(\because r_d = \frac{\Delta V_{DS}}{\Delta I_D}, g_m = \frac{\Delta I_D}{\Delta V_{GS}} \right)$$

So, $\boxed{\mu = g_m \times r_d}$ ✓

COMPARISON BETWEEN FET & BJT

FET	BJT
1. FET is an unipolar semiconductor device because its operation depends upon the flow of majority carriers i.e either holes or electrons as the case may be.	1. BJT is a bipolar semiconductor device because the current constituting elements are both majority carriers as well as minority carriers in this case.
2. The input impedance of FET is much larger (in the range of Megohms) than BJT. The reason is that input terminal i.e gate to source of FET is reverse biased, which offer ideally infinite resistance.	2. The input impedance of BJT is very less in comparison to FET.
3. FET is voltage controlled device.	3. BJT is current controlled device.
4. FET is less noisy. Because there are no junctions.	4. BJT is much noisy than FET.
5. Higher frequency response	5. Frequency variation affects the performance.
6. Good thermal stability because of absence of minority carriers.	6. Temperature dependent, thermal runaway may cause.
7. Costlier than BJT.	7. Relatively Cheaper.

FET	BJT
8. Occupies less space (small size). So, it is used in ICs.	8. Comparatively bigger.
9. $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$	9. $I = I_o (e^{V/nV_T} - 1)$
10. No offset voltage, so it works better as a switch.	10. There is always an offset voltage before switching.
11. Small gain bandwidth product.	11. Greater than FET

* FET applications *

- 1) Due to their high input impedance, FETs are commonly used as input amplifiers in devices i.e. Voltmeters, Oscilloscopes, and other measuring devices.
- 2) FETs are also used in radio frequency amplifiers for FM devices.
- 3) FETs are used for mixer operation of FM and TV Receivers.
- 4) FET is a voltage controlled device due to this it is used in Operational amplifiers as voltage variable resistors.
- 5) FETs are used in large scale integration (LSI) and computer memories because of its small size.

FET Disadvantages

- 1) It has relatively lower gain bandwidth product compared to BJT.
- 2) FET performance degrades as frequency increases. This is due to the feedback by internal capacitance.
- 3) Transconductance is low, hence voltage gain is low.