



# Performance Analysis of AlGaN/GaN Nanowire HEMTs over Planar AlGaN/GaN HEMT

Analog VLSI and Device Modelling Lab(25VL681)

## Mentor

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# Overview

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# Abstract

## Objective:

- To design, simulate, compare the analysis of both planar and nanowire AlGaN/GaN HEMT structures using TCAD
- To define an appropriate 3D mesh, material regions, and doping profiles for the nanowire geometry.
- To perform electrical characterization by obtaining  $Id-Vg$  and  $Id-Vd$  characteristics under different bias conditions.
- To analyze current conduction and gate control in the nanowire structure.
- To compare the electrical performance of the nanowire HEMT with a conventional planar AlGaN/GaN HEMT, focusing on drain current, transconductance, and threshold voltage.

- **Goal:** To design, simulate and compare planar AlGaN/GaN HEMT vs GaN nanowire (GAA/wrap-gate) HEMT using TCAD.
- **Output:** GAA GaN nanowire HEMT exhibits enhanced gate control, higher transconductance, and improved current modulation compared to the conventional planar AlGaN/GaN HEMT through comprehensive TCAD-based 3D simulation and electrical analysis.

# Project Phases

- **Stage 1 Work:**
  - Analyzed a conventional planar AlGaN/GaN HEMT, focusing on understanding 2DEG formation and planar device behavior
- **Stage 2 Work:**
  - Designed a 3D GaN nanowire HEMT, enabling gate-all-around control and performing a detailed comparative analysis between the planar and nanowire structures to evaluate improvements in electron mobility, gate controllability, doping concentration and transconductance performance.

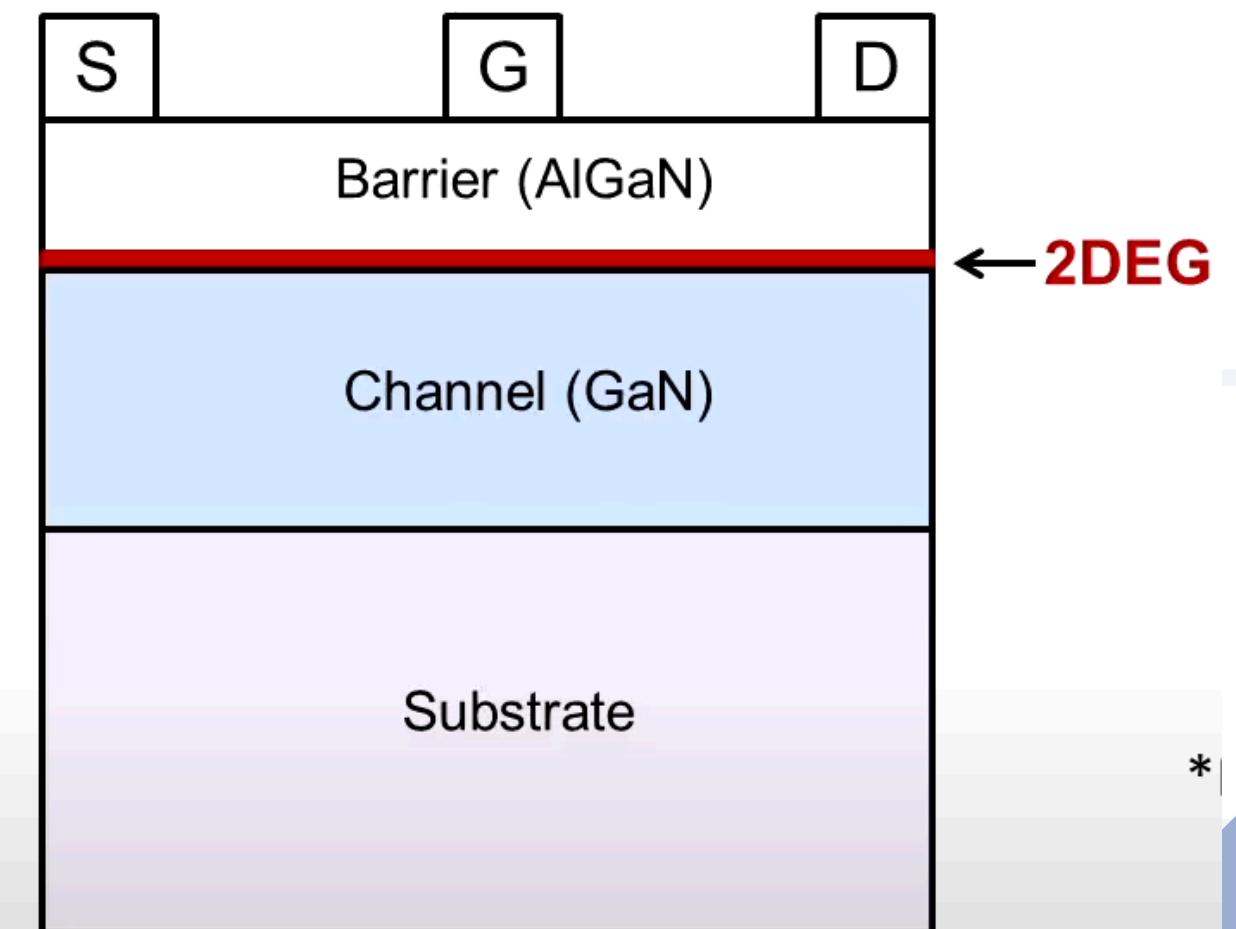
## Introduction- Working of HEMT

- **High Electron Mobility Transistors (HEMTs):**

- Belong to the heterostructure FET family.
- Exploit 2DEG (Two-Dimensional Electron Gas) at the AlGaN/GaN interface for ultra-high mobility.

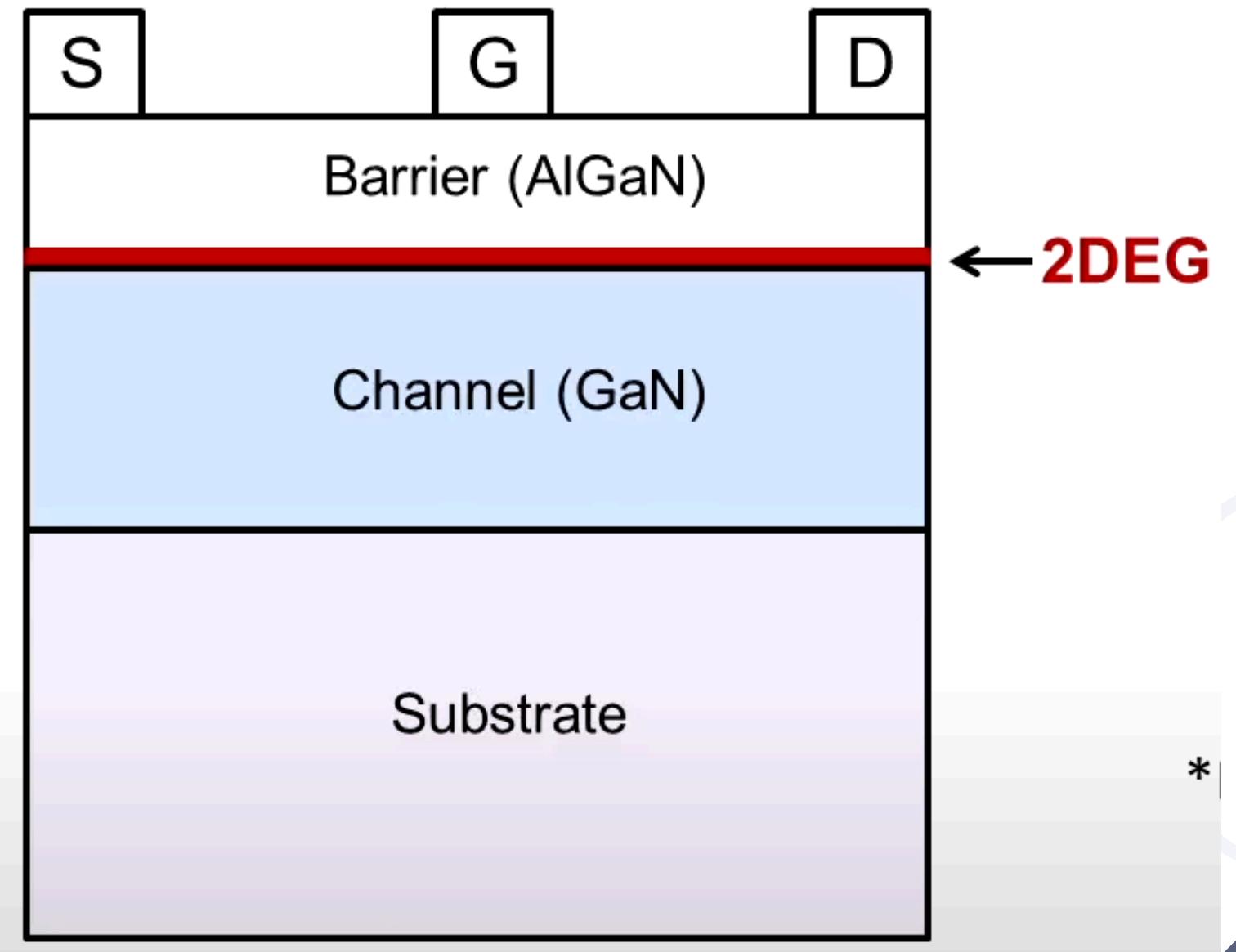
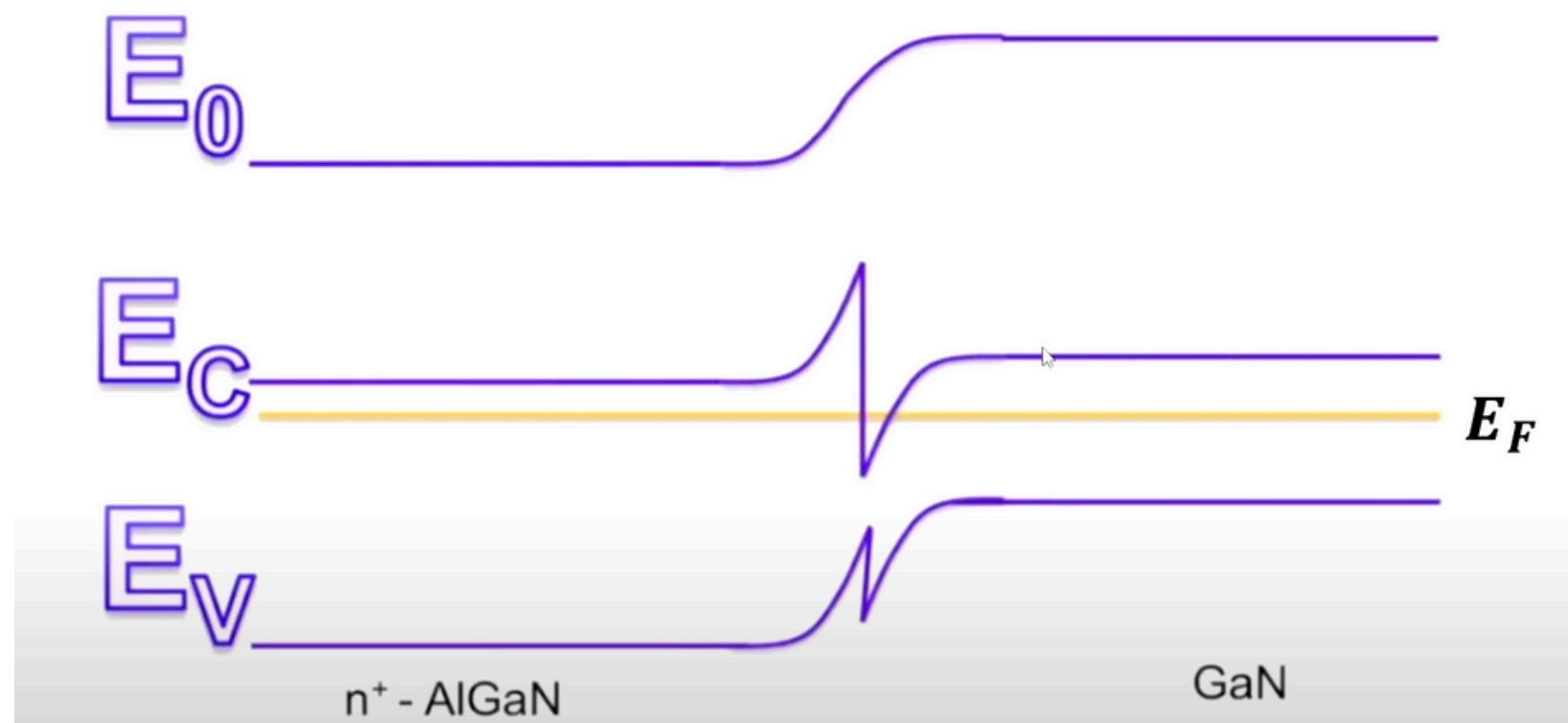
- **Why AlGaN/GaN HEMTs was developed?**

- To achieve very high electron mobility and high-speed switching performance,



# Working Principle

1. Heterojunction Formation
2. DEG Creation
3. Gate Modulation



# Literature Survey

Paper & Publishing Details	Summary	Interface
<p><b>Title:</b> Effects of Interface Traps and Self-Heating on the Performance of GAA GaN Vertical Nanowire MOSFET</p> <p><b>Authors:</b> Terirama Thingujam, Dong-Hyeok Son, Jeong-Gil Kim, Sorin Cristoloveanu, and Jung-Hee Lee</p> <p><b>Journal:</b> IEEE Transactions on Electron Devices, Vol. 67, No. 3, March 2020</p>	<ul style="list-style-type: none"><li>GaN-based gate-all-around (GAA) vertical nanowire MOSFET shows how interface traps and self-heating effects influence device performance.</li><li>Multilevel trap distribution at the <math>\text{Al}_2\text{O}_3/\text{GaN}</math> interface.</li><li>The self-heating simulation showed that optical phonon scattering dominates mobility degradation at high gate voltage.</li></ul>	<ul style="list-style-type: none"><li>The device structure and simulation flow in your ATLAS code follows the same 3D cylindrical GAA nanowire concept.</li><li>The FLDMOB, SRH, AUGER, FERMI, and BGN models used for accurate GaN transport and recombination behavior.</li></ul>

# Literature Survey

Paper & Publishing Details	Summary	Interface
<ul style="list-style-type: none"><li><b>Title:</b> Planar Two-Dimensional Electron Gas (2DEG) IDT SAW Filter on AlGaN/GaN Heterostructure .</li><li><b>Authors:</b> King-Yuen Wong, Wilson Tang, Kei May Lau, and Kevin J. Chen</li><li><b>Conference:</b> IEEE Ultrasonics Symposium, 2007</li><li><b>Affiliation:</b> Hong Kong University of Science and Technology, Hong Kong</li></ul>	<ul style="list-style-type: none"><li>This work demonstrates a Surface Acoustic Wave (SAW) filter using 2DEG as Interdigital Transducers (IDTs) formed on an AlGaN/GaN heterostructure.</li><li>Used fluoride-based (<math>CF_4</math>) plasma treatment to pattern 2DEG IDTs without removing the AlGaN barrier.</li><li>Demonstrated integration possibility with HEMTs on the same substrate for system-on-chip (SoC) wireless sensors.</li></ul>	<ul style="list-style-type: none"><li>Relevance of 2DEG in AlGaN/GaN heterostructures, which forms the conduction channel in GaN core and AlGaN shell regions.</li><li>Justifies inclusion of SRH, POLAR, and FLDMOB models in our model.</li></ul>

# Literature Survey

Paper & Publishing Details	Summary	Interface
<ul style="list-style-type: none"><li><b>Title:</b> Low Frequency Noise Analysis in AlGaN/GaN HEMTs</li><li><b>Authors:</b> Pradipta Kumar Jena, Sarita Misra, Sanghamitra Das, Biswajit Baral, Srikrishna Bardhan, and Sudhansu Kumar Pati</li><li><b>Conference:</b> 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS), IEEE, 2023</li><li><b>Affiliation:</b> Silicon Institute of Technology, Bhubaneswar, India</li></ul>	<ul style="list-style-type: none"><li>The paper analyzes low-frequency (<math>1/f</math>) noise in short-channel AlGaN/GaN HEMTs (<math>L_g = 0.2 \mu\text{m}</math>).</li><li>Found that higher Al content increases defect density, increasing trap-assisted scattering and current collapse.</li><li>Noise performance improves with lower Al content and higher temperature due to reduced trapping.</li></ul>	<ul style="list-style-type: none"><li>Useful for optimizing AlGaN shell thickness and material composition.</li><li>Suggests future improvements, incorporate temperature-dependent mobility (TEMP model) or interface trap density (<math>Q_f</math>).</li></ul>

# Literature Survey

Paper & Publishing Details	Summary	Interface
<ul style="list-style-type: none"><li><b>Title:</b> Analysis of AlGaN/GaN High Electron Mobility Transistor for High Frequency Application</li><li><b>Authors:</b> Subrangshu Chatterjee, Anumita Sengupta, Sudip Kundu, Aminul Islam</li><li><b>Conference:</b> IEEE Devices for Integrated Circuit (DevIC), March 2017, Kalyani, India</li><li><b>Affiliation:</b> Department of ECE, BIT Mesra, India</li></ul>	<ul style="list-style-type: none"><li>The study presents the DC and RF simulation of a planar AlGaN/GaN HEMT structure with a <math>\text{Si}_3\text{N}_4</math> surface passivation layer and a T-shaped Ni gate (5.2 eV) using Silvaco ATLAS.</li><li>Models used: SRH recombination, Albrecht low-field mobility, NEWTON solver for bias-dependent analysis.</li></ul>	<ul style="list-style-type: none"><li>The structural configuration (AlGaN barrier, GaN channel, <math>\text{Si}_3\text{N}_4</math> passivation) directly inspired the baseline planar device geometry</li><li>The extracted DC and RF parameters (<math>\text{Id}-\text{Vd}</math>, <math>\text{Id}-\text{Vg}</math>, <math>\text{gm}</math>, <math>f_t</math>) act as benchmark validation points for comparing the planar vs. nanowire HEMT performance</li></ul>

## PLANAR AlGaN/ GaN HEMT

# Reference Paper

**Objective:** Analyze AlGaN/GaN HEMT structure for high-frequency applications using SILVACO simulations.

**Substrate & Passivation:** Sapphire substrate;  $\text{Si}_3\text{N}_4$  passivation at gate region.

**Structure Parameters:**

PARAMETERS	VALUES
Gate Length	0.6 microns
Channel Length	2.2 microns
Source Length	0.3 microns
Drain Length	0.3 microns
Gate Work Function	4.4 microns
GaN doping concentration	$6 \times 10^{12} \text{ cm}^{-3}$
GaN doping concentration	$6 \times 10^{12} \text{ cm}^{-3}$

**Analysis of AlGaN/GaN for High Frequency Application using HEMT Transistor**

1Pramod Martha, 2Ranjita Rout, 3Rashmi Tiwary, 4Ankita Vishwakarma

# Reference Paper

- **Simulation Details:**

SRH recombination model used

Observed ID–VD and transfer characteristics

- **Key Results:**

*Threshold voltage ( $V_t$ ): -6 V*

*Peak current:  $\approx 0.44$  A at  $V_{GS} = 0$  V,  $V_{DS} = 8$  V*

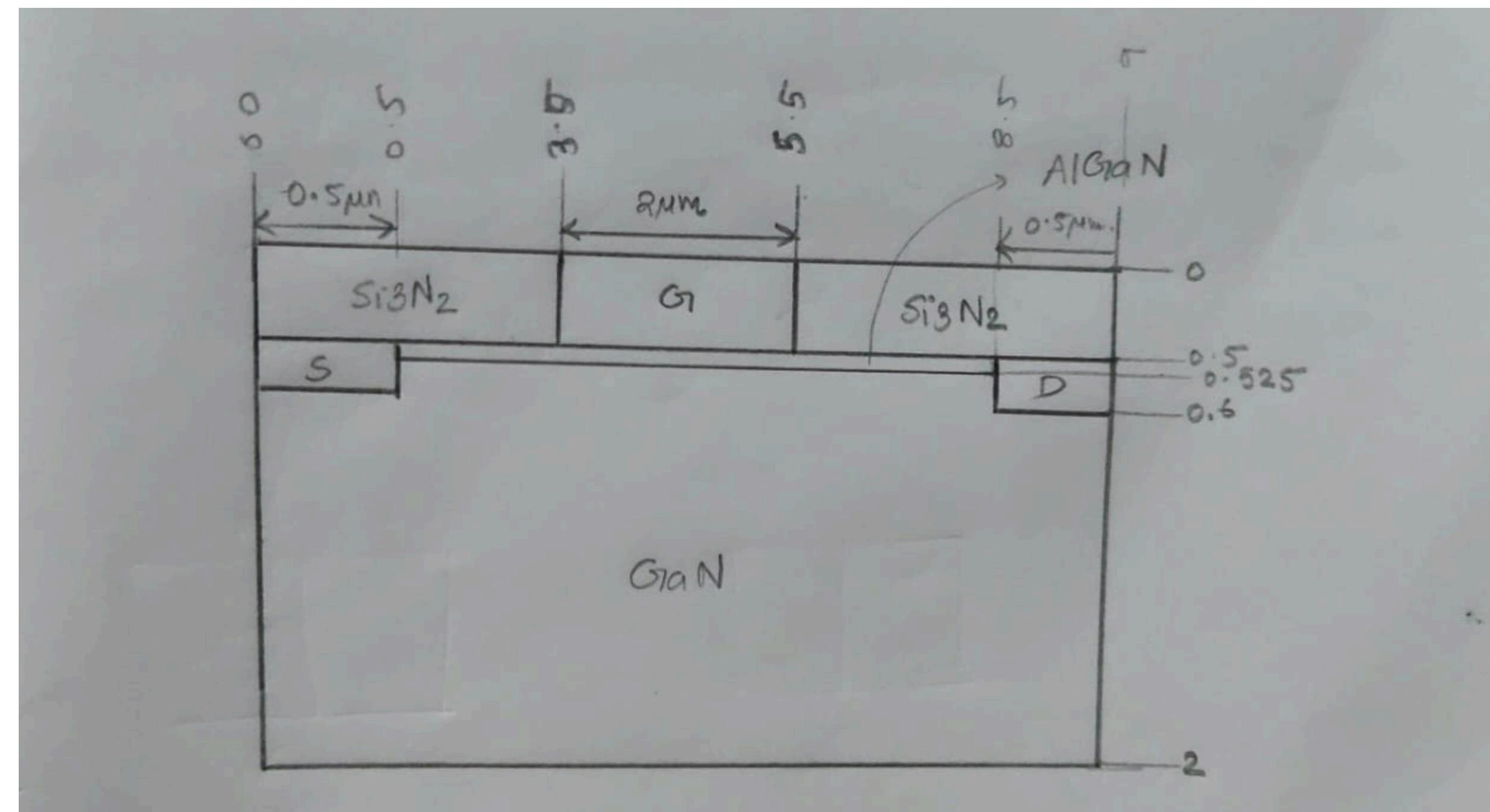
*Device saturates at  $V_{DS} \approx 7$  V*

*Subthreshold slope: low  $\rightarrow$  high switching speed*

- **Conclusion:**

AlGaN/GaN HEMT shows excellent high-frequency performance and suitability for power/microwave applications.

# Schematic of Structure



# Schematic of Structure

Parameters	Values
Gate Length	2um
Source Length	0.5um
Drain Length	0.5um
Gate Work Function	5eV

# CODE

## **Mesh Definition:**

3D grid created using mesh three ( $x$  = length,  $y$  = vertical,  $z$  = width).  
Fine mesh near junctions ( $0.001\text{ }\mu\text{m}$ ) for accuracy.

## **Device Regions:**

AlGaN barrier ( $x$  =  $0\text{--}9\text{ }\mu\text{m}$ ,  $y$  =  $0.5\text{--}0.525\text{ }\mu\text{m}$ )  
 $\text{Si}_3\text{N}_4$  insulator (gate dielectric)  
GaN substrate (main conduction layer)

## **Electrodes:**

Source ( $x$  =  $0\text{--}0.5\text{ }\mu\text{m}$ ), Drain ( $x$  =  $8.5\text{--}9\text{ }\mu\text{m}$ ), Gate ( $x$  =  $3.5\text{--}5.5\text{ }\mu\text{m}$ ), and substrate contact.

## **Contact Work Functions:**

Gate = 5 eV; Source/Drain = 3.93 eV.

## **Models Used:**

SRH recombination, Albrecht mobility, polarization (strain-induced).  
Enables realistic carrier transport and polarization effects in GaN.

# CODE

## **Bias Sweep:**

Simulates  $I_d$ - $V_g$  and  $I_d$ - $V_d$  curves.

$v_{drain}$  swept  $0 \rightarrow 15$  V;  $v_{gate}$  swept  $-10 \rightarrow +1$  V.

## **Extraction Section:**

Calculates  $V_{th\_lowVd}$ ,  $V_{th\_highVd}$ , and  $DIBL = \Delta V_{th} / \Delta V_d$ .

Enables evaluation of short-channel behavior and threshold shift.

## **Visualization:**

`tonyplot` and `tonyplot3d` used to view current, potential, and band diagrams

# CODE

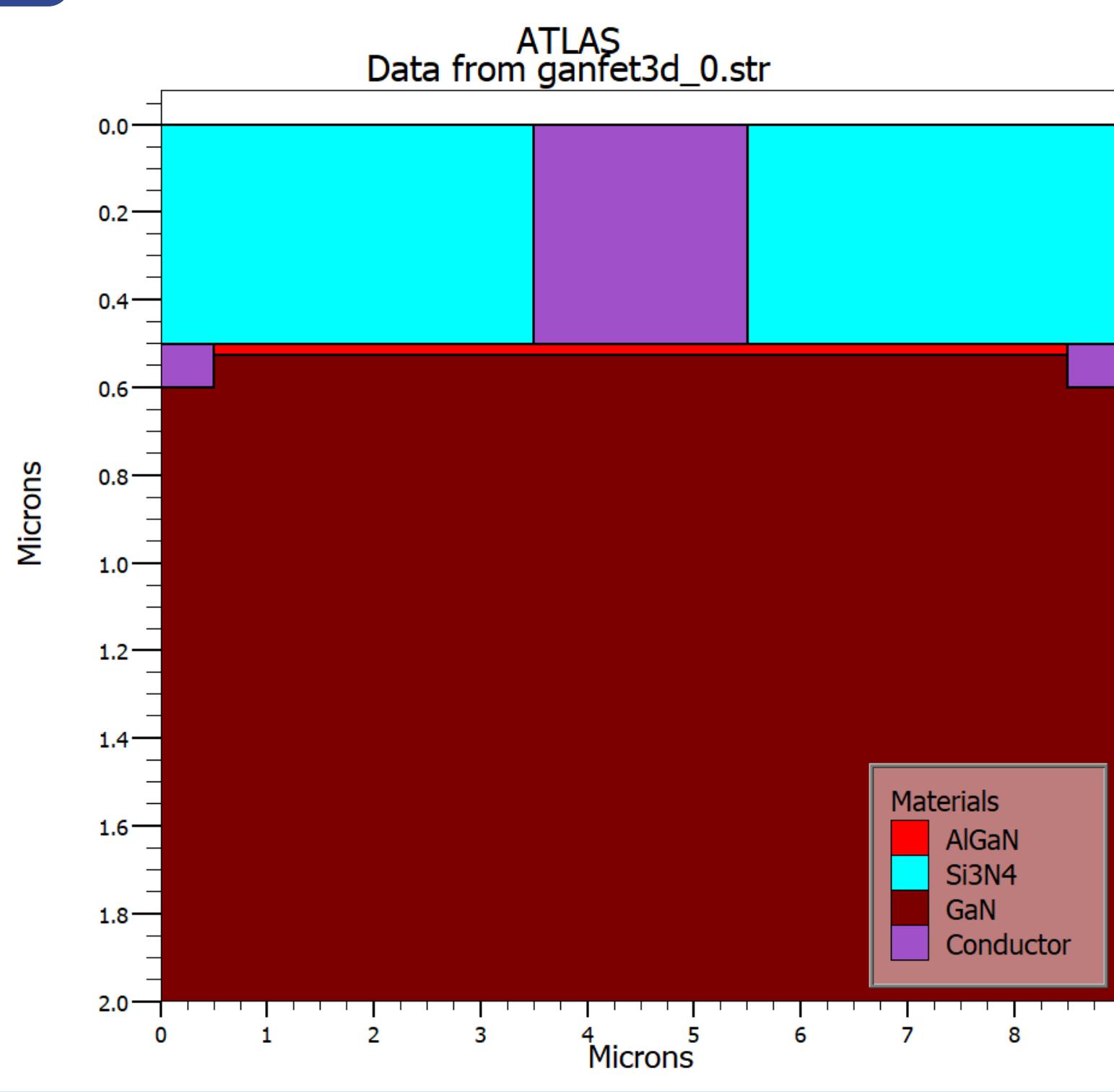
## Models Used

Model	Purpose / Function
FLDMOB	Includes <b>field-dependent mobility</b> – reduces carrier mobility at high electric fields.
SRH	<b>Shockley-Read-Hall recombination</b> – models carrier loss through trap states in the bandgap.
AUGER	<b>Auger recombination</b> – accounts for carrier recombination at very high carrier densities.
FERMI	Uses <b>Fermi-Dirac statistics</b> instead of Maxwell-Boltzmann for accurate carrier distribution at high doping.
BGN	<b>Bandgap narrowing</b> – models bandgap reduction in heavily doped regions.

# CODE

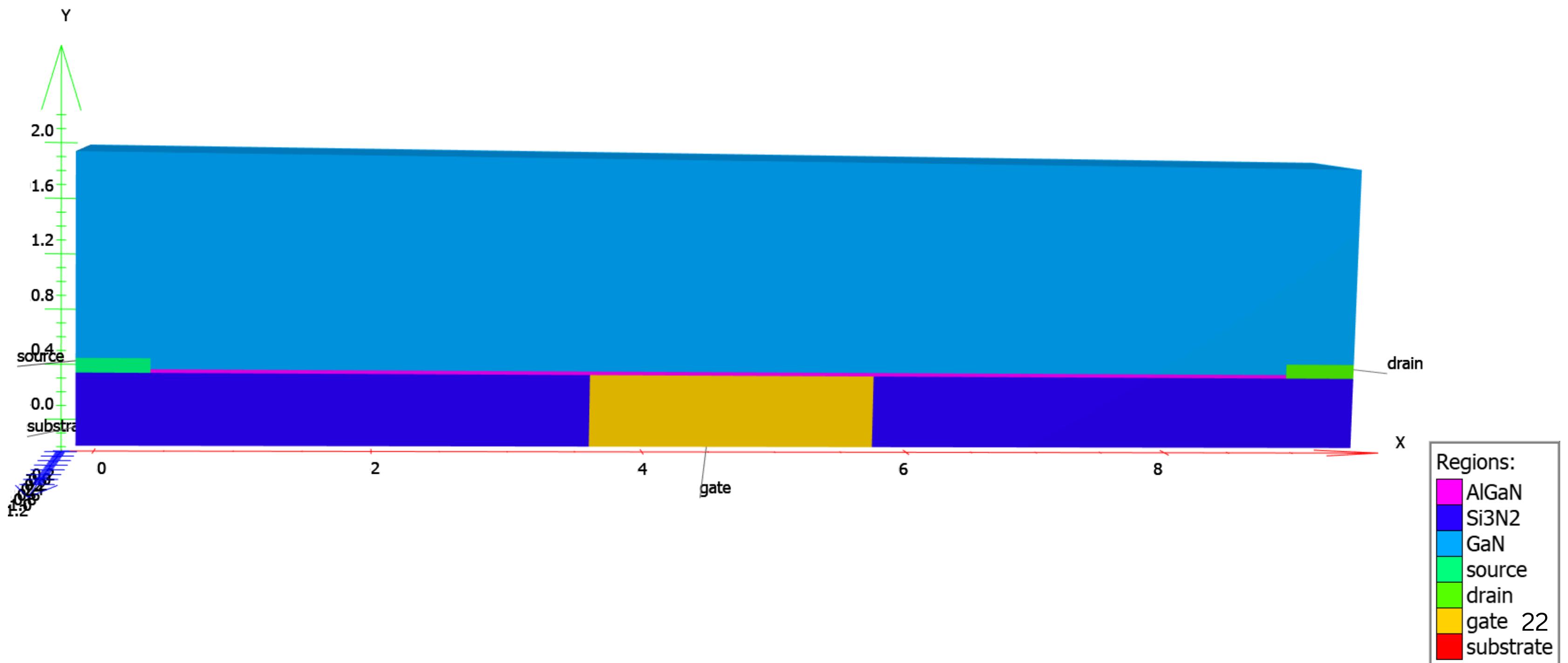
POLAR	Enables <b>polarization charge effects</b> (spontaneous + piezoelectric) in III-nitride materials.
bipolar	Activates <b>both electron and hole transport equations</b> (important for complete current balance).
TEMP=300	Sets the <b>simulation temperature to 300 K</b> (room temperature).
mobility albrct.n	Uses <b>Albrecht low-field mobility model</b> for electrons – realistic drift behavior in GaN.

# 2D Structure of GaNFET

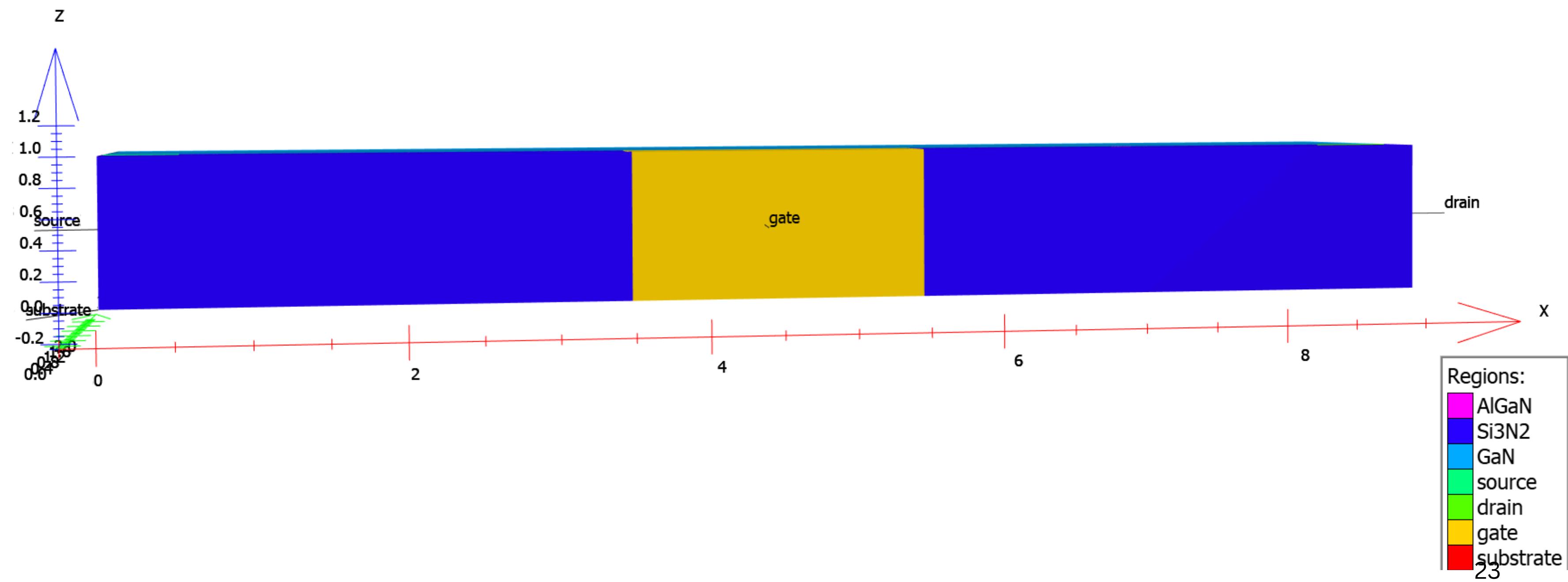


# 3D Structure of GaNFET

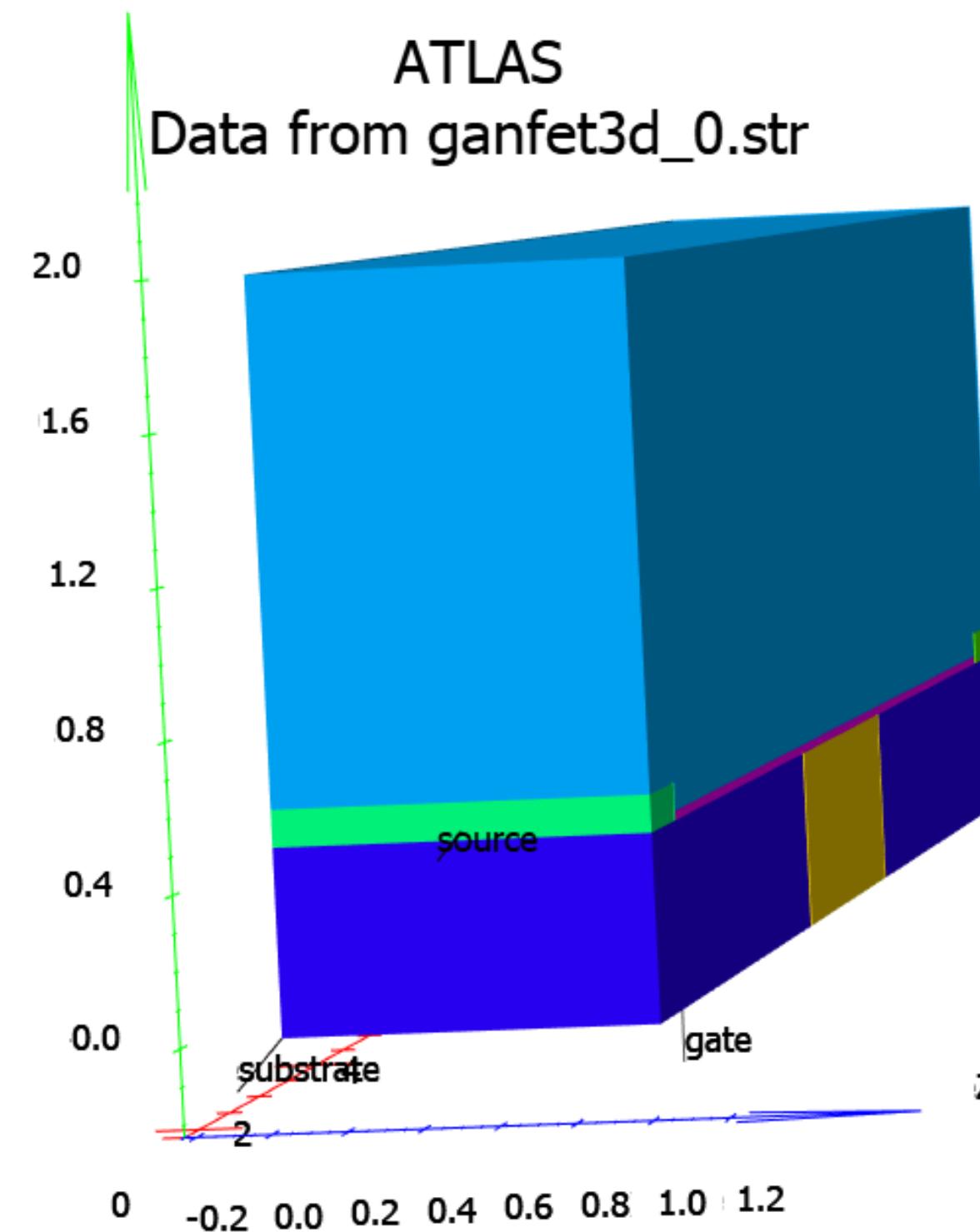
ATLAS  
Data from ganfet3d\_0.str



# 3D Structure of GaNFET

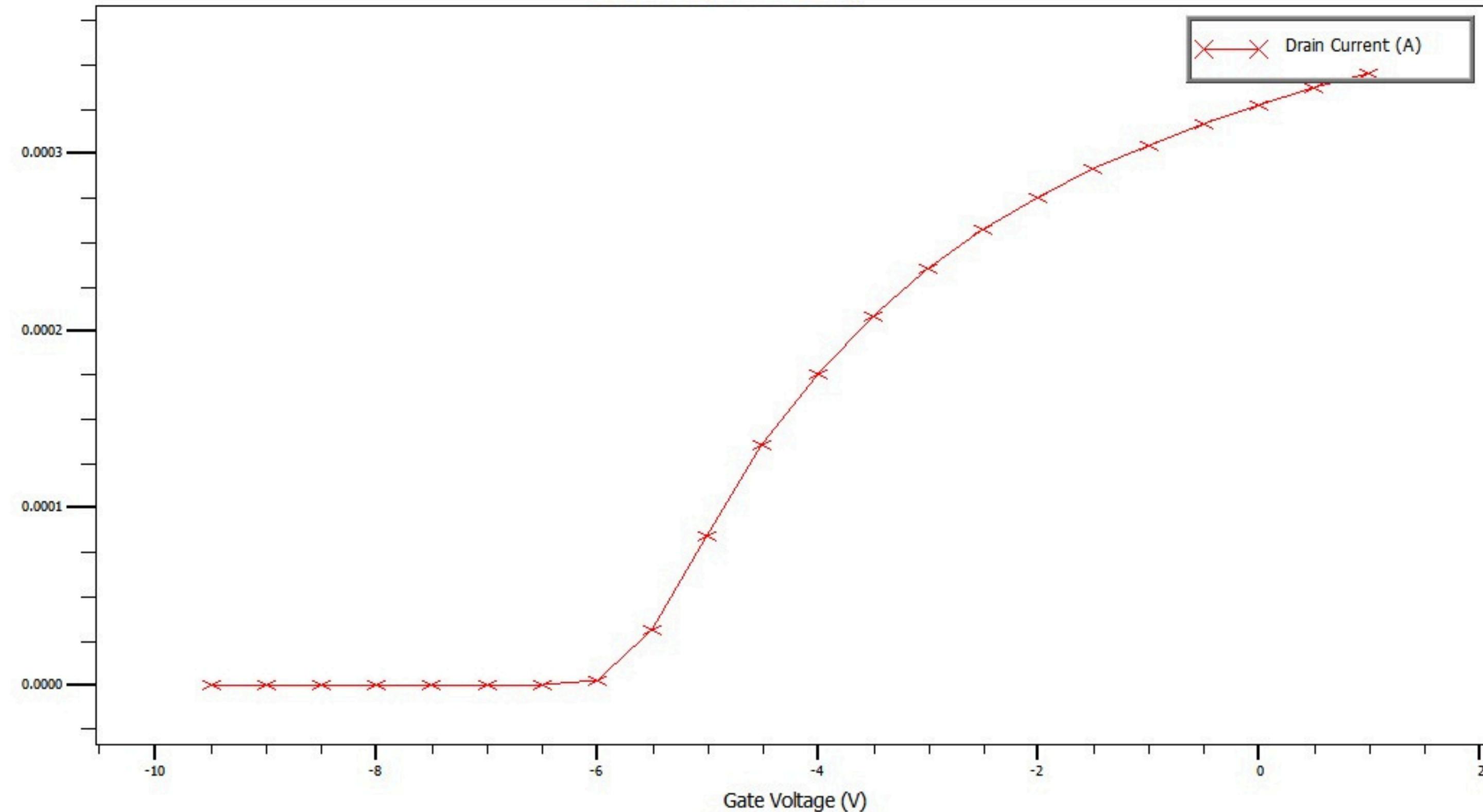


# 3D Structure of GaNFET

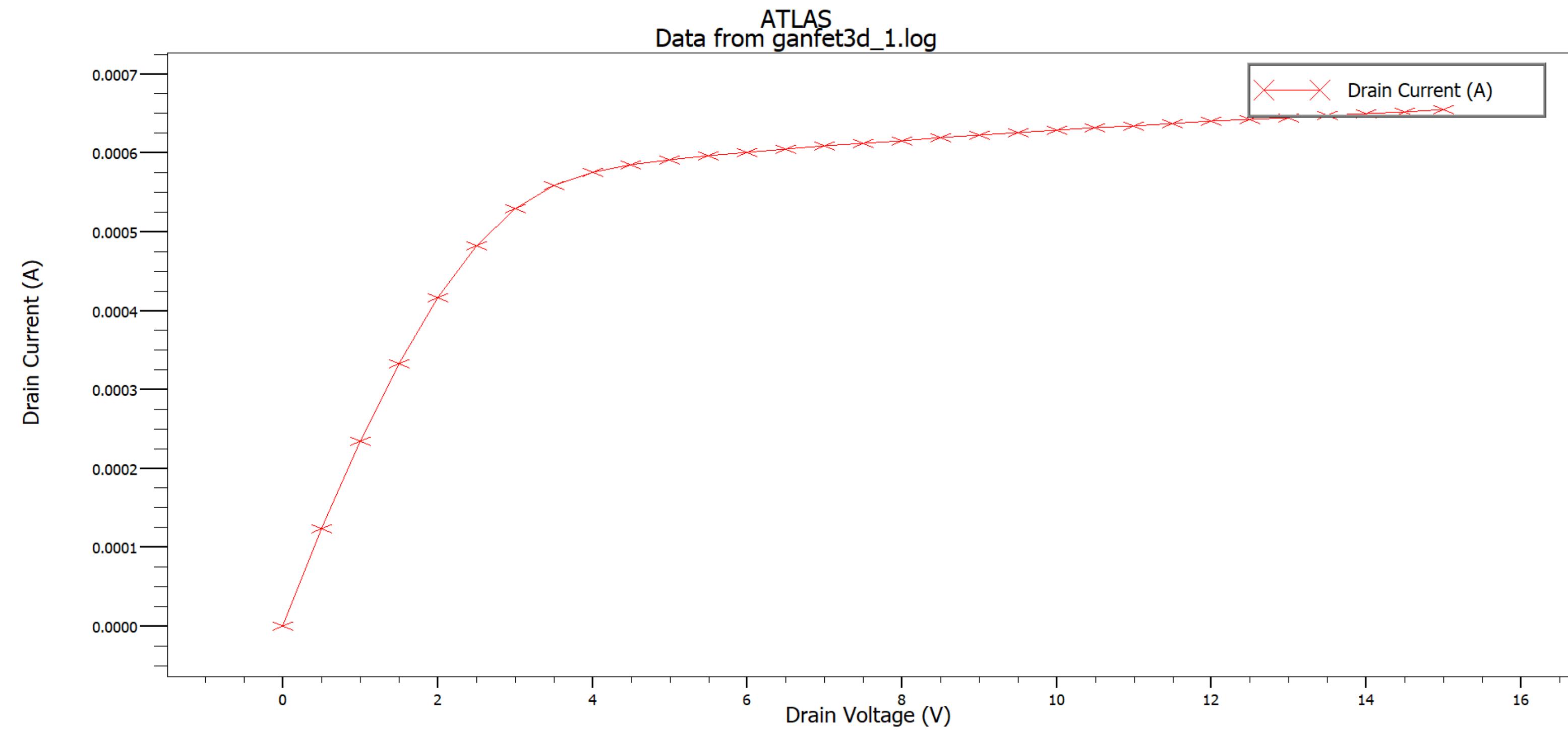


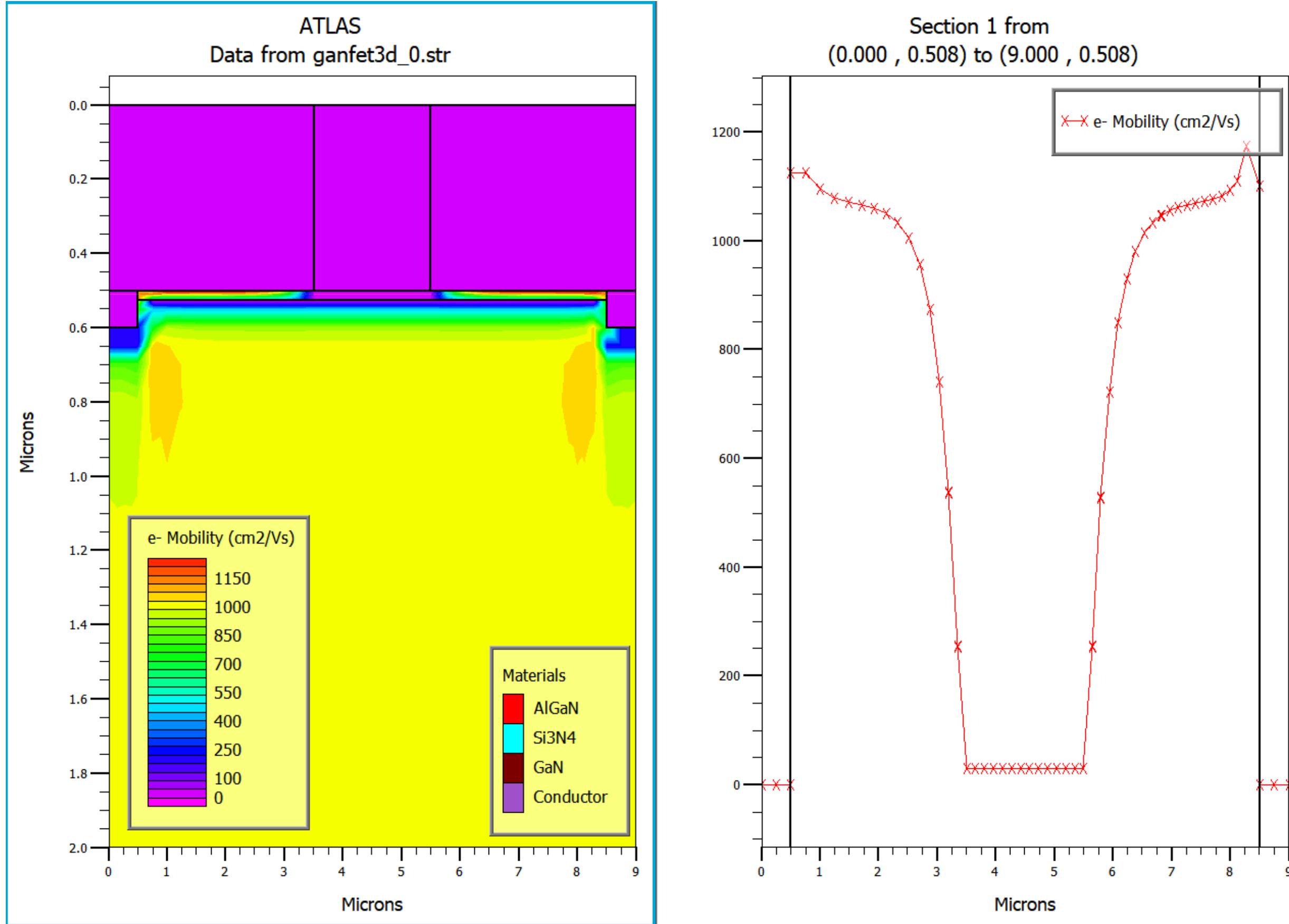
# Transfer Chara

ATLAS  
Data from ganfet3d\_0.log



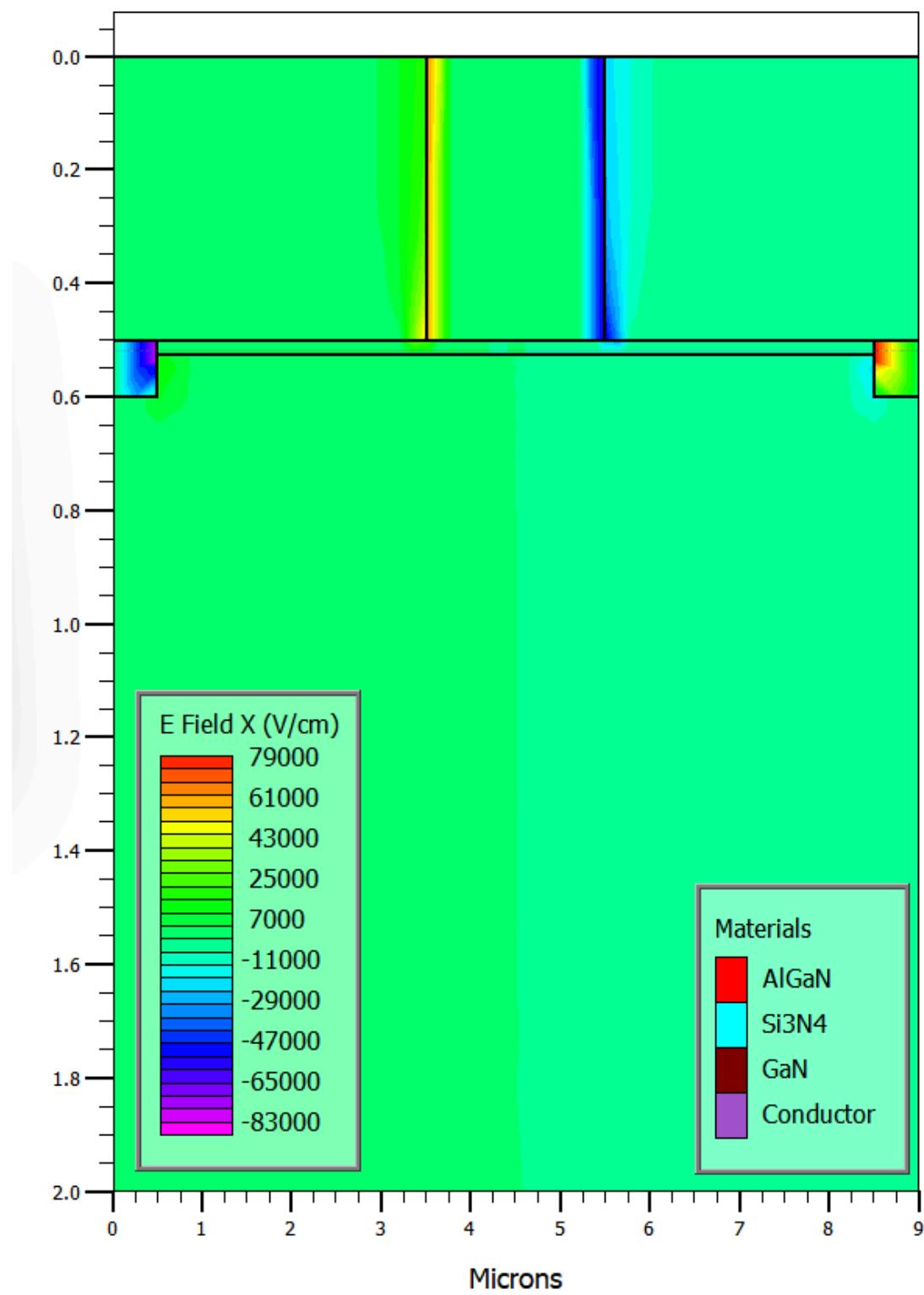
# Output Chara



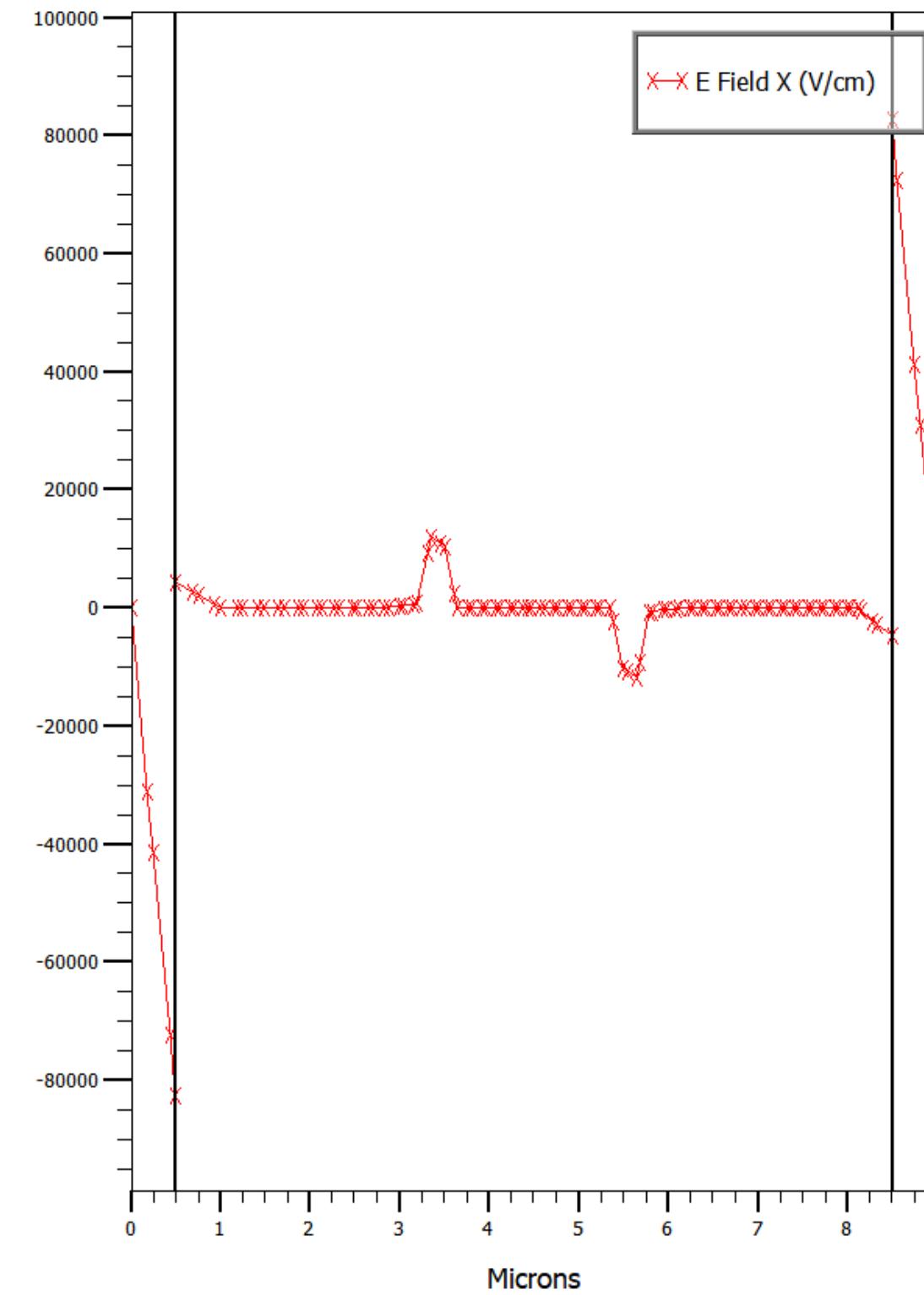


## e- Mobility

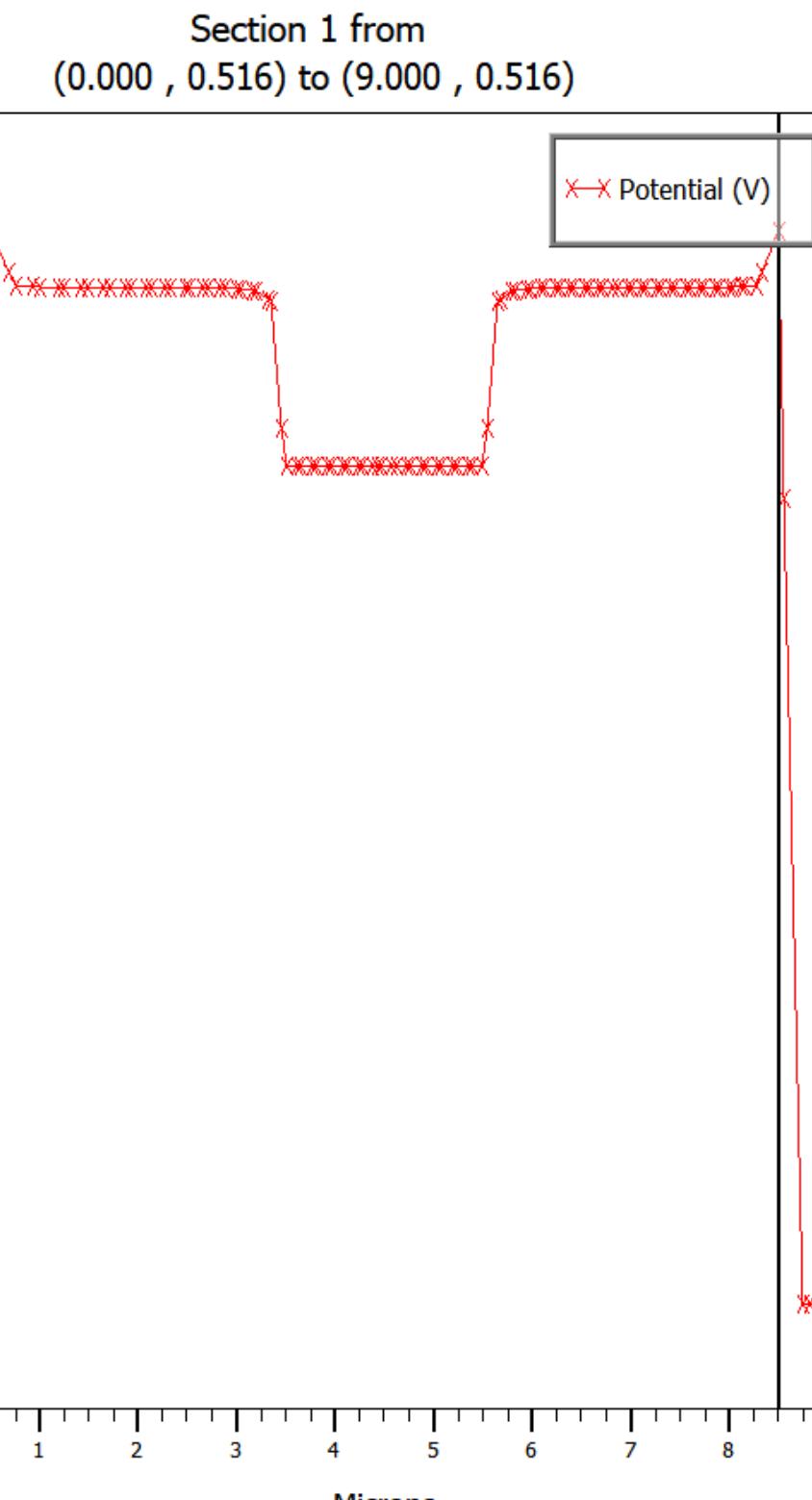
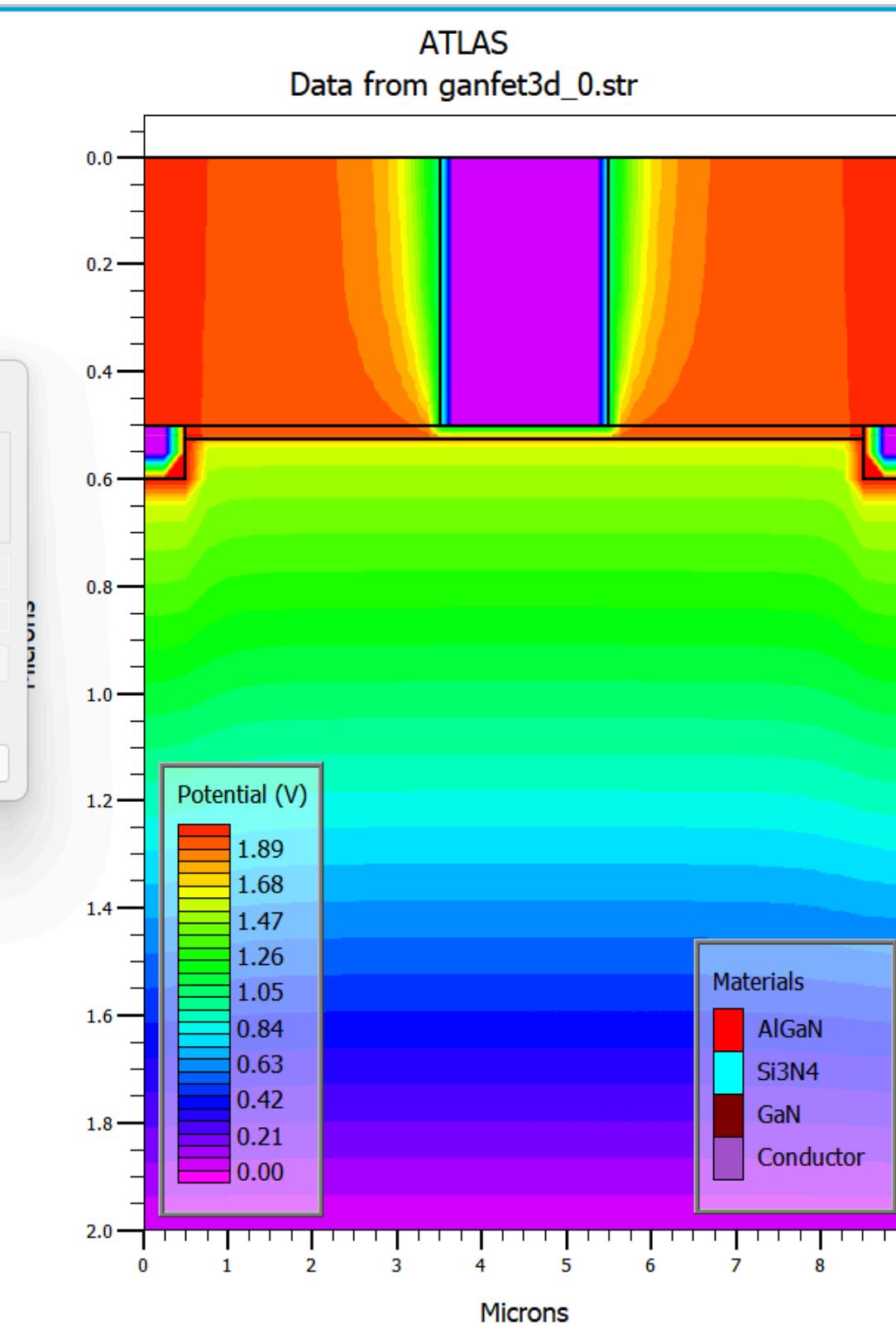
ATLAS  
Data from ganfet3d\_0.str



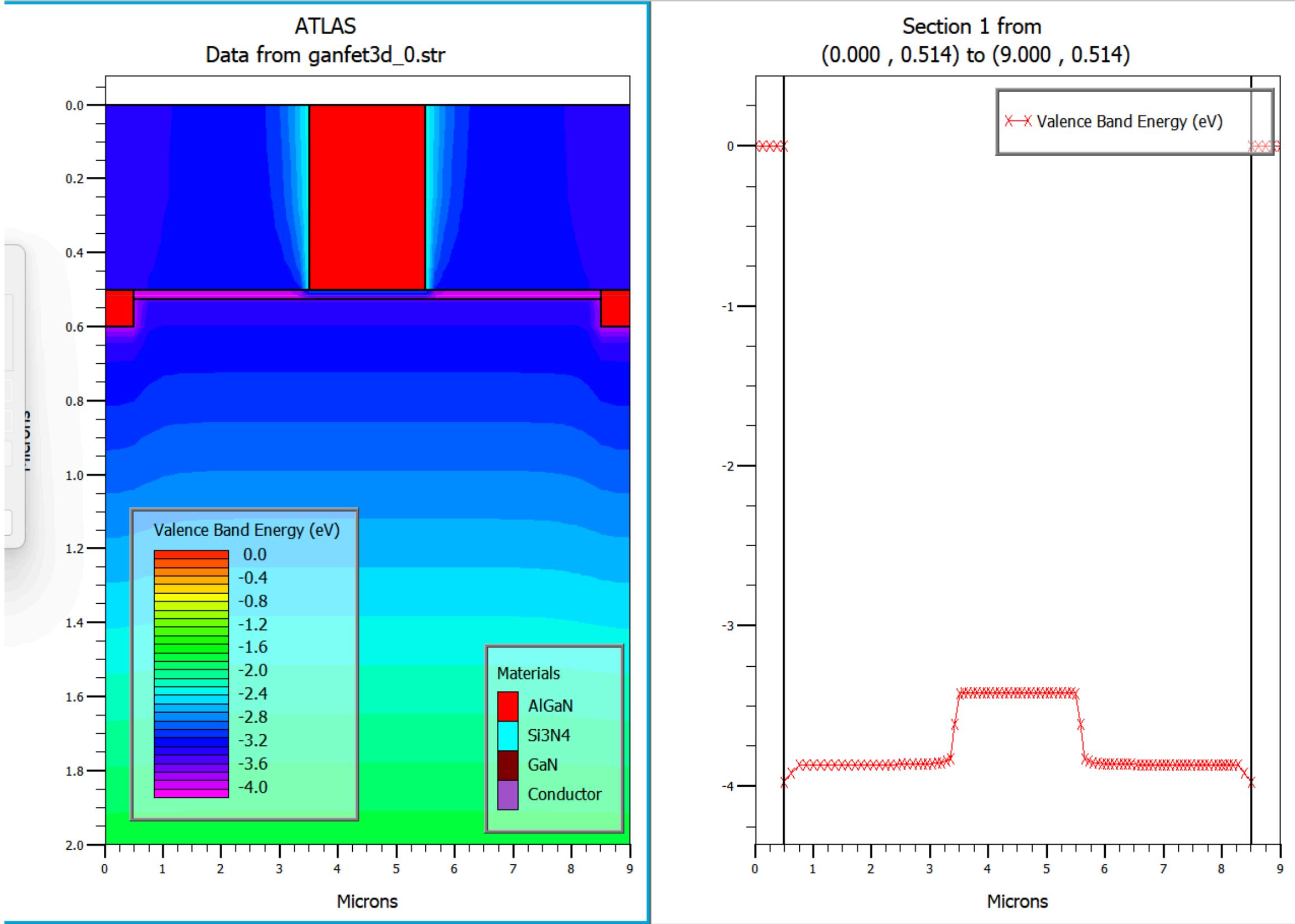
Section 1 from  
(0.000 , 0.516) to (9.000 , 0.516)



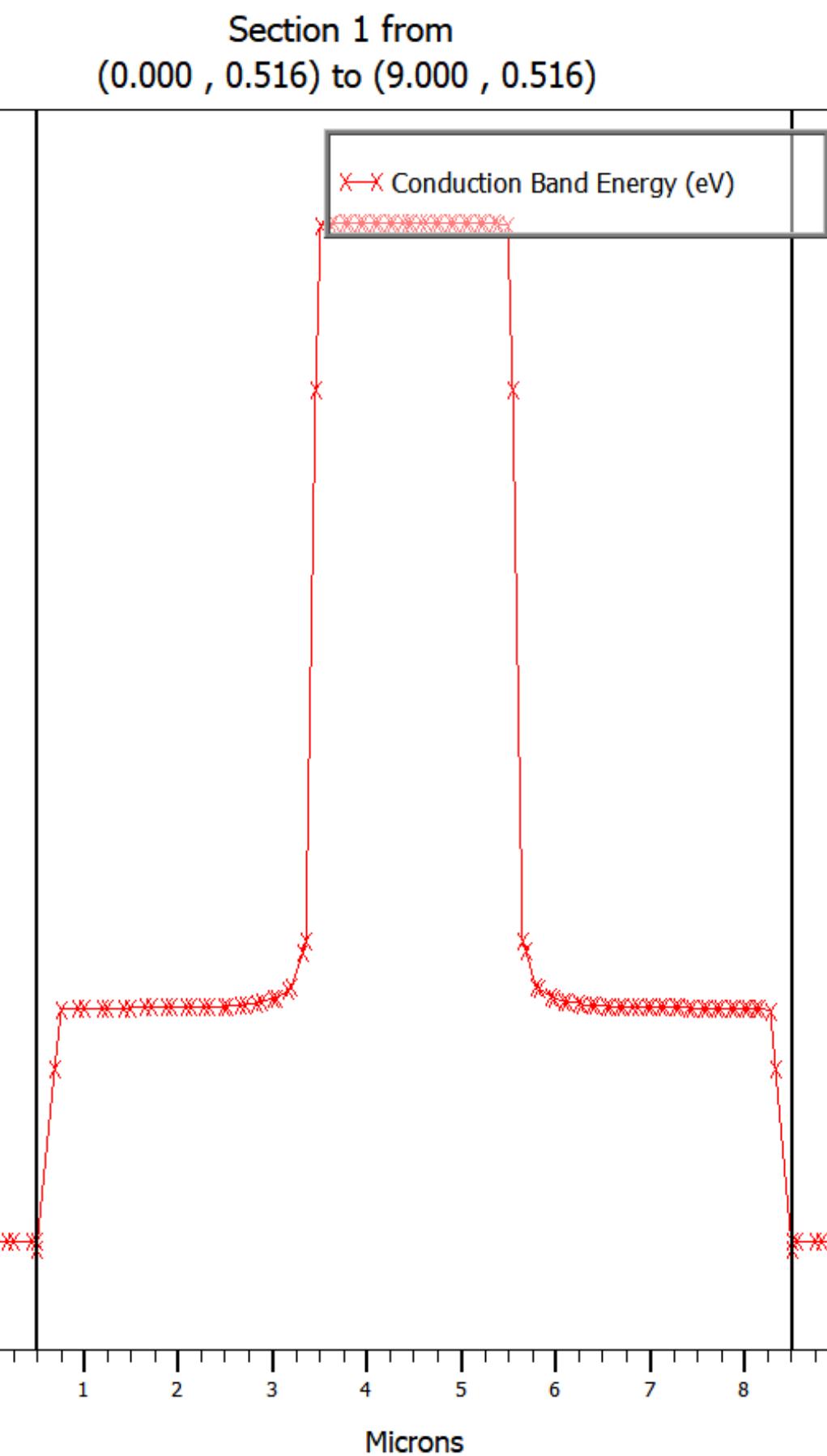
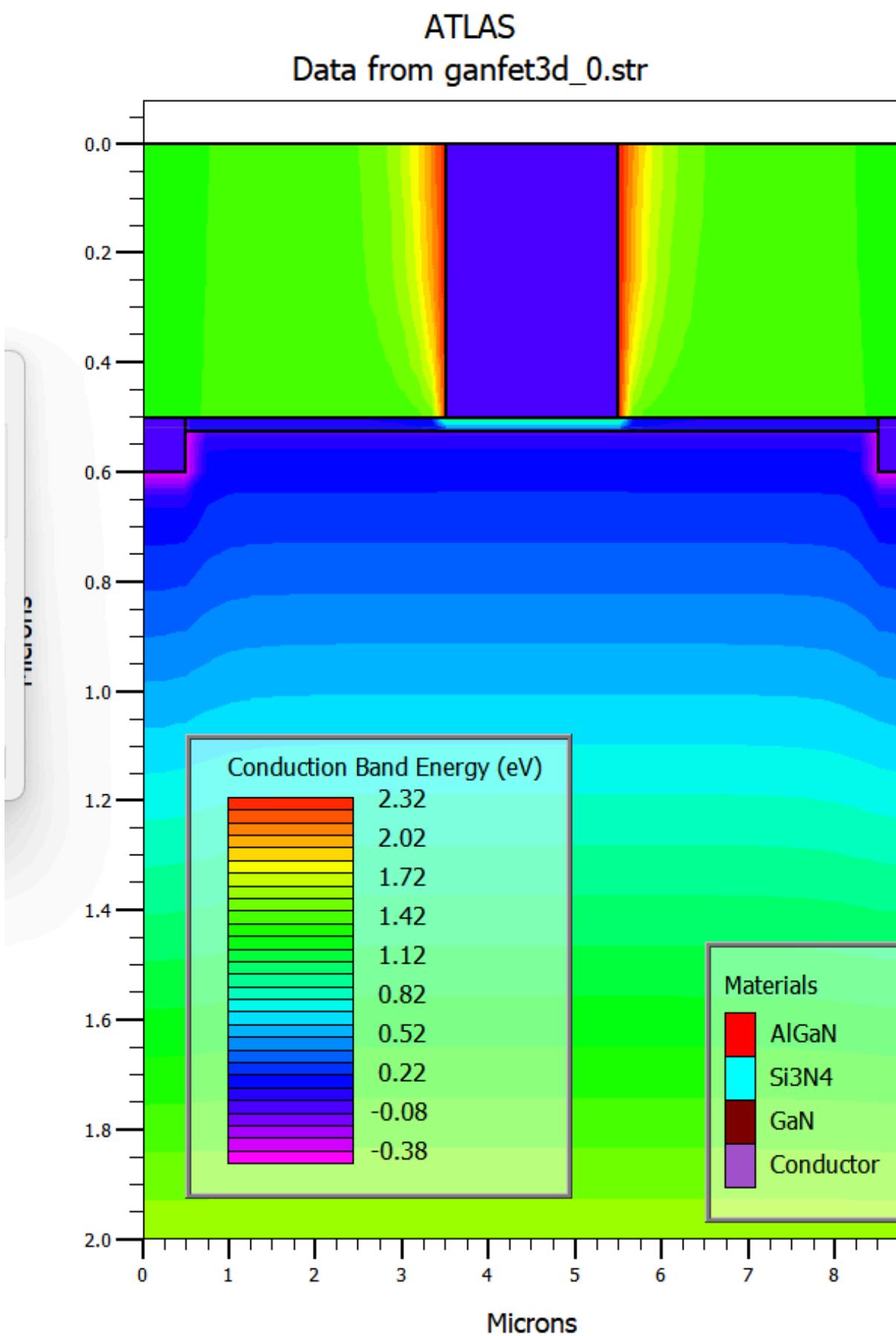
Electric Field



# Potential



## Valence Band Energy



## Conduction Band Energy

```
Vth_lowVd=-6.11133
EXTRACT>
EXTRACT> # --- Load high drain voltage data ---
EXTRACT> quit
EXTRACT> init infile="ganfet3d_1.log"
EXTRACT> extract name="Vth_highVd" x.val from curve(v."gate", log10(abs(i."drain")))) where y.val=-7
Vth_highVd=-3
EXTRACT>
EXTRACT> # --- Define constants ---
EXTRACT> extract name="Vd_low" 1.0
Vd_low=1
EXTRACT> extract name="Vd_high" 15.0
Vd_high=15
EXTRACT>
EXTRACT> # --- Compute intermediate values ---
EXTRACT> extract name= "deltaVth" (-6.11133 - -3)
deltaVth=-3.11133
EXTRACT> extract name="deltaVd" (15 - 1)
deltaVd=14
EXTRACT>
EXTRACT> # --- Finally compute DIBL ---
EXTRACT> extract name="DIBL" (-3.11133 / 14)
DIBL=-0.222238
EXTRACT>
```

Parameter	Value (approx.)	Meaning / Observation
<b>Vth_lowVd</b>	-6.11 V	Threshold voltage at low drain bias (1 V) – device starts to conduct.
<b>Vth_highVd</b>	-3.00 V	Threshold at high drain bias (15 V) – barrier reduced due to DIBL.
<b>ΔVth</b>	3.11 V	Voltage shift between low and high drain biases.
<b>DIBL</b>	0.222 V/V	Drain-induced barrier lowering – moderate short-channel effect.
<b>gm_max</b>	~ $1.0 \times 10^{-5}$ A/V (estimated from slope of Id–Vg near -5 V → -3 V)	Peak transconductance; represents how effectively gate voltage controls drain current.



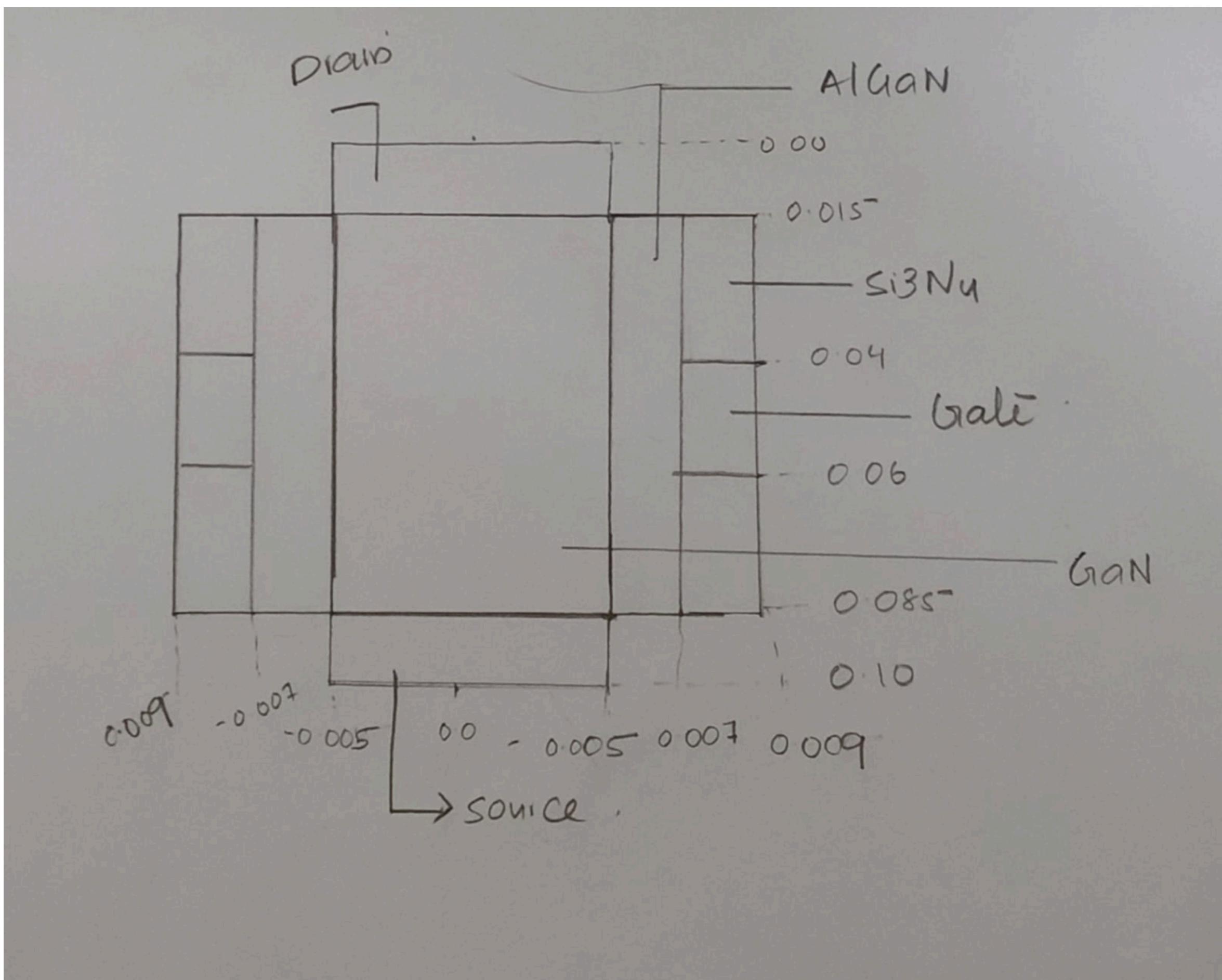
# GAA Nanowire AlGaN/ GaN HEMT

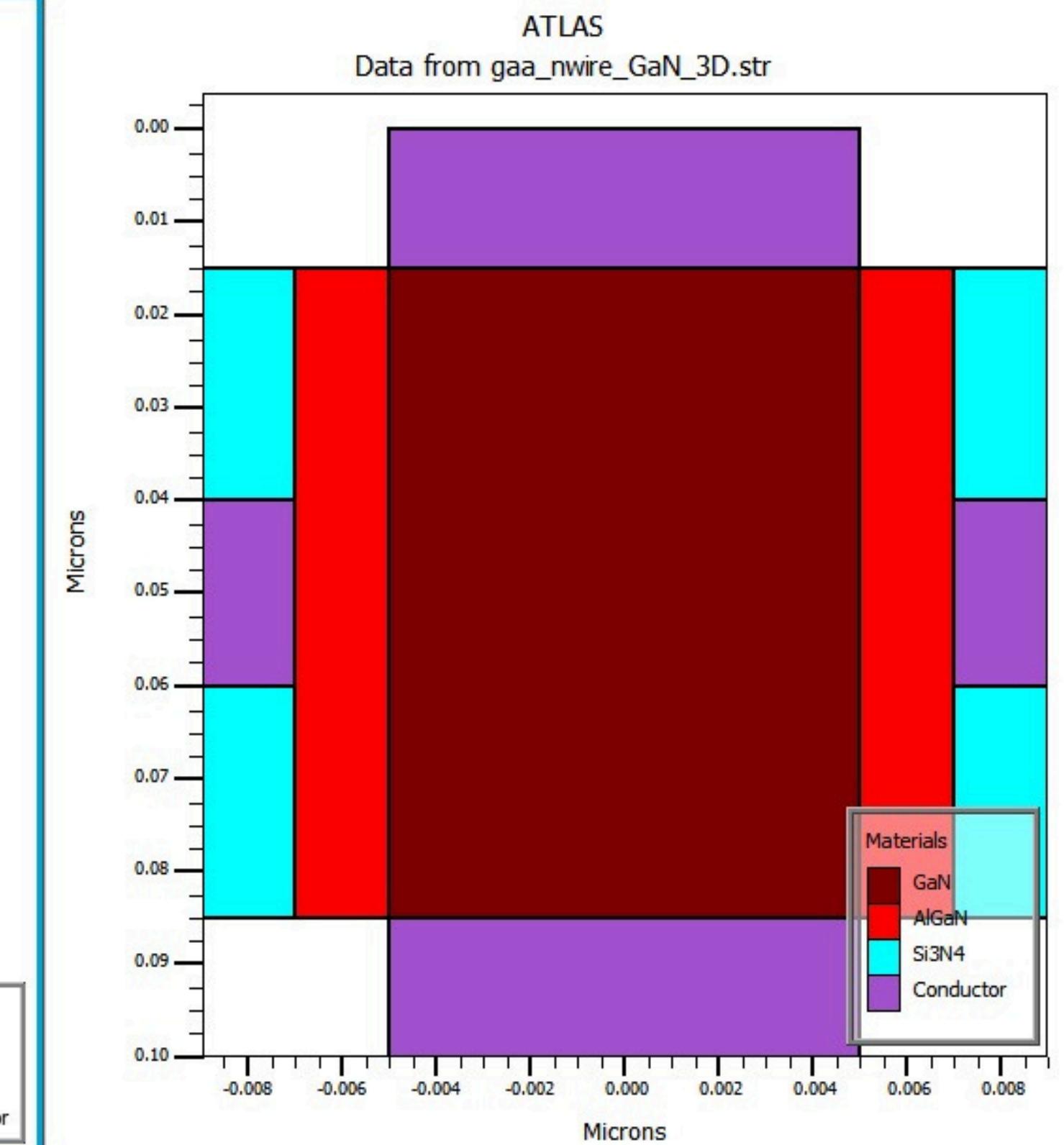
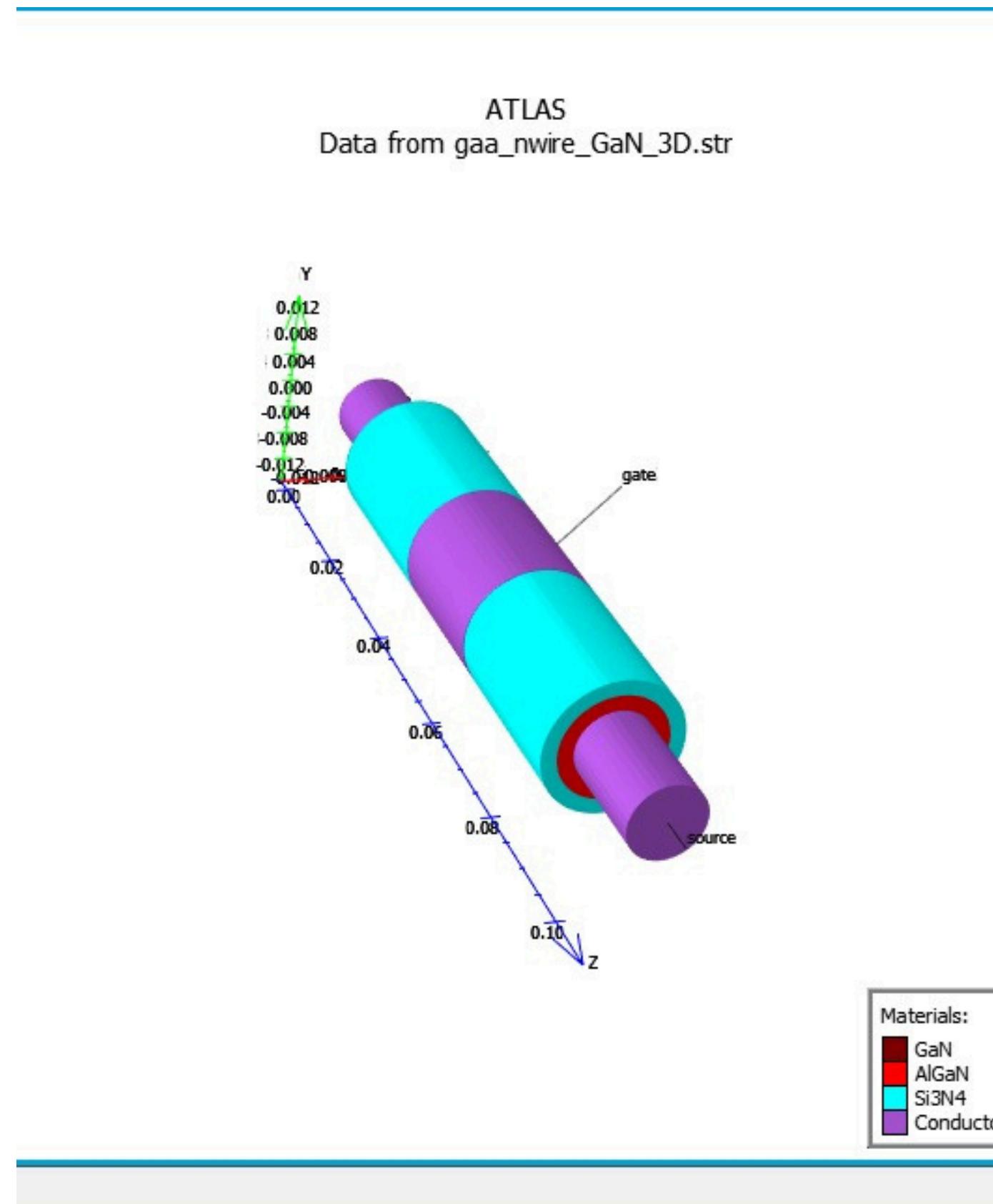
# GaN/ HEMT Nano wire

- **Superior Electrostatic Control:** GAA geometry wraps the gate entirely around the channel, providing 360° control. This drastically improves gate control over the channel charge, reducing short-channel effects and leakage currents.
- **Better Scalability:** GAA transistors can be scaled down further than planar devices because their gate fully encloses the channel, maintaining excellent control even at very small dimensions, essential for future nanoscale electronics.
- **Higher ON/OFF Current Ratio:** The enhanced gate control in GAA devices results in sharper switching characteristics and a higher ratio of ON-state current to OFF-state leakage, improving power efficiency

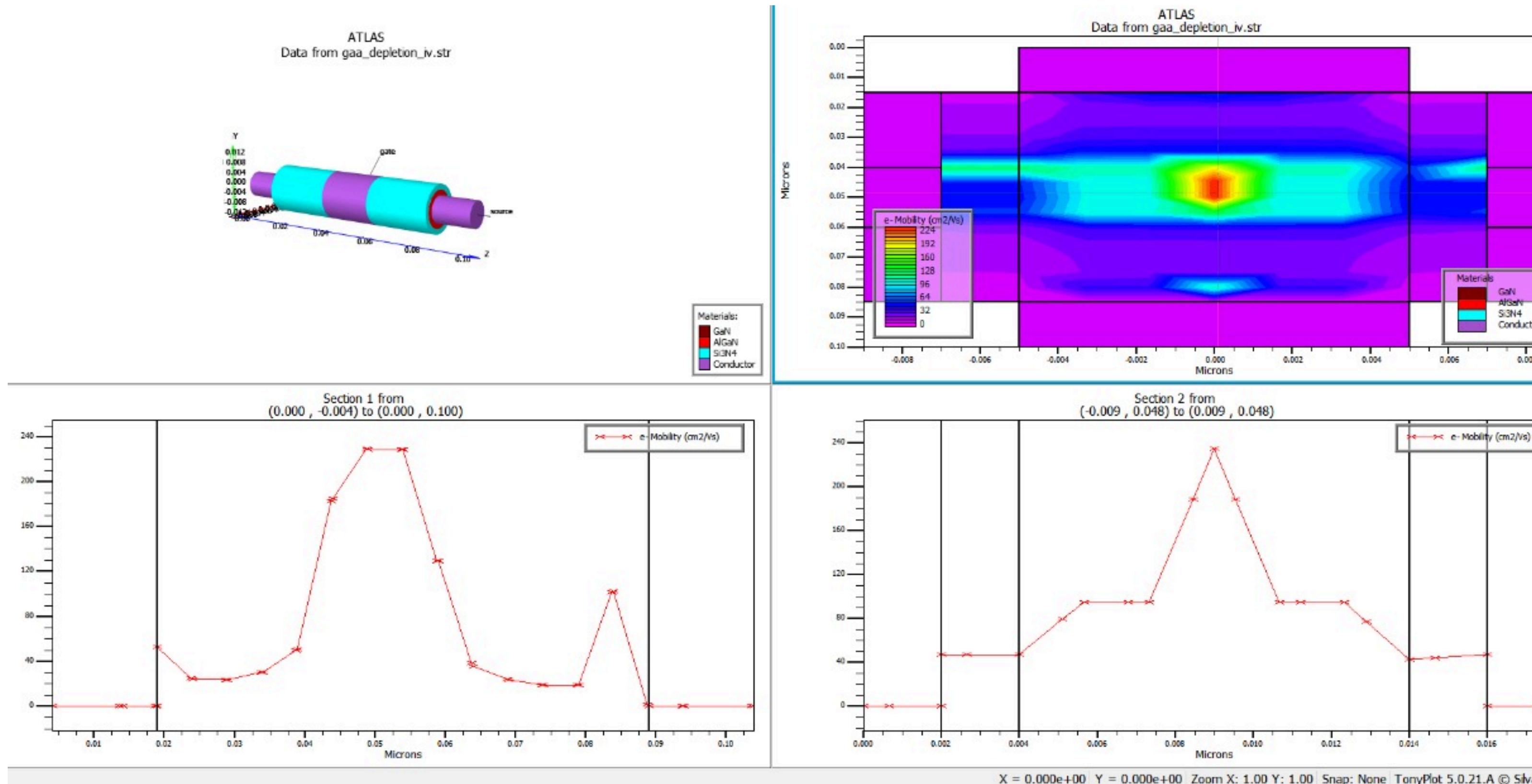
# Dimensions

- GaN Core (Channel) Radius: 0 to 0.005  $\mu\text{m}$  (5 nm)
- GaN Core Length (along z-axis): 0 to 0.10  $\mu\text{m}$  (100 nm)
- AlGaN Shell Thickness: From radius 0.005  $\mu\text{m}$  to 0.007  $\mu\text{m}$  (2 nm thickness)
- AlGaN Shell Length (along z-axis): 0.015 to 0.085  $\mu\text{m}$  (70 nm)
- Si<sub>3</sub>N<sub>4</sub> Shell Thickness: From radius 0.007  $\mu\text{m}$  to 0.009  $\mu\text{m}$  (2 nm thickness)
- Si<sub>3</sub>N<sub>4</sub> Shell Length (along z-axis): 0.015 to 0.085  $\mu\text{m}$  (70 nm)
- Air Region Radius: From radius 0.009  $\mu\text{m}$  to 0.012  $\mu\text{m}$  (3 nm gap)
- Electrode Lengths (z-axis):
  - Drain: 0.00 to 0.015  $\mu\text{m}$  (15 nm)
  - Source: 0.085 to 0.10  $\mu\text{m}$  (15 nm)
  - Gate: 0.040 to 0.060  $\mu\text{m}$  (20 nm)
- Electrode Radial Positions (r-axis):
  - Source & Drain overlap GaN core (0 to 0.005  $\mu\text{m}$  radius)
  - Gate wraps around Si<sub>3</sub>N<sub>4</sub> shell (0.007 to 0.009  $\mu\text{m}$  radius)

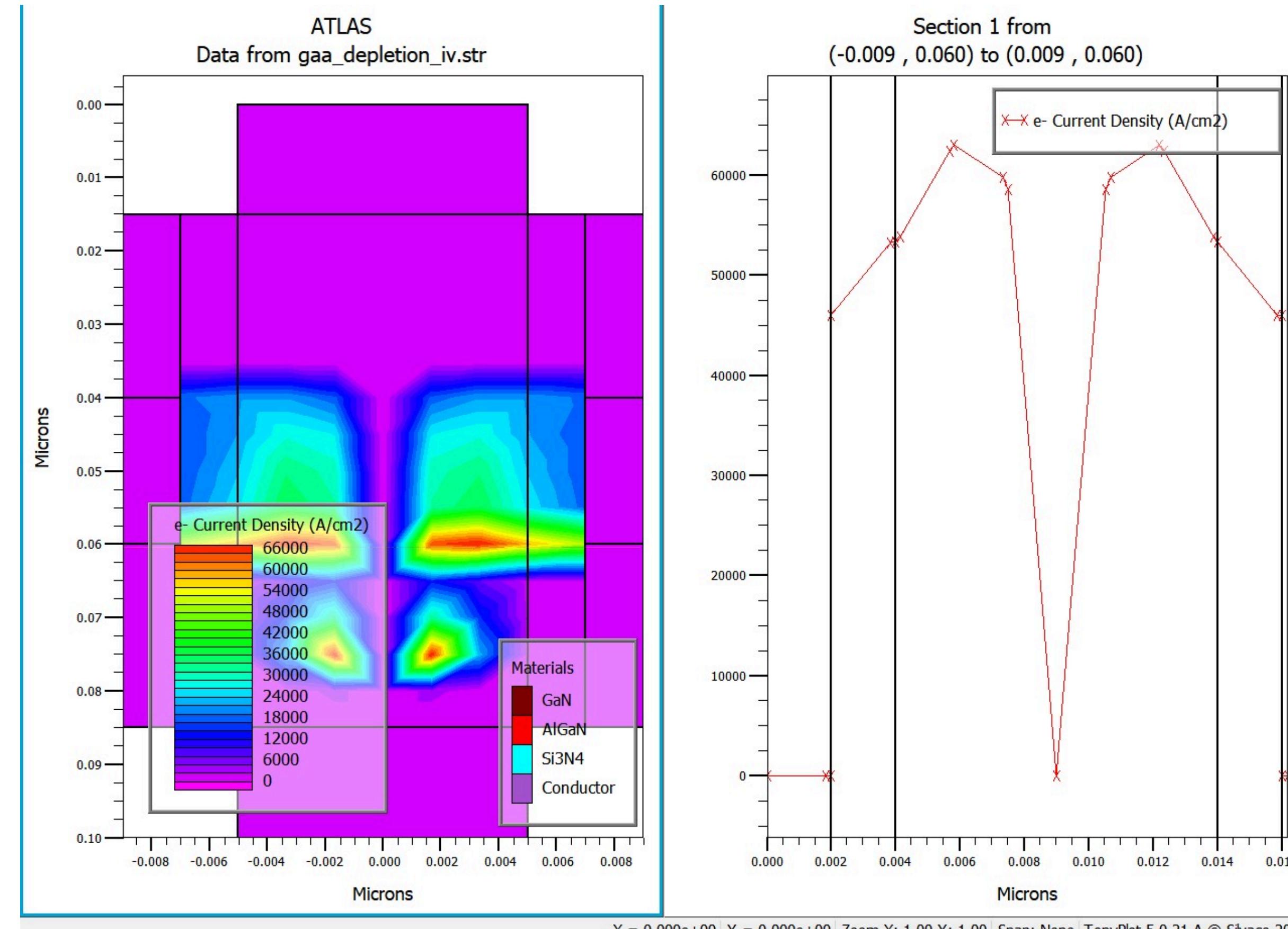




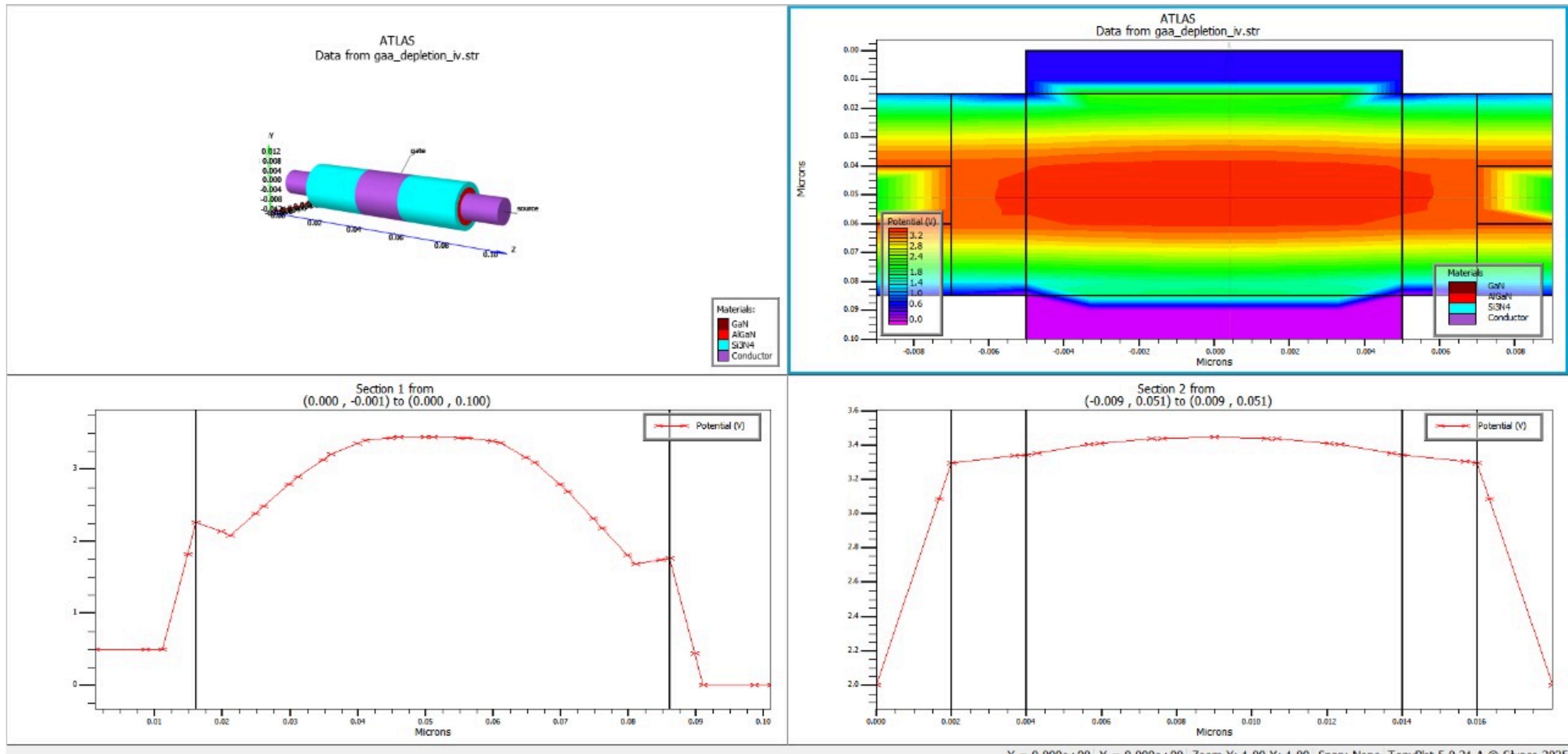
# MOBILITY



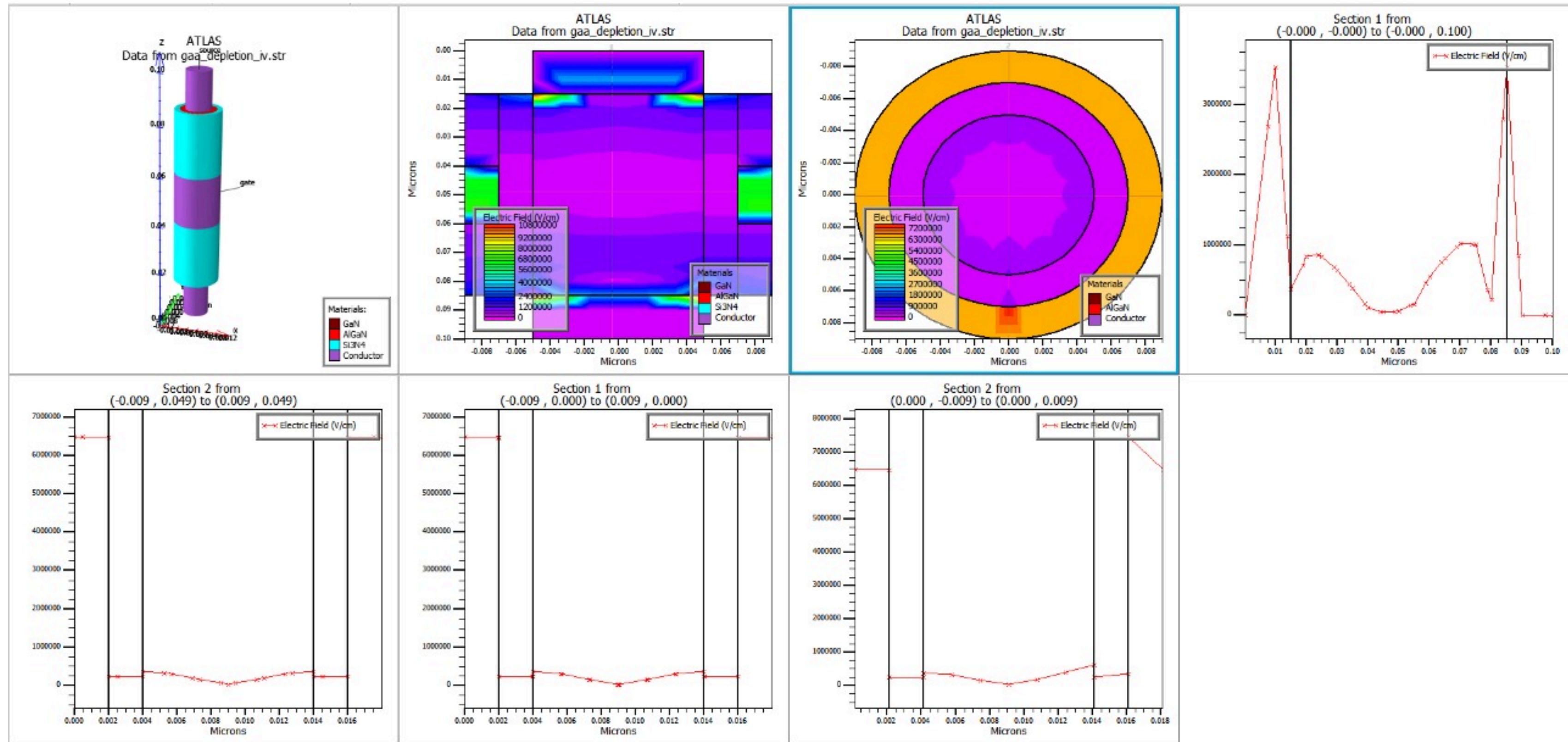
# CURRENT DENSITY



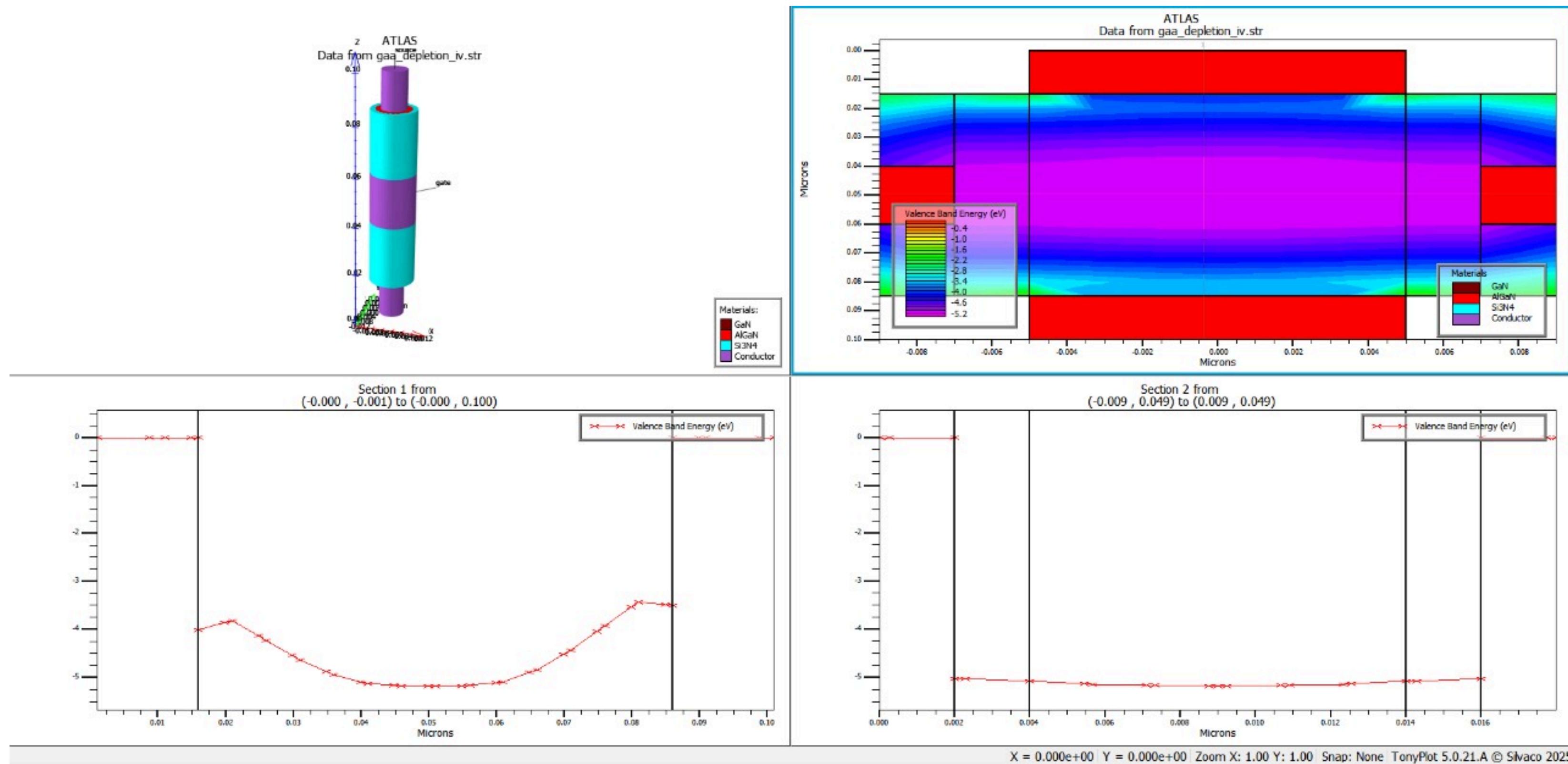
# POTENTIAL



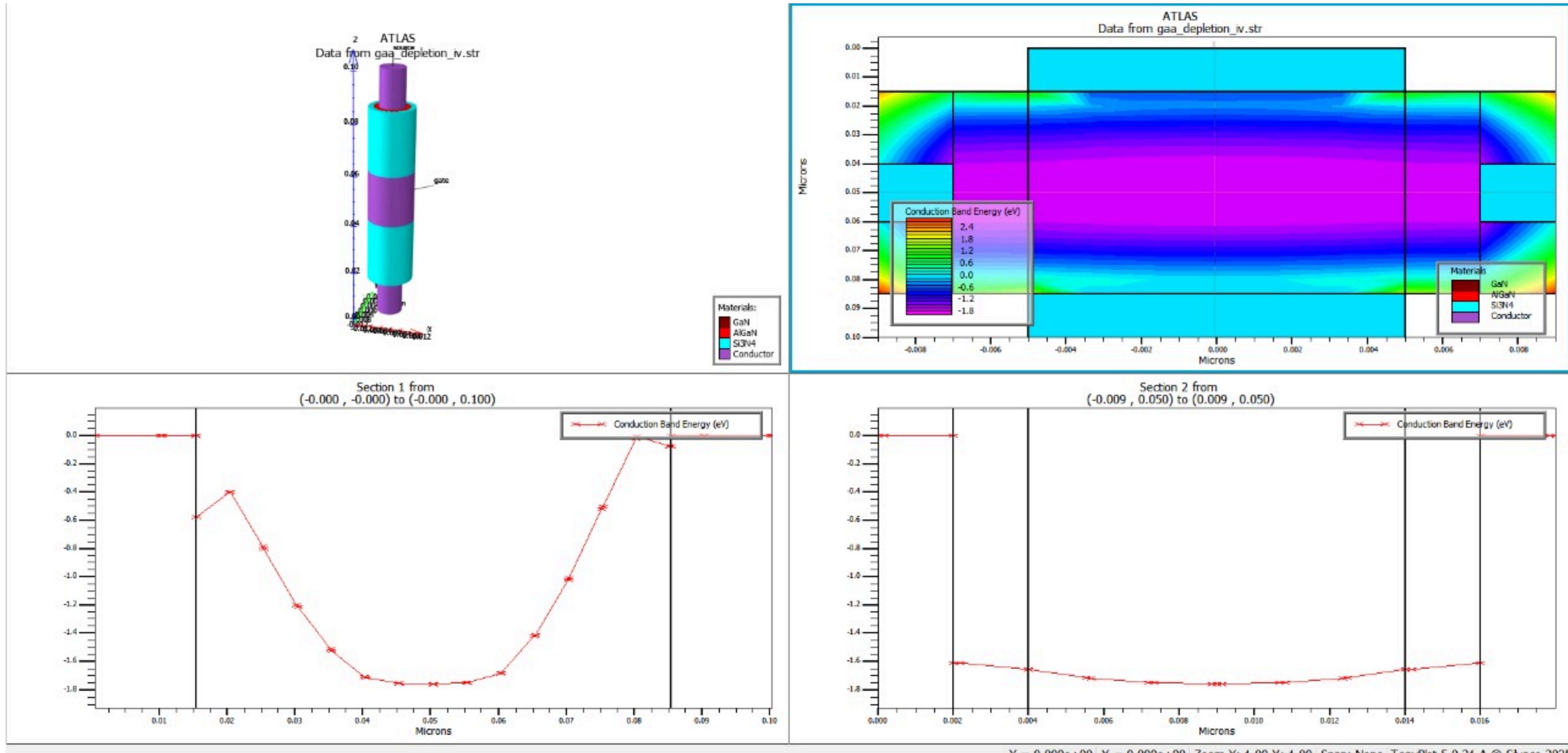
# ELECTRIC FIELD



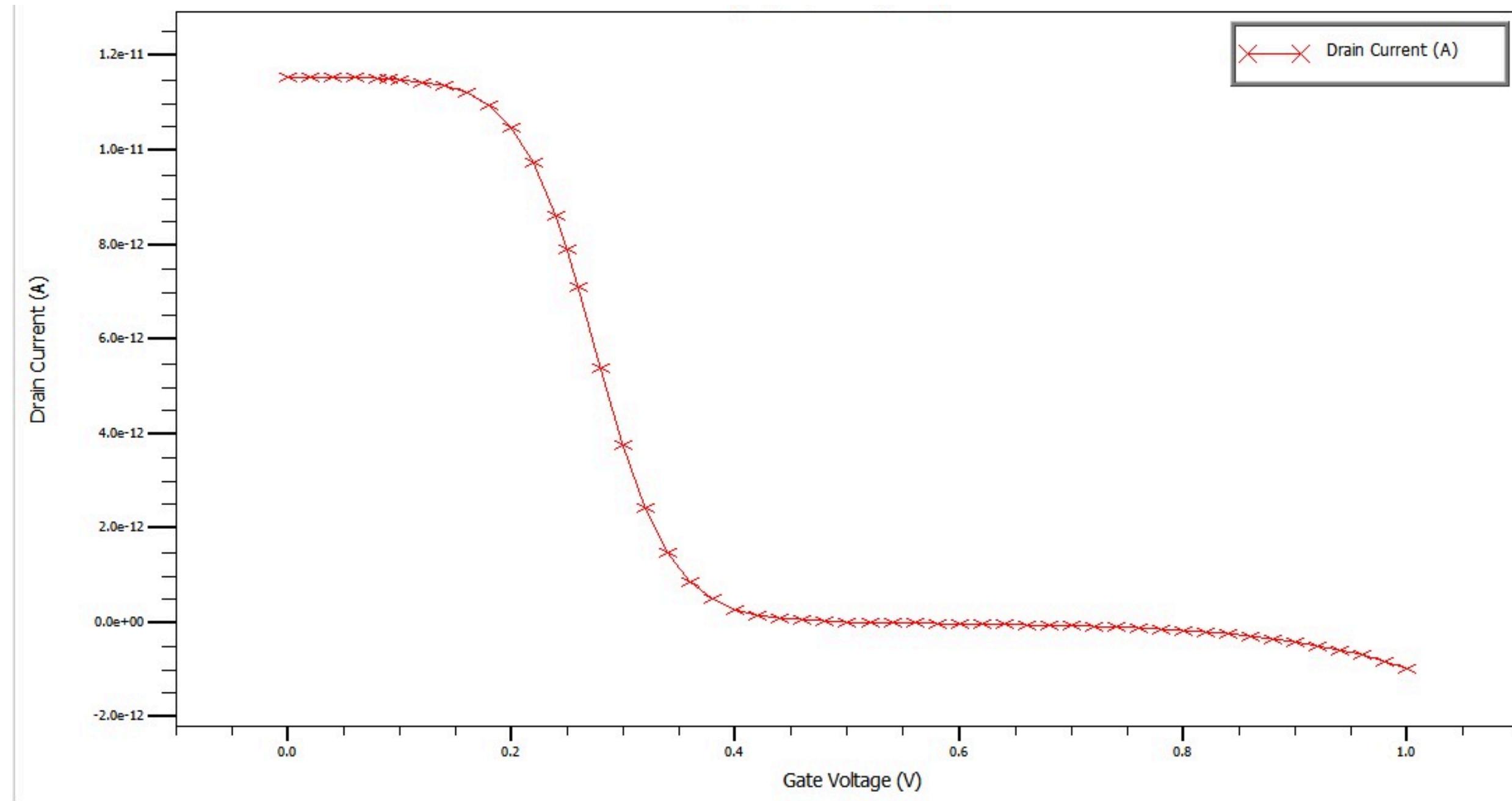
# VALENCE BAND ENERGY



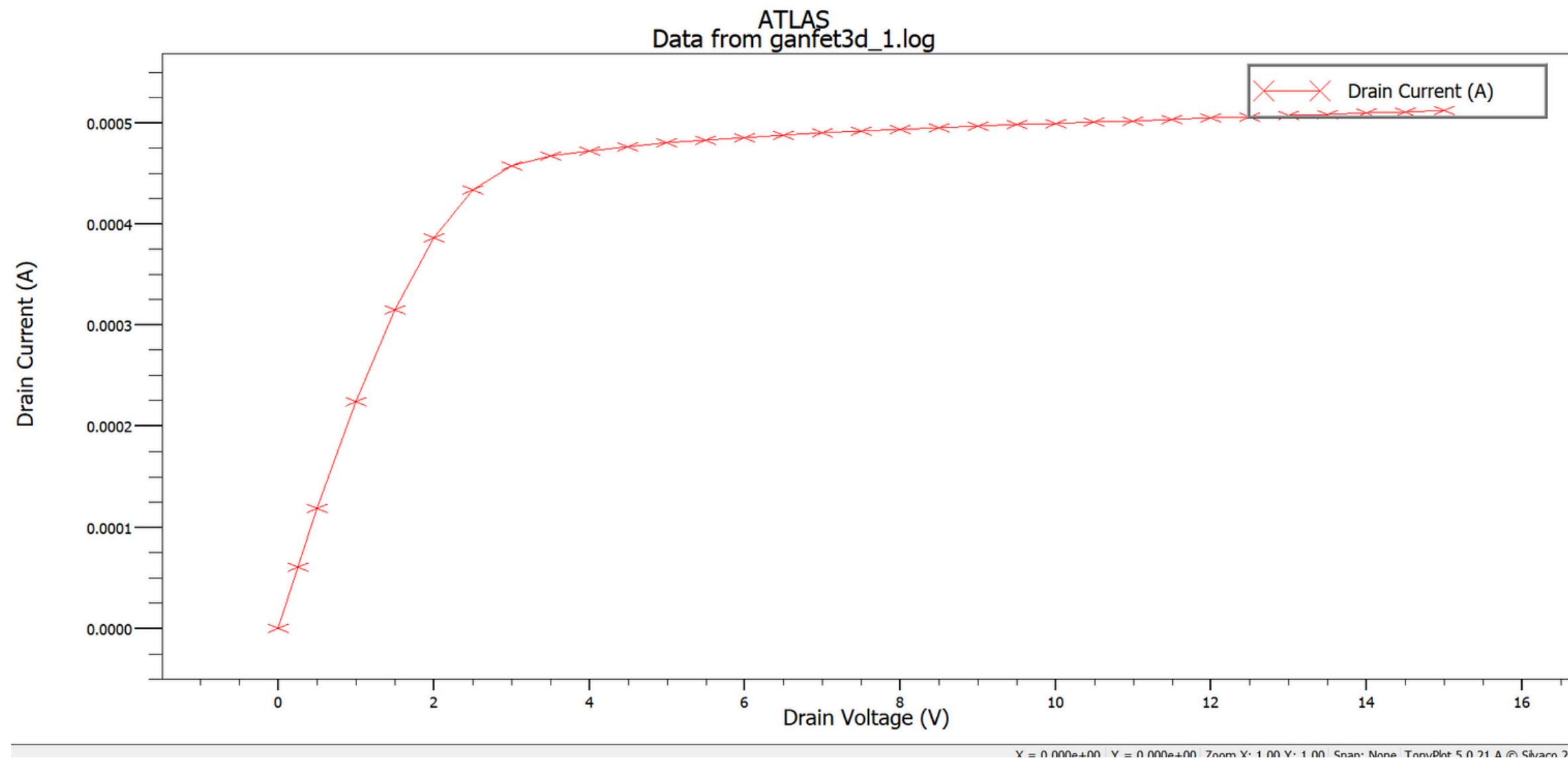
# CONDUCTION BAND ENERGY



# ID VS VGS



# ID VS VDS



The plot shape (**saturation beyond 4 V**) is for a nanowire HEMT.  
This shows nanowire geometry and models **are functioning properly – current increases linearly then saturates**.  
**Threshold voltage (V<sub>th</sub>): 0.46V**, confirming depletion-mode (normally-on) nanowire HEMT operation.  
The shift shows drain-induced barrier lowering (**DIBL ≈ 0.034/V**) – typical for GaN HEMTs of this scale.

```

) # === 3. Subthreshold Slope (SS) ===
EXTRACT> extract name="SS" 1.0/slope(maxslope(curve(v."gate", log10(abs(i."drain")))))
SS=0.0222626

) # === 4. On/Off Currents ===
EXTRACT> extract name="Ioff" y.val from curve(v."gate", i."drain") where x.val=0
Ioff=1.15363e-011
EXTRACT> extract name="Ion" y.val from curve(v."gate", i."drain") where x.val=2
Ion=-5.00344e-009
EXTRACT> extract name="Ion_Ioff" -5.00344e-009/1.15363e-011
Ion_Ioff=-433.713

) # === 5. DIBL Calculation (optional) ===
EXTRACT> init infile="sgo_gaa_Vd_005.log"
EXTRACT> extract name="Vth_lowVd" x.val from curve(v."gate", log10(abs(i."drain")))) where y.val=-7
Vth_lowVd=0.461016
)
EXTRACT> init infile="sgo_gaa_Vd_1.log"
EXTRACT> extract name="Vth_highVd" x.val from curve(v."gate", log10(abs(i."drain")))) where y.val=-7
Vth_highVd=0.429111
)
EXTRACT> extract name="DIBL" (0.461016 - 0.429111) / 0.95
DIBL=0.0335842

save outfile="gaa_depletion_extract.dat"
quit

```

Parameter	Value (approx.)	Meaning / Observation
$V_{th\_lowVd}$	0.46 V	Threshold voltage at low drain bias (1 V) – device begins to turn ON.
$V_{th\_highVd}$	0.43 V	Threshold voltage at high drain bias (15 V) – small shift, shows excellent gate control.
$\Delta V_{th}$	0.03 V	Tiny voltage shift between low and high drain bias; indicates suppressed short-channel effects.
DIBL	0.034 V/V	Extremely low drain-induced barrier lowering; strong immunity to short-channel effects.

## COMPARISON & Results Observed

# Comparison between Planar HEMT and Nanowire

Parameter	Planar HEMT	Nanowire / GAA HEMT
Drain current	High ( $10^{-4}$ – $10^{-3}$ A typical in simulation)	Lower ( $10^{-8}$ – $10^{-11}$ A typical)
Gate control	Weaker	Stronger (wraps all around)
Leakage	Higher	Very low
Power efficiency	Moderate	Higher
Device safety (normally-off)	No	Yes

Parameter	Planar AlGaN/GaN HEMT	Nanowire / GAA AlGaN/GaN HEMT
<b>Structure Type</b>	2D planar heterostructure (AlGaN barrier on GaN channel)	Cylindrical / Gate-all-around nanowire (3D confinement of channel)
<b>Regions of Operation</b>	1. Cutoff ( $V_{gs} < V_{th}$ ) 2. Linear ( $V_{ds} < V_{gs} - V_{th}$ ) 3. Saturation ( $V_{ds} \geq V_{gs} - V_{th}$ )	1. Subthreshold region 2. Linear region 3. Saturation / Velocity-sat region 4. Quantum confinement region (unique to nanowire)
<b>Typical <math>V_{gs}</math> Range</b>	-10 V → +1 V (depletion mode) or -5 V → +5 V (enhancement mode)	0 V → +2 V (GAA depletion-mode) or up to +3 V for enhancement-mode GAA
<b>Typical <math>V_{ds}</math> Range</b>	0 V → 20 V (for power and RF) High-voltage operation possible (>100 V for power GaN HEMTs)	0 V → 1–5 V (low-power logic or nanoscale device) Limited breakdown due to small radius
<b>Carrier Channel</b>	2DEG formed at AlGaN/GaN interface via polarization	Quasi-1D channel (2DEG wraps around the nanowire surface)

## **Control Gate Geometry**

Top gate (planar), Schottky or insulated

Gate-all-around (wraps fully around channel) → best electrostatic control

## **Applications**

RF power amplifiers,  
high-voltage power switches,  
microwave electronics

Low-power digital logic, sensors,  
quantum devices, next-gen HEMTs

## **Merits**

- Mature fabrication
- High current capability
- Easier contacts and scaling
- Proven for RF and power

- Superior gate control (no short-channel effects)
- Lower subthreshold slope
- Reduced DIBL
- Smaller footprint, better scaling
- High Ion/Ioff ratio

## **Demerits**

- Weaker gate control → DIBL & short-channel effects
- Larger parasitics
- Difficult to scale below 50 nm gate length
- Complex fabrication
- Hard to make uniform nanowires
- Higher surface trap density
- Thermal issues (limited heat flow)

## **Common Physical Models Used in ATLAS**

- SRH, FLDMOB, FERMI, POLAR- ALBRTC.N, FIELD.DEP- BGN (bandgap narrowing)- TRAP models for surface states
- All planar models +- BQP or DENSITY.GRADIENT (for quantum confinement)- POLARIZATION with CALC. STRAIN- FERMI, FLDMOB, SRH, AUGER

Device	DIBL	Vth_lowVd	Vth_highVd
GAA HEMT	0.0336	0.461 V	0.429 V
Planar HEMT	0.2222	-6.111 V	-3 V

Parameter	Value (approx.)	Meaning / Observation
Vth_lowVd	-6.11 V	Threshold voltage at low drain bias (1 V) – device starts to conduct.
Vth_highVd	-3.00 V	Threshold at high drain bias (15 V) – barrier reduced due to DIBL.
ΔVth	3.11 V	Voltage shift between low and high drain biases.
DIBL	-0.222 V/V	Drain-induced barrier lowering – moderate short-channel effect.
gm_max	~ $1.0 \times 10^{-5}$ A/V (estimated from slope of Id-Vg near -5 V → -3 V)	Peak transconductance; represents how effectively gate voltage controls drain current.

Device	DIBL	Vth_lowVd	Vth_highVd
GAA HEMT	0.0336	0.461 V	0.429 V
Planar HEMT	0.2222	-6.111 V	-3 V

Parameter	Value (approx.)	Meaning / Observation
Vth_lowVd	0.46 V	Threshold voltage at low drain bias (1 V) – device begins to turn ON.
Vth_highVd	0.43 V	Threshold voltage at high drain bias (15 V) – small shift, shows excellent gate control.
ΔVth	0.03 V	Tiny voltage shift between low and high drain bias; indicates suppressed short-channel effects.
DIBL	0.034 V/V	Extremely low drain-induced barrier lowering; strong immunity to short-channel effects.

# Applications

- 1.5G RF front-end modules → high-frequency amplifiers with low noise.
2. Satellite communication & RADAR systems → due to high breakdown voltage and RF power.
3. Power switching converters → efficient DC-DC & AC-DC converters in EVs/renewables.
4. High-power RF transmitters → defense and aerospace communication.
5. Millimeter-wave devices → for next-gen wireless (mmWave 28–100 GHz bands).

## Challenges Faced

- exclusion of self-heating and reliability analysis.
- Dimension Fixation.
- LACK OF PRECISE PAPERS FOR GAN/ALGAN NANOWIRE AND PLANAR HEMT.

# References

- [1.] T. Thingujam, D. -H. Son, J. -G. Kim, S. Cristoloveanu and J. -H. Lee, "Effects of Interface Traps and Self-Heating on the Performance of GAA GaN Vertical Nanowire MOSFET," in IEEE Transactions on Electron Devices, vol. 67, no. 3, pp. 816-821, March 2020, doi: [10.1109/TED.2019.2963427](https://doi.org/10.1109/TED.2019.2963427)
- [2.] K. -Y. Wong, W. Tang, K. M. Lau and K. J. Chen, "Planar Two-dimensional Electron Gas (2DEG) IDT SAW Filter on AlGaN/GaN Heterostructure," 2007 IEEE/MTT-S International Microwave Symposium, Honolulu, HI, USA, 2007, pp. 2043-2046, doi: [10.1109/MWSYM.2007.380252](https://doi.org/10.1109/MWSYM.2007.380252).
- [3.] P. K. Jena, S. Das, S. Bardhan, S. Misra, B. Baral and S. K. Pati, "Low Frequency Noise Analysis in AlGaN/GaN HEMTs," 2023 1st International Conference on Circuits, Power and Intelligent Systems (CCPIS), Bhubaneswar, India, 2023, pp. 1-4, doi: [10.1109/CCPIS59145.2023.10291825](https://doi.org/10.1109/CCPIS59145.2023.10291825).
- [4.] S. Chatterjee, A. Sengupta, S. Kundu and A. Islam, "Analysis of AlGaN/GaN high electron mobility transistor for high frequency application," 2017 Devices for Integrated Circuit (DevIC), Kalyani, India, 2017, pp. 196-199, doi: [10.1109/DEVIC.2017.8073935](https://doi.org/10.1109/DEVIC.2017.8073935)

**Thank  
You**