ASIC LAB

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CB.EN.P2VLD25017

Date: 3/12/2025

Eperiment No. 1

1. Ripple Carry Adder using 4 full Adders from Half adders

Design Code for Half Adder

```
module half_adder(input a,
                  input b,
                  output sum,
                  output carry);
                 assign sum = a^b;
                 assign carry= a&b;


endmodule
```

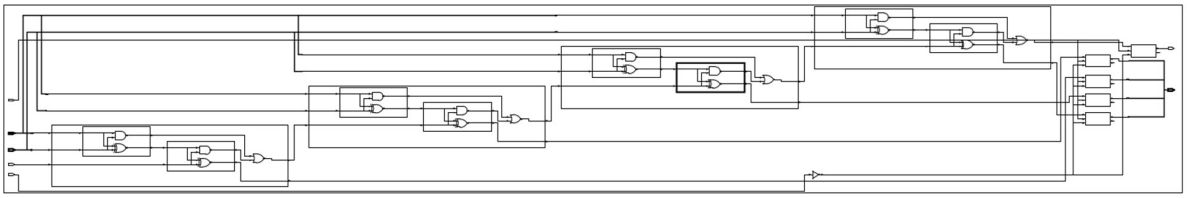
Design Code for Full Adder using half adder

```
module fa_ha(input a,
             input b,
             input cin,
             output sum,
             output carry);
        wire s1,c1,c2;
        half_adder h1(a,b,s1,c1);
        half_adder h2(cin,s1,sum,c2);
        or a1(carry,c1,c2);
endmodule
```

Design Code for Ripple Carry Adder (Top Module)

```
module rca_fa_ha(input [3:0] a,b,
                 input cin,clk,rst,
                  output reg [3:0]sum,
                     output reg carry);

    wire [3:0]c,s;

    fa_ha f1(a[0],b[0],cin,s[0],c[0]);

    genvar i;
    generate
    for(i=1;i<4;i=i+1)
    begin
    fa_ha fag(a[i],b[i],c[i-1],s[i],c[i]);
    end
    endgenerate

always@(posedge clk or posedge rst)
begin
    if(rst) begin
    sum<=4'b0;
    carry<=1'b0;
    end
    else begin
    sum <={s[3],s[2],s[1],s[0]};
    carry<=c[3];
    end
end
endmodule
```

Schematic View



Area Report

```
****************************************
Report : area
Design : rca_fa_ha
Version: V-2023.12
Date   : Thu Dec  4 04:26:32 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed90nm_max_htm_hvt_ccs (File: /home/c2user16/asic_17/saed90nm_max_htm_hvt_ccs.db)

Number of ports:                           68
Number of nets:                            89
Number of cells:                           38
Number of combinational cells:             21
Number of sequential cells:                 5
Number of macros/black boxes:               0
Number of buf/inv:                          1
Number of references:                       6

Combinational area:                204.595201
Buf/Inv area:                        5.529600
Noncombinational area:             161.280003
Macro/Black Box area:                0.000000
Net Interconnect area:               8.712571

Total cell area:                   365.875204
Total area:                        374.587776
```

Power Report

```
****************************************
Report : power
        -analysis_effort low
Design : rca_fa_ha
Version: V-2023.12
Date   : Thu Dec  4 04:26:36 2025
****************************************


Library(s) Used:

    saed90nm_max_htm_hvt_ccs (File: /home/c2user16/asic_17/saed90nm_max_htm_hvt_ccs.db)


Operating Conditions: WORST   Library: saed90nm_max_htm_hvt_ccs
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
rca_fa_ha              8000              saed90nm_max_htm_hvt_ccs
fa_ha_0                ForQA             saed90nm_max_htm_hvt_ccs
half_adder_0           ForQA             saed90nm_max_htm_hvt_ccs
fa_ha_1                ForQA             saed90nm_max_htm_hvt_ccs
fa_ha_2                ForQA             saed90nm_max_htm_hvt_ccs
fa_ha_3                ForQA             saed90nm_max_htm_hvt_ccs
half_adder_1           ForQA             saed90nm_max_htm_hvt_ccs
half_adder_2           ForQA             saed90nm_max_htm_hvt_ccs
half_adder_3           ForQA             saed90nm_max_htm_hvt_ccs
half_adder_4           ForQA             saed90nm_max_htm_hvt_ccs
half_adder_5           ForQA             saed90nm_max_htm_hvt_ccs
half_adder_6           ForQA             saed90nm_max_htm_hvt_ccs
half_adder_7           ForQA             saed90nm_max_htm_hvt_ccs


Global Operating Voltage = 0.65
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW
```

```
Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.2771 uW   (92%)
  Net Switching Power  = 114.3750 nW    (8%)
                         ---------
Total Dynamic Power    =   1.3915 uW  (100%)

Cell Leakage Power     = 142.2353 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power
(   %    )  Attrs
------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000
(   0.00%)
memory             0.0000            0.0000            0.0000            0.0000
(   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000
(   0.00%)
clock_network      0.6867            0.0000            0.0000            0.6867
(  44.77%)  i
register       4.1557e-02        4.0248e-05        5.1857e+04        9.3454e-02
(   6.09%)
sequential         0.0000            0.0000            0.0000            0.0000
(   0.00%)
combinational      0.5489            0.1143        9.0378e+04            0.7536
(  49.13%)
------------------------------------------------------------------------------------------
Total              1.2771 uW         0.1144 uW     1.4224e+05 pW         1.5337 uW
```

Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : rca_fa_ha
Version: V-2023.12
Date   : Thu Dec  4 04:26:43 2025
****************************************

Operating Conditions: WORST   Library: saed90nm_max_htm_hvt_ccs
Wire Load Model Mode: enclosed

  Startpoint: a[0] (input port clocked by clk)
  Endpoint: carry_reg (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model   |    Library
  ------------------------------------------------
  rca_fa_ha          8000                saed90nm_max_htm_hvt_ccs
  fa_ha_0            ForQA               saed90nm_max_htm_hvt_ccs
  fa_ha_3            ForQA               saed90nm_max_htm_hvt_ccs
  fa_ha_2            ForQA               saed90nm_max_htm_hvt_ccs
  fa_ha_1            ForQA               saed90nm_max_htm_hvt_ccs

-----------------------------------------
```

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	2.00	2.00 f
a[0] (in)	0.00	2.00 f
f1/a (fa_ha_0)	0.00	2.00 f
f1/h1/a (half_adder_0)	0.00	2.00 f
f1/h1/U1/Q (XOR2X1_HVT)	1.39	3.39 r
f1/h1/sum (half_adder_0)	0.00	3.39 r
f1/h2/b (half_adder_7)	0.00	3.39 r
f1/h2/U2/Q (AND2X1_HVT)	0.92	4.31 r
f1/h2/carry (half_adder_7)	0.00	4.31 r
f1/U1/Q (OR2X1_HVT)	0.63	4.94 r
f1/carry (fa_ha_0)	0.00	4.94 r
genblk1[1].fag/cin (fa_ha_3)	0.00	4.94 r
genblk1[1].fag/h2/a (half_adder_5)	0.00	4.94 r
genblk1[1].fag/h2/U2/Q (AND2X1_HVT)	0.92	5.86 r
genblk1[1].fag/h2/carry (half_adder_5)	0.00	5.86 r
genblk1[1].fag/U1/Q (OR2X1_HVT)	0.63	6.49 r
genblk1[1].fag/carry (fa_ha_3)	0.00	6.49 r
genblk1[2].fag/cin (fa_ha_2)	0.00	6.49 r
genblk1[2].fag/h2/a (half_adder_3)	0.00	6.49 r

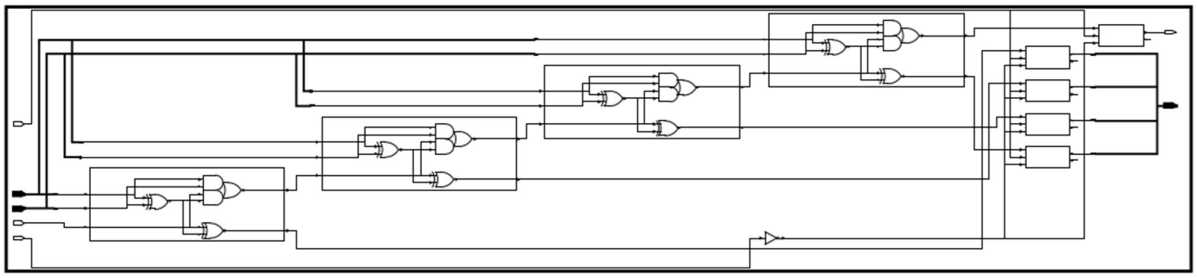
```
genblk1[2].fag/h2/U2/Q (AND2X1_HVT)                    0.92       7.41 r
genblk1[2].fag/h2/carry (half_adder_3)                 0.00       7.41 r
genblk1[2].fag/U1/Q (OR2X1_HVT)                        0.63       8.04 r
genblk1[2].fag/carry (fa_ha_2)                         0.00       8.04 r
genblk1[3].fag/cin (fa_ha_1)                           0.00       8.04 r
genblk1[3].fag/h2/a (half_adder_1)                     0.00       8.04 r
genblk1[3].fag/h2/U2/Q (AND2X1_HVT)                    0.92       8.96 r
genblk1[3].fag/h2/carry (half_adder_1)                 0.00       8.96 r
genblk1[3].fag/U1/Q (OR2X1_HVT)                        0.60       9.55 r
genblk1[3].fag/carry (fa_ha_1)                         0.00       9.55 r
carry_reg/D (DFFARX1_HVT)                              0.03       9.58 r
data arrival time                                                 9.58

clock clk (rise edge)                                 20.00      20.00
clock network delay (ideal)                            0.00      20.00
carry_reg/CLK (DFFARX1_HVT)                            0.00      20.00 r
library setup time                                    -1.07      18.93
data required time                                               18.93
--------------------------------------------------------------------------
data required time                                               18.93
data arrival time                                                -9.58
--------------------------------------------------------------------------
slack (MET)                                                       9.34
```

2. Ripple Carry Adder using 4 full Adders

Design Code for Ripple Carry Adder (Top Module)

```
module rca_4fa(input [3:0]a,b,
        input cin,
        input rst,clk,
        output reg [3:0]sum,
        output reg carry);

    wire [3:0]c,s;
    full_adder f1(a[0],b[0],cin,s[0],c[0]);
    genvar i;
    generate
    for(i=1;i<4;i=i+1)
    begin
    full_adder fag(a[i],b[i],c[i-1],s[i],c[i]);
    end
    endgenerate


always@(posedge clk or posedge rst)
begin
    if(rst) begin
    sum<=4'b0;
    carry<=1'b0;
    end
    else begin
    sum <={s[3],s[2],s[1],s[0]};
    carry<=c[3];
    end
end
endmodule
```

Schematic View



Area Report

```
****************************************
Report : area
Design : rca_4fa
Version: V-2023.12
Date   : Thu Dec  4 04:14:22 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed90nm_max_htm_hvt_ccs (File: /home/c2user16/asic_17/saed90nm_max_htm_hvt_ccs.db)

Number of ports:                           36
Number of nets:                            49
Number of cells:                           22
Number of combinational cells:             13
Number of sequential cells:                 5
Number of macros/black boxes:               0
Number of buf/inv:                          1
Number of references:                       6

Combinational area:                164.044802
Buf/Inv area:                        5.529600
Noncombinational area:             161.280003
Macro/Black Box area:                0.000000
Net Interconnect area:               8.050569

Total cell area:                   325.324804
Total area:                        333.375373
```

Power Report

```
****************************************
Report : power
        -analysis_effort low
Design : rca_4fa
Version: V-2023.12
Date   : Thu Dec  4 04:15:14 2025
****************************************


Library(s) Used:

    saed90nm_max_htm_hvt_ccs (File: /home/c2user16/asic_17/saed90nm_max_htm_hvt_ccs.db)


Operating Conditions: WORST   Library: saed90nm_max_htm_hvt_ccs
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
rca_4fa               8000               saed90nm_max_htm_hvt_ccs
full_adder_0          ForQA              saed90nm_max_htm_hvt_ccs
full_adder_1          ForQA              saed90nm_max_htm_hvt_ccs
full_adder_2          ForQA              saed90nm_max_htm_hvt_ccs
full_adder_3          ForQA              saed90nm_max_htm_hvt_ccs


Global Operating Voltage = 0.65
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------

Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.1812 uW   (93%)
  Net Switching Power  =  90.0034 nW    (7%)
                         ---------
Total Dynamic Power    =   1.2712 uW  (100%)

Cell Leakage Power     = 111.9263 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
---------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.6867           0.0000            0.0000            0.6867  (  49.65%)  i
register       4.4344e-02       4.0114e-05        5.1863e+04        9.6248e-02  (   6.96%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational      0.4501       8.9963e-02        6.0063e+04            0.6002  (  43.39%)
---------------------------------------------------------------------------------------------------
Total              1.1812 uW     9.0003e-02 uW     1.1193e+05 pW         1.3831 uW
```

Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : rca_4fa
Version: V-2023.12
Date   : Thu Dec  4 04:15:33 2025
****************************************

Operating Conditions: WORST   Library: saed90nm_max_htm_hvt_ccs
Wire Load Model Mode: enclosed

  Startpoint: b[0] (input port clocked by clk)
  Endpoint: carry_reg (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  rca_4fa            8000                  saed90nm_max_htm_hvt_ccs
  full_adder_0       ForQA                 saed90nm_max_htm_hvt_ccs

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     2.00       2.00 f
  b[0] (in)                                0.00       2.00 f
  f1/b (full_adder_0)                      0.00       2.00 f
  f1/U3/Q (XOR2X1_HVT)                     1.39       3.39 r
  f1/U2/Q (AO22X1_HVT)                     1.15       4.54 r
  f1/carry (full_adder_0)                  0.00       4.54 r
  genblk1[1].fag/cin (full_adder_3)        0.00       4.54 r
  genblk1[1].fag/U2/Q (AO22X1_HVT)         1.14       5.68 r
  genblk1[1].fag/carry (full_adder_3)      0.00       5.68 r
  genblk1[2].fag/cin (full_adder_2)        0.00       5.68 r
  genblk1[2].fag/U2/Q (AO22X1_HVT)         1.14       6.82 r
  genblk1[2].fag/carry (full_adder_2)      0.00       6.82 r
  genblk1[3].fag/cin (full_adder_1)        0.00       6.82 r
```

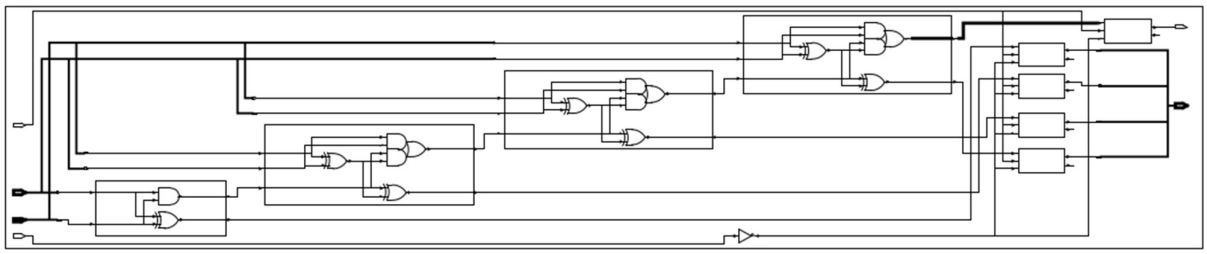
```
genblk1[3].fag/U2/Q (AO22X1_HVT)          1.09       7.91 r
genblk1[3].fag/carry (full_adder_1)       0.00       7.91 r
carry_reg/D (DFFARX1_HVT)                 0.03       7.94 r
data arrival time                                    7.94

clock clk (rise edge)                    20.00      20.00
clock network delay (ideal)               0.00      20.00
carry_reg/CLK (DFFARX1_HVT)               0.00      20.00 r
library setup time                       -1.16      18.84
data required time                                  18.84
-----------------------------------------------------------
data required time                                  18.84
data arrival time                                   -7.94
-----------------------------------------------------------
slack (MET)                                         10.91
```

3. Ripple Carry Adder using 3 full Adders and LSB as a Half Adder

Design Code for Ripple Carry Adder (Top Module)

```
module rca_3fa__lsb_ha(input [3:0]a,b,
                       input rst,clk,
                       output reg [3:0]sum,
                       output reg carry);


                wire [3:0]c,s;
                half_adder h1(a[0],b[0],s[0],c[0]);
                genvar i;
                generate
                for(i=1;i<4;i=i+1)
                begin
                full_adder fag(a[i],b[i],c[i-1],s[i],c[i]);
                end
                endgenerate


always@(posedge clk or posedge rst)
begin
        if(rst) begin
        sum<=4'b0;
        carry<=1'b0;
        end
        else begin
        sum <={s[3],s[2],s[1],s[0]};
        carry<=c[3];
        end
end
endmodule
```

Schematic View



Area Report

```
****************************************
Report : area
Design : rca_3fa__lsb_ha
Version: V-2023.12
Date   : Thu Dec  4 04:21:49 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed90nm_max_htm_hvt_ccs (File: /home/c2user16/asic_17/saed90nm_max_htm_hvt_ccs.db)

Number of ports:                           34
Number of nets:                            46
Number of cells:                           21
Number of combinational cells:             12
Number of sequential cells:                 5
Number of macros/black boxes:               0
Number of buf/inv:                          1
Number of references:                       6

Combinational area:                145.612802
Buf/Inv area:                        5.529600
Noncombinational area:             161.280003
Macro/Black Box area:                0.000000
Net Interconnect area:               7.547613

Total cell area:                   306.892804
Total area:                        314.440417
```

Power Report

```
****************************************
Report : power
        -analysis_effort low
Design : rca_3fa__lsb_ha
Version: V-2023.12
Date   : Thu Dec  4 04:22:06 2025
****************************************


Library(s) Used:

    saed90nm_max_htm_hvt_ccs (File: /home/c2user16/asic_17/saed90nm_max_htm_hvt_ccs.db)


Operating Conditions: WORST   Library: saed90nm_max_htm_hvt_ccs
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
rca_3fa__lsb_ha        8000              saed90nm_max_htm_hvt_ccs
half_adder             ForQA             saed90nm_max_htm_hvt_ccs
full_adder_0           ForQA             saed90nm_max_htm_hvt_ccs
full_adder_1           ForQA             saed90nm_max_htm_hvt_ccs
full_adder_2           ForQA             saed90nm_max_htm_hvt_ccs


Global Operating Voltage = 0.65
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW

-----------------------------------------

Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.1027 uW   (94%)
  Net Switching Power  =  76.4424 nW    (6%)
                         ---------
Total Dynamic Power    =   1.1792 uW  (100%)

Cell Leakage Power     = 106.2651 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
---------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000           0.0000  (   0.00%)
clock_network      0.6867           0.0000            0.0000           0.6867  (  53.42%)  i
register       3.8894e-02       3.7089e-05        5.1751e+04       9.0682e-02  (   7.05%)
sequential         0.0000           0.0000            0.0000           0.0000  (   0.00%)
combinational      0.3772       7.6405e-02        5.4514e+04           0.5081  (  39.53%)
---------------------------------------------------------------------------------------------------
Total              1.1027 uW     7.6442e-02 uW     1.0627e+05 pW        1.2854 uW
```

Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : rca_3fa__lsb_ha
Version: V-2023.12
Date   : Thu Dec  4 04:22:25 2025
****************************************

Operating Conditions: WORST   Library: saed90nm_max_htm_hvt_ccs
Wire Load Model Mode: enclosed

  Startpoint: b[1] (input port clocked by clk)
  Endpoint: carry_reg (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  rca_3fa__lsb_ha    8000                  saed90nm_max_htm_hvt_ccs
  full_adder_0       ForQA                 saed90nm_max_htm_hvt_ccs

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     2.00       2.00 f
  b[1] (in)                                0.00       2.00 f
  genblk1[1].fag/b (full_adder_0)          0.00       2.00 f
  genblk1[1].fag/U3/Q (XOR2X1_HVT)         1.39       3.39 r
  genblk1[1].fag/U2/Q (AO22X1_HVT)         1.15       4.54 r
  genblk1[1].fag/carry (full_adder_0)      0.00       4.54 r
  genblk1[2].fag/cin (full_adder_2)        0.00       4.54 r
  genblk1[2].fag/U2/Q (AO22X1_HVT)         1.14       5.68 r
  genblk1[2].fag/carry (full_adder_2)      0.00       5.68 r
  genblk1[3].fag/cin (full_adder_1)        0.00       5.68 r
  genblk1[3].fag/U2/Q (AO22X1_HVT)         1.09       6.77 r
  genblk1[3].fag/carry (full_adder_1)      0.00       6.77 r
  carry_reg/D (DFFARX1_HVT)                0.03       6.80 r
  data arrival time                                   6.80
```

```
clock clk (rise edge)                    20.00      20.00
clock network delay (ideal)               0.00      20.00
carry_reg/CLK (DFFARX1_HVT)               0.00      20.00 r
library setup time                       -1.16      18.84
data required time                                  18.84
-----------------------------------------------------------
data required time                                  18.84
data arrival time                                   -6.80
-----------------------------------------------------------
slack (MET)                                         12.05
```

Comparison

Parameter	RCA (FA-from-HA)	RCA (4FA)	RCA (3FA + LSB HA)
Total Cell Area (µm²)	**374.587**	**333.373**	**314.440**
Combinational Area (µm²)	204.595	164.044	145.613
Sequential Area (µm²)	0	0	0
Total Power (µW)	**1.5337 µW**	**2.1219 µW**	**1.6027 µW**
Internal Power (µW)	1.2771	1.8324	1.2605
Switching Power (µW)	0.1144	0.2895	0.1635
Leakage (nW)	142.253	0.923	0.992
Worst-case Data Arrival Time (ns)	**9.58 ns**	**6.82 ns**	**6.87 ns**
Slack	+9.34 ns	+13.18 ns	+13.13 ns
Speed Ranking	Slowest	**Fastest**	Near-fast

Inference / Conclusion

Area

- **Lowest area:** *3FA + LSB HA* (314 μm²)
- This is because replacing one full adder with a half adder reduces logic complexity.
- **Highest area:** FA-from-HA RCA — because every FA is built from **two half adders + OR**, making it gate-heavy.

Power

- **Lowest power:** FA-from-HA RCA (1.53 μW).
    - Even though structurally inefficient, each HA cell has lower internal activity, reducing overall dynamic power.
- **Highest power:** 4FA RCA (2.12 μW).
    - Full adders generate more switching and internal capacitance → higher dynamic power.

Timing

- **Fastest:** 4FA RCA (6.82 ns).
    - Direct FA → FA chaining avoids extra XOR/AND/OR levels.
- **Slowest:** FA-from-HA (9.58 ns).
    - Because sum and carry propagate through **two HAs + OR gate**, increasing logic depth.
- *3FA + HA* lands very close to 4FA (6.87 ns), making it nearly as fast.

Overall Balanced Design

3FA + LSB HA RCA

- Lowest area
- Low power
- Almost-fastest timing
- Most area/power efficient without sacrificing speed