Single-Electron Transistors

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Abstract. Single-electron transistors (SET's) are often discussed as elements of nanometer scale electronic circuits because they can be made very small and they can detect the motion of individual electrons. However, SET's have low voltage gain, high output impedances, and are sensitive to random background charges. This makes it unlikely that single-electron transistors would ever replace field-effect transistors (FET's) in applications where large voltage gain or low output impedance is necessary. The most promising applications for SET's are charge-sensing applications such as the readout of few electron memories, the readout of charge-coupled devices, and precision charge measurements in metrology.

1. Introduction

Single-electron transistors [1] have been made with critical dimensions of just a few nanometers using metals, [2] semiconductors, [3] carbon nanotubes, [4] and individual molecules. [5-7] Some of the smallest transistors operate at room temperature. In this paper, first some basics of single-electron transistors are introduced and then a few different kinds of SET's are described. The real problems preventing the use of SET's in most applications are the low gain, the high output impedance, and the background charges. Each of these problems is discussed and the circuits where SET's show the most promise are described.

2. SET Basics

A single-electron transistor consists of a small conducting island coupled to source and drain leads by tunnel junctions and capacitively coupled to one or more gates. The geometry of a SET is shown in Fig. 1(a) and the equivalent electrical circuit is shown in Fig. 1(b). A stray capacitance C_0 from the island to ground and a random background charge on the island Q_0 are also included in the model. There are two gates in the equivalent circuit because two gates are often used in practice. For example, one gate can be used to tune the background charge while the other is used as the input of the SET. A straightforward electrostatic calculation shows that the voltage of the island as a function of the number of electrons on the island is,

$$V(n) = (-ne + Q_0 + C_1V_1 + C_2V_2 + C_{g1}V_{g1} + C_{g2}V_{g2})/C_\Sigma. \qquad [1]$$

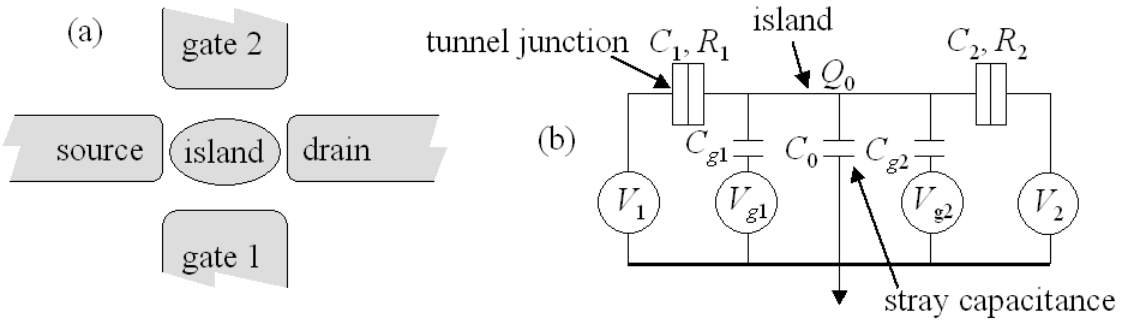

Fig. 1 (a) The geometry of a SET with two gates. (b) The equivalent circuit for a SET.

Here n is the number of electrons on the island, e is the positive elementary charge, and C_Σ is the total capacitance of the island $C_\Sigma = C_1 + C_2 + C_{g1} + C_{g2} + C_0$. The energy it takes to move an infinitesimally small charge dq from ground at a potential $V = 0$ to the island is Vdq. As soon as charge is added to the island, the voltage of the island changes. The energy needed to take a whole electron from ground and put it on the island is,

$$\int_0^{-e} Vdq = -eV(n) + \frac{e^2}{2C_\Sigma}. \qquad [2]$$

Here n is the number of electrons on the island before the final electron is added. The term $E_c = e^2/(2C_\Sigma)$ is called the charging energy and it sets the energy scale for single-electron effects. The charging energy is typically in the range 1 - 100 meV.

There are four single-electron tunneling events that can take place. An electron can tunnel left through junction 1, right through junction 1, left through junction 2 or right through junction 2. The energies associated with these four tunnel events can be calculated using Eq. 2,

$$\begin{aligned} \Delta E_{1R} &= eV_1 - eV(n) + E_c, \quad & \Delta E_{1L} &= -eV_1 + eV(n) + E_c, \\ \Delta E_{2R} &= -eV_2 + eV(n) + E_c, \quad & \Delta E_{2L} &= eV_2 - eV(n) + E_c. \end{aligned} \qquad [3]$$

If any of these energies are negative, an electron will tunnel. If all four of these energies are positive, a condition known as the Coulomb blockade is achieved and no electrons will tunnel. Figure 2 shows a calculation of the conductance of a SET as a function of the gate voltage and the bias voltage. The straight lines that form the edges of the diamond shaped regions are given by setting $\Delta E = 0$ in Eqs. 3. The diamond labeled 0 is a region of Coulomb blockade where there are zero excess electrons on the island and the diamond labeled 1 is a region of Coulomb blockade with one excess electron on the island, etc. When a bias voltage is applied that is great enough to overcome the Coulomb blockade, current flows as electrons tunnel from the source onto the island and then from the island to the drain. In the region labeled (0,1), only one electron at a time can pass through the SET at low temperatures. Exact formulas for the current in each diamond can be derived in the limit of low temperature. For all of the diamonds labeled with just a single number n, the current is zero. In the diamonds labeled by two numbers (n,n+1) the charge on the island is alternately n and n+1 as current flows through the SET. The formula for the current in this case is,

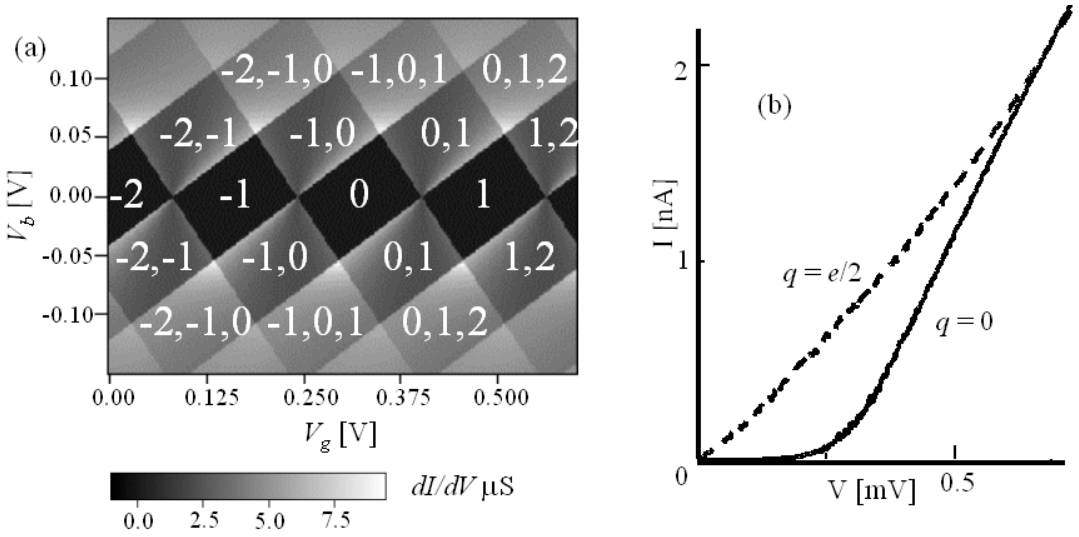

Fig. 2 (a) The calculated conductance (dI/dV) through a SET plotted as a function of the gate voltage and the bias voltage. The diamonds are labeled with the charge states that are occupied at low temperature. (b) The experimental current-voltage characteristics of a SET are shown for two values of the gate. The solid line is for an induced gate charge of zero; this is the condition for maximum Coulomb blockade. The dashed line is for an induced gate charge of $e/2$; this is the minimum Coulomb blockade.

$$I = \frac{ab}{C_\Sigma\left(R_2 a + R_1 b\right)}, \qquad [4]$$

where $a = C_\Sigma V_1 + ne - Q_0 - C_1 V_1 - C_2 V_2 - C_{g1} V_{g1} - C_{g2} V_{g2} + e/2$ and $b = -C_\Sigma V_2 - ne + Q_0 + C_1 V_1 + C_2 V_2 + C_{g1} V_{g1} + C_{g2} V_{g2} - e/2$. This is a useful formula because in most applications a SET is biased in the (n,n+1) diamond. From this formula, the voltage gain can be determined. For a current biased SET, the maximum voltage gain is $-C_{g1}/C_1$ if junction 2 is grounded and $-C_{g1}/C_2$ if junction 1 is grounded. The maximum transconductance (dI/dV_{g1}) at low temperatures can also be determined from Eq. 4. Near the boundary between the diamonds labeled n and n,n+1; the quantity $b \approx 0$ and the transconductance is $dI/dV_{g1} \approx C_g/(R_2 C_\Sigma)$. Near the boundaries between the diamond labeled n,n+1 and n+1; the quantity $a \approx 0$ and the transconductance is $dI/dV_{g1} \approx -C_g/(R_1 C_\Sigma)$. The individual resistances of the two junctions in a SET are typically determined by measuring the transconductance.

As more charge states are included, the formula for the current gets more complicated. The formula for the current in the diamonds labeled (n-1,n,n+1) is,

$$I = \frac{R_1(a+(n-1)e)(b-ne)(b-(n-1)e) + R_2(a+(n-1)e)(a+ne)(b-ne)}{C_\Sigma\left(R_2^2(a+(n-1)e)(a+ne) + R_1 R_2(a+(n-1)e)(b-ne) + R_1^2(b-(n-1)e)(b-ne)\right)}. \qquad [5]$$

3. Types of single-electron transistors

Single-electron transistors can be made using metals, semiconductors, carbon nanotubes, or single molecules. Aluminum SET's made with $Al/AlO_x/Al$ tunnel junctions are the SET's that have been used most often in applications. This kind of SET is used in metrology to measure currents, capacitance, and charge. [8] They are used in astronomical measurements [9] and they have been used to make primary

thermometers. [10] However, many fundamental single-electron measurements have been made using GaAs heterostructures. The island of this kind of SET is often called a quantum dot. Quantum dots have been very important in contributing to our understanding of single-electron effects because it is possible to have just one or a few conduction electrons on a quantum dot. The quantum states that the electrons occupy are similar to electron states in an atom and quantum dots are therefore sometimes called artificial atoms. The energy necessary to add an electron to a quantum dot depends not just on the electrostatic energy of Eq. 2 but also on the quantum confinement energy and the magnetic energy associated with the spin of the electron states. By measuring the current that flows thorough a quantum dot as a function of the gate voltage, magnetic field, and temperature allows one understand the quantum states of the dot in quite some detail. [11]

The SET's described so far are all relatively large and have to be measured at low temperature, typically below 100 mK. For higher temperature operation, the SET's have to be made smaller. Ono et al. [3] used a technique called pattern dependent oxidation (PADOX) to make small silicon SET's. These SET's had junction capacitances of about 1 aF and a charging energy of 20 meV. The silicon SET's have the distinction of being the smallest SET's that have been incorporated into circuits involving more than one transistor. Specifically, Ono et al. constructed an inverter that operated at 27 K. Postma et al. [4] made a SET that operates at room temperature by using an AFM to buckle a metallic carbon nanotube in two places. The tube buckles much the same way as a drinking straw buckles when it is bent too far. Using this technique, a 25 nm section of the nanotube between the buckles was used as the island of the SET and a conducting substrate was used as the gate. The total capacitance achievable in this case is also about 1 aF. Pashkin et al. [2] used e-beam lithography to fabricate a SET with an aluminum island that had a diameter of only 2 nm. This SET had junction capacitances of 0.7 aF, a charging energy of 115 meV, and operated at room temperature. SET's have also been made by placing just a single molecule between closely spaced electrodes. Park et al. [5] built a SET by placing a C_{60} molecule between electrodes spaced 1.4 nm apart. The total capacitance of the C_{60} molecule in this configuration was about 0.3 aF. Individual molecules containing a Co ion bonded to polypyridyl ligands were also placed between electrodes only 1-2 nm apart to fabricate a SET. [6] In similar work, Liang et al. [7] placed a single divanadium molecule between closely spaced electrodes to make a SET. In the last two experiments, the Kondo effect was observed as well as the Coulomb blockade. The charging energy in the molecular devices was above 100 meV.

One of the conclusions that can be drawn from this review of SET devices is that small SET's can be made out a of variety of materials. Single electron transistors with a total capacitance of about 1 aF were made with aluminum, silicon, carbon nanotubes and individual molecules. It seems unlikely that SET's with capacitances smaller than the capacitances of the molecular devices can be made. This sets a lower limit on the smallest capacitances that can be achieved at about 0.1 aF. Achieving small capacitances such as this has been a goal of many groups working on SET's. However, while some of the device characteristics improve as a SET is made smaller, some of the device characteristics get worse as SET's are made smaller. For some applications, the single molecule SET's are too small to be useful. As SET's are made smaller, there is an increase in the operating temperature, the operating frequency, and the device packing density. These are desirable consequences of the shrinking of SET devices. The undesirable consequences of the shrinking of SET's are that the electric fields increase, the current densities increase, the operating voltage increases, the energy dissipated per switching event increases, and the power dissipated per unit area increases, the voltage

gain decreases, the charge gain decreases, and the number of Coulomb oscillations that can be observed decrease.

4. The problems: gain, high output impedance, and background charges

Voltage gain is one of the properties of a SET that decreases as SET's are made smaller. This is because voltage gain decreases with decreasing gate capacitance. It is difficult to achieve a large gate capacitance when the island of a SET consists of a single molecule. For the single molecule devices, the gate capacitance can be as small as a few zeptoFarads. In this case, tens of volts have to be applied at the input to modulate the output by tens of millivolts. This results in a voltage gain on the order of 0.001; the transistors attenuate the signals by a factor of about 1000. The voltage gain in a SET is the ratio of the gate capacitance to the junction capacitance. As the gate capacitance is increased for fixed junction capacitance and fixed temperature, the voltage gain first increases and then it decreases. This is illustrated in Fig. 3(a) where the voltage gain is plotted as a function of gate capacitance for different temperatures. In all of the curves the junction capacitance is assumed to be 0.1 aF. The voltage gain increases with increasing gate capacitance until the charging energy is on the order of k_BT and then the voltage gain drops sharply.

Thus for every junction capacitance and temperature, there is a maximum voltage gain. Figure 3(b) is a plot of the maximum gain. To determine the maximum gain, both the gate capacitance and the bias current of the SET were varied. The graph shows that it will be very difficult to make SET's with voltage gain greater than one that operate at room temperature. It will be even harder to get them to operate in a dense integrated circuit, which usually has a temperature of about 400 K. For room temperature voltage gain, the junction capacitance will have to be about 0.1 aF with a gate capacitance of 0.3 aF. This kind of SET has not yet been fabricated. So far, the largest voltage gain that has been observed is 5.2 and that was measured at 100 mK. [12] The highest temperature

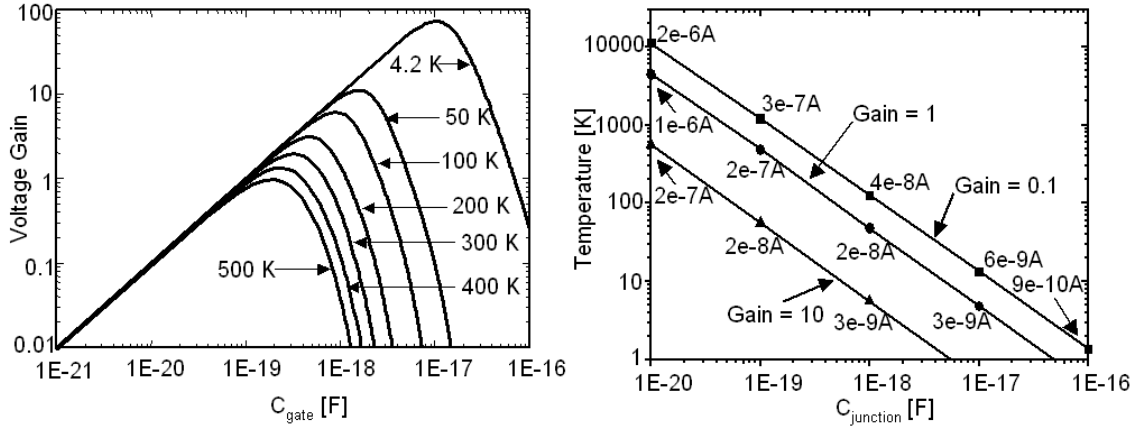

Fig. 3(a) The voltage gain is plotted as a function of the gate capacitance and temperature for a junction capacitance of 0.1 aF. The voltage gain depends on the bias current. The bias current was adjusted to achieve maximum gain. The bias currents that were used were I = 1 nA at 4.2 K, I = 20 nA at 50 K, I = 50 nA at 100 K, I = 100 nA at 200 K, I = 200 nA at 300 K, I = 200 nA at 400 K, I = 300 nA at 500 K. (b) The maximum voltage gain possible for a given junction capacitance is plotted as a function of temperature. The currents which resulted in the maximum gain are given in the plot.

where voltage gain greater than one was observed is 27 K. [3] While voltage gain at room temperature seems difficult, a voltage gain of 10 would be possible at 77 K, a voltage gain of 100 should be possible at 4.2 K, and a voltage gain of 1000 should be possible at 100 mK. The low temperature SET's could be useful for sensitive low temperature measurements.

Some of the circuit architectures that have been proposed for single-electron transistors are basically copies of the semiconducting architectures and require SET's with voltage gain. [13] Because of the limited gain of room temperature SET's, it now seems unlikely that dense integrated circuits based on these principles will ever be made. However, a transistor does not necessarily have to exhibit voltage gain to be useful. For single-electron transistors it is more relevant to consider the charge gain. The charge gain is the modulation of the charge that passes through the SET divided by the change in charge on the gate. This is a frequency dependent quantity. By waiting long enough, it is always possible to transport more charge through the SET than was added to the gate. Charge gain greater than one can easily be achieved at room temperature. The charge gain is maximum at low bias voltages and low temperatures where it is $g_{\text{charge}} = (dI/dV_{g1})/(2\pi f C_{\text{g}}) = 1/(2\pi f R C_{\Sigma})$. Here f is the frequency at which the charge is modulated and R is the lower of the two junction resistances. This result can be derived from Eq. 4.

Charge gain would be used in situations where charge needs to be measured, for instance to readout a memory cell or to readout a charge coupled device. The speed of the charge readout would be limited by the RC-delay formed by the resistance of the SET and the capacitance at the output of the SET. This capacitance depends on the parasitic capacitance of the wire at the output of the SET and the input capacitance of any devices connected to the SET. The parasitic capacitance of a wire is approximately 100 aF/μm. The large output impedance of a SET of at least 100 kΩ makes the SET an intrinsically slow device. To speed up the charge measurement, conventional field-effect transistors (FET's) should be placed as close as possible to the SET. The field-effect transistor can then buffer the high output impedance of the SET. Using both SET's and FET's in a circuit is a retreat from the idea that small SET's will someday replace FET's entirely. However, it now seems unlikely that SET's could ever replace FET's. Perhaps twenty different logic schemes that utilize single-electron transistors exclusively have been proposed but none is widely accepted as being practical. Until a practical scheme in developed, the best way to proceed is to use SET's only as sensitive charge sensors and perform all other functions with conventional FET's.

The background charge problem is another important issue that is inhibiting the widespread use of SET's. The origin of the background charge problem is the extreme charge sensitivity of SET's. A single charged vacancy or an interstitial ion in the oxide near a SET can be enough to switch the transistor from the being conducting to being nonconducting. The same kinds of charged defects are present and move in field-effect transistors but most field-effect transistors are not as sensitive to charge so the consequences of these background charges are not as great. The only effective way to compensate for this problem is to use field-effect transistors to tune the background charges away. One circuit that accomplishes this is the charge-locked loop shown in Fig. 4(a). A charge-locked loop uses feedback to keep the charge on the island of a SET constant. This improves the speed, the linearity and the dynamic range of the charge measurements.

The three problems of low gain, high output impedance, and sensitivity to background can all be remedied by combining SET's with FET's. In such hybrid

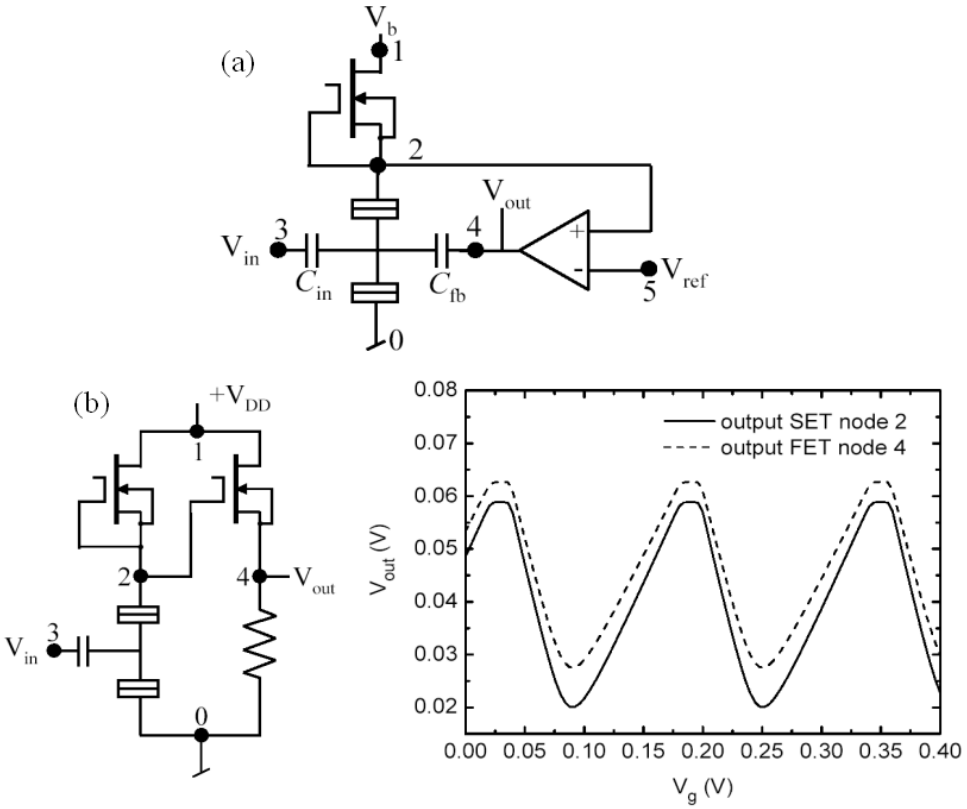

Fig. 4. (a) A charged lock loop that automatically tunes away the background charge. Provided that the amplifier has enough gain, the voltage gain in this circuit is set by the ratio of the input and output capacitors C_{in}/C_{out}. The linearity and the dynamic range of the charge measurement are also improved by the charge-locked loop. The FET is used to current bias the SET. (b) The schematic of a current biased SET with a FET output stage and the corresponding SPICE simulation. The solid line is the voltage at the output voltage of the SET stage (node 2), and the dashed line is the voltage at the output of the FET stage (node 4). A voltage of 0.4 V has been subtracted from the voltage at node 4 to remove a dc offset. The SPICE source code for simulating the circuits shown can be found at http://qt.tn.tudelft.nl/research/set/spice/.

circuits, the SET's provide the charge sensitivity while the FET's provide the gain and the low output impedance. In order to design SET/FET circuits, it is important to have a simulation package that will model both SET's and FET's. The simulation package SPICE is one of the few packages that will do this. [14] Figure 4(b) shows a single-electron transistor that is current biased by a FET and the corresponding SPICE simulation of the circuit. A second FET is used to buffer the output of the SET which increases the speed of the circuit.

5. Conclusions

Single-electron transistors are the most sensitive charge-measuring devices presently available. They have become an important tool in the field of fundamental measurements. The fact that most SET's only perform at low temperature is not seen as a disadvantage for fundamental measurements because these measurements are often performed at low temperature anyway to reduce noise. In fact, very low temperature operation (less than 100 mK) is seen as an advantage because many semiconducting

devices don't work in this temperature range. However for mass-market applications, room temperature operation is necessary. The SET's that operate at room temperature have the problems of low gain, high output impedance, and background charges. No room temperature SET logic or memory scheme is now widely accepted as being practical. The most promising room temperature applications for SET's are in charge sensing circuits where the problems of low gain, high output impedance, and background charges can be solved by integrating SET's with field-effect transistors.

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