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Few-Electron Quantum Dots in Nanowires

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ABSTRACT

We demonstrate transport spectroscopy on bottom-up grown few-electron quantum dots in semiconductor nanowires. The dots are defined by InP double barrier heterostructures in InAs nanowires catalytically grown from nanoparticles. By changing the dot size, we can design devices ranging from single-electron transistors to few-electron quantum dots. In the latter case, electrons can be added one by one to the dots from 0 to ∼50 electrons while maintaining an almost constant charging energy, with addition spectra of the devices displaying shell structures as a result of spin and orbital degeneracies. The reduced dimensionality of the nanowire emitter gives rise to pronounced resonant tunneling peaks, where a gate can be used to control the peak positions.

Semiconductor nanowires have attracted considerable attention due to the possibilities of large-scale fabrication of nanometer-sized systems with controllable electronic and optical properties. Here we demonstrate a unique control of nanowire growth, allowing design of strongly confined quantum mechanical systems inside nanowires. From basic atomic physics it is known that quantum systems with symmetric confinement have a shell structure of the energy levels due to spin and orbital degeneracies. In electrical transport measurements this phenomenon has until now only been demonstrated in top-down fabricated semiconductor quantum dots, also called artificial atoms,[1,2] envisaged to be crucial elements in for example quantum computing.[3] However, the top-down approach requires intricate processing to obtain such devices, which in the past few years has led to rapid advances in alternative bottom-up approaches to produce low-dimensional systems. One important example is one-dimensional nanowires, which have mainly been directed at demonstrating downscaling of bulk devices, such as pn-junctions[4,5] and field-effect transistors.[6] Here we take advantage of the reduced dimensionality of the system to fabricate designed heterostructure few-electron quantum dots within the nanowires, where the lateral confinement generates a shell structure. By growing one-dimensional heterostructures, strain relaxation is very efficient and the conventional requirements of lattice matching are circumvented, thereby offering increased possibilities for band gap engineering and silicon integration. Moreover, bottom-up fabrication of nanowires offers a possibility of creating branched structures,[7] which is an important step for enabling more complex electronics and nanowire networks.

The base material for the heterostructure nanowires reported here is InAs, which is a very promising material for nanowires since it is not hampered by surface depletion problems. This important property in combination with a very low electron effective mass makes InAs an interesting material for various kinds of quantum devices. The InAs/InP nanowires reported here were grown by chemical beam epitaxy (CBE)[8] and seeded by Au nanoparticles. In our case the nanoparticles are deposited on ⟨111⟩ B InAs substrates, and the resulting wires grow epitaxially from the substrate in the ⟨111⟩ or the ⟨001⟩ direction. Hence the cross sections are hexagonal or square with surfaces defined by crystal facets. The diameter of the wires is determined by the size of the deposited Au particles and falls in the range of 50 to 60 nm. Growth can also be nucleated from ordered arrays of Au particles defined by, for instance, electron beam lithography (EBL)[9] or nanoimprint lithography.[10] Figure 1a shows an example of InAs nanowires grown by CBE from gold catalysts defined by EBL. Such nanowire arrays are almost free of defects and the wires maintain their defined position. The heterostructure nanowires reported here were, however, all grown from randomly deposited nanoparticles and contain an InP double barrier structure. We show devices with InAs dot lengths of 100, 30, and 10 nm (Figure 1, b and c). The InP barriers are nominally 5 nm wide but vary somewhat with diameter; a larger diameter results in thinner barriers and vice versa. Electrical measurements on InAs

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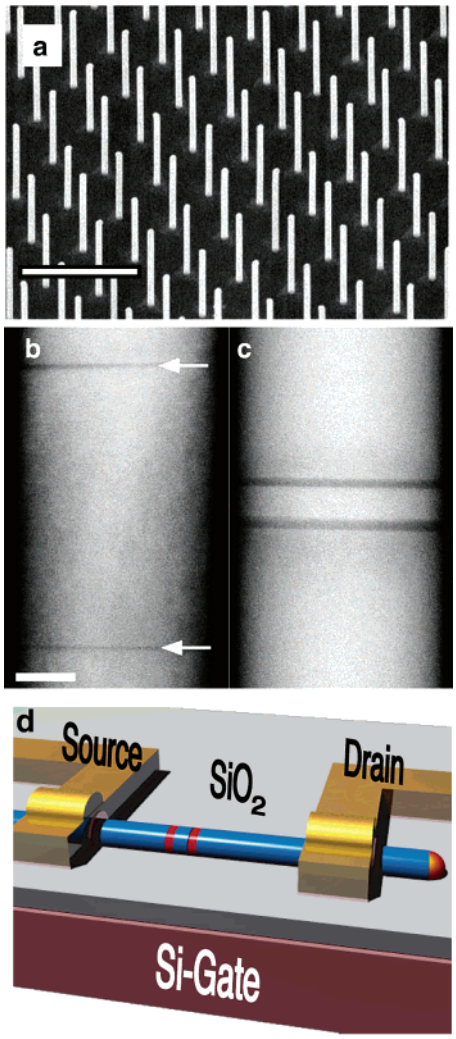

Figure 1. Characterization and processing of nanowires. (a) Scanning electron micrograph of homogeneous InAs nanowires grown on an InAs substrate from lithographically defined arrays of Au particles. The image demonstrates the ability of the CBE to produce identical nanowire devices. The scale bar corresponds to 1 μm. (b) Dark-field scanning transmission electron microscopy image of a nanowire with a 100 nm long InAs quantum dot between two very thin InP barriers. Scale bar depicts 20 nm. (c) Corresponding image of a 10 nm long InAs dot. The InP barrier thickness is 3 and 3.7 nm, respectively. (d) The heterostructured wires are deposited on a SiO_2-capped Si substrate and source and drain contacts are fabricated by lithography.

wires with single InP barriers yields a conduction band offset between InAs and InP of 600 meV[11] and consequently electron transport will be blocked at low temperatures unless the barrier thickness is made sufficiently thin to allow for tunneling.

Electrical contacts to individual wires were established by EBL and metal evaporation on wires transferred to a degenerately doped Si substrate with a 1000 Å SiO_2 cap layer, as is schematically shown in Figure 1d. The contacts to InAs nanowires are Ohmic down to at least 200 mK with a conductance of more than $2e^2/h$ for wires with diameters above 40 nm. The conductance is n-type and can be tuned by the nonlocal Si backgate over several orders of magnitude. Typically, wires above 40 nm in diameter are pinched off at a gate voltage of -2 V or less.

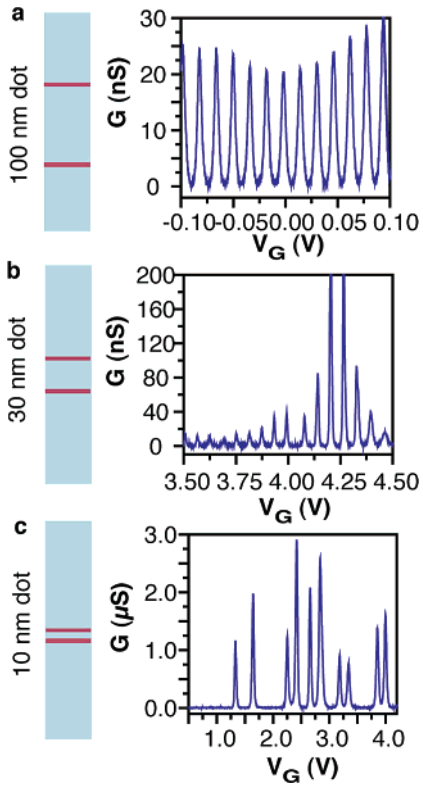

Figure 2. Effect of reduced quantum dot length. (a) Gate characteristics of a SET with a 100 nm long dot. The oscillations are perfectly periodic and are visible up to 12 K. (b) When the dot length is 30 nm, the level spacing at the Fermi energy is comparable to the charging energy and the Coulomb oscillations are no longer completely periodic. (c) A 10 nm dot results in a device depleted of electrons at zero gate voltage. By increasing the electrostatic potential electrons are added one by one. For some electron configurations the addition energy is larger corresponding to filled electron shells. All data in this figure were recorded at 4.2 K.

Devices with a quantum dot length of 100 nm show single-electron charging below 12 K[12] with perfectly periodic gate oscillations, as shown in Figure 2a. The gate voltage spacing of the current peaks is proportional to the addition energy of the dot, which in the constant interaction (CI) model[13] is $E_{ADD}(N) = E_c + \Delta E(N)$. Here the charging energy E_c is the electrostatic energy required for adding one electron to the dot, and $\Delta E(N)$ is the difference in the single-particle energies for N and $N-1$ electrons on the dot. The charging energy of the 100 nm dots is around 5 meV, which is much larger than the average energy level spacing, $\Delta E \ll 1$ meV at the Fermi level, and thus the current peaks are periodic in gate voltage (Figure 2a). However, these dots cannot be completely depleted of electrons before the emitter or collector is pinched off.

For devices with 30 nm dots, the confinement in the growth direction becomes stronger than the lateral confinement. The periodicity of the gate oscillations is broken since $\Delta E \sim 2-3$ meV is comparable to E_c near the Fermi level, and $E_{ADD}(N)$ will vary with N. As seen in Figure 2b, the peak heights vary considerably with gate voltage, as expected for tunneling via single quantum states. Still, the dots cannot be depleted of electrons without also pinching off the emitter or collector.

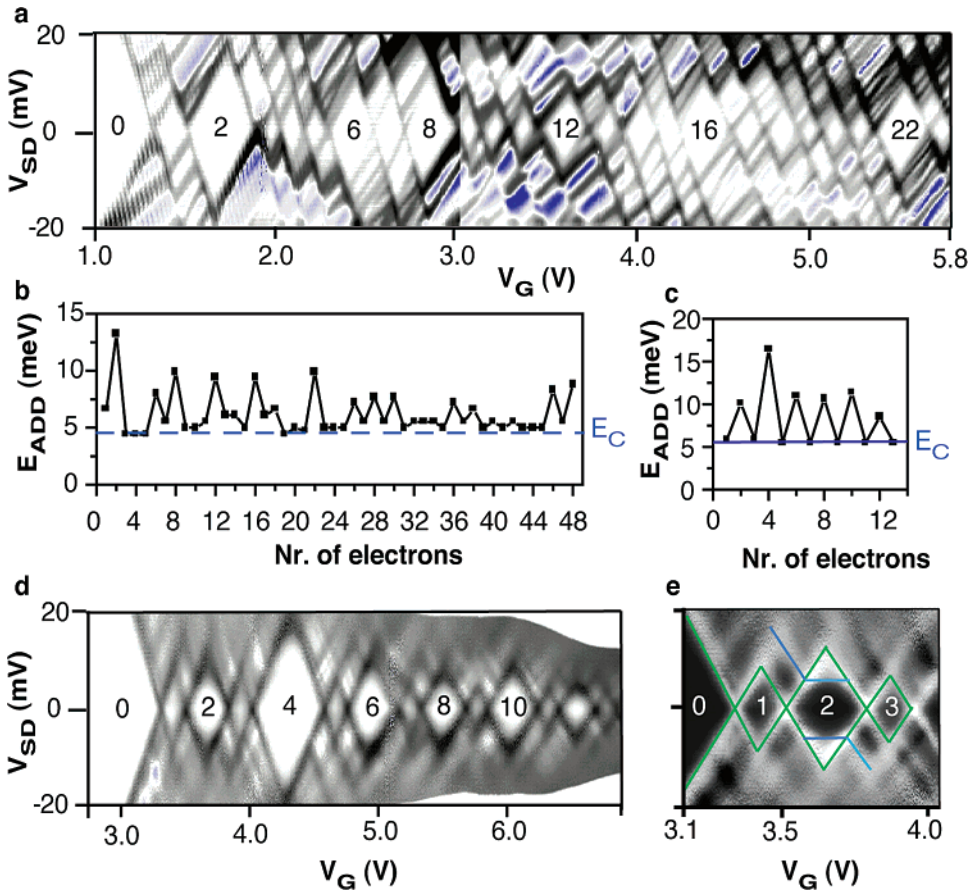

Figure 3. Transport characteristics of few-electron quantum dots. (a) Conductance dI/dV as a function of bias and gate voltage. The "magic" numbers signifying a shell structure are explicitly shown inside the corresponding large Coulomb diamonds. We interpret the saw-tooth pattern superimposed on the first few diamonds to be an effect of an accumulation layer before the barrier. This behavior is only observed in a small fraction of the studied devices. (b) Addition spectrum of the device in (A). The charging energy E_C appears almost constant for all gate voltages. (c) Addition energy of a device displaying an even−odd shell structure. (d) The stability diagram of the device in (C) shows similar behavior to (A) but with less negative differential conductance. The even electron number Coulomb diamonds are truncated due to co-tunneling, which is seen clearer in (e). The onset of co-tunneling coincides with the first-order tunneling through the first excited state. The white regions in the upper and lower parts of (E) at high gate voltages are due to overload in the current amplifier. All data in this figure were recorded at 4.2 K.

For wires with a quantum dot length of 10 nm, the dots are completely emptied of carriers at $V_g = 0$ V, where the emitter and collector are far from pinch off (Figure 2c). This is a result of the strong quantum confinement in the growth direction of the system where the ground state is considerably pushed up in energy compared to the corresponding emitter and collector states. The mean level spacing ($\Delta E \sim 10$ meV) is now larger than the charging energy due to the small number of electrons on the dot, and the addition energy reaches values up to 30 meV for some devices. By increasing the gate voltage, electrons are added to the dot one by one up to as many as 50 before the barrier transmission probability becomes too large. Conductance peaks are visible up to roughly 60 K before they are thermally smeared out. The peak width scales linearly with temperature and the peak height increases as the temperature is decreased in agreement with tunneling through discrete states.

The charging energy of the devices is given by the total capacitance of the system, $E_c = e^2/C_\Sigma$ and is almost constant for all island lengths studied, ranging from 4 to 6 meV. The diameter of a wire seems to be the important factor causing the spread in values, where the source and drain capacitances, C_S and C_D, are the dominating terms (∼30 aF in total). The gate capacitance, C_g, is observed to scale linearly with island length from 10 aF down to 1 aF.

Figure 3a shows dI/dV as a function of gate voltage and source−drain voltage for a nanowire with a 10 nm long dot. Darker color here indicates a higher dI/dV, the blue color a negative dI/dV, whereas the white diamond-shaped areas correspond to Coulomb blockade of the current through the device. Some of the diamonds are considerably larger, reflecting larger addition energies. The larger diamonds correspond to an electron number of 2, 6, 8, 12, 16, and 22. In Figure 3b the addition energies required for adding up to 48 electrons to the dot is displayed. Aside from the first diamond occasionally being larger than other odd-electron diamonds,[14] a very uniform size of the odd-electron diamonds is observed. According to the CI model the odd-electron diamonds have $\Delta E(N) = 0$ due to the spin degeneracy, and therefore $E_{ADD} = E_C$. The fact that E_C is not affected by the gate voltage indicates a rigid confinement potential for the carriers and contrasts earlier studies of few-electron quantum dots.[1,2] We believe this is explained by the lack of surface depletion in InAs.

The energy level structure of a quantum system with symmetric confinement will exhibit a shell structure. The magic numbers (2, 6, 8, 12, 16) observed above are the same as for a 2D dot with square hard-wall confinement, where it is estimated that the second mode in the growth direction is not populated until $N \sim 30$. A square cross-section of the dot is possible since also ⟨001⟩ wires appear in the growth, although less frequently than ⟨111⟩. In contrast, a ⟨111⟩ wire would have completely filled shells for electron numbers (2, 6, 10, 12, 14, 16, ...)[15] due to the hexagonal cross-section. The fourth diamond is also slightly enlarged, which might be due to exchange interactions, leading to shell filling according to Hund's rule.[1,16] We have performed measurements on several devices and always observed enlarged addition energies for electron numbers (2, 6, 8). However sometimes other diamonds (4, 10, ...) are unusually large as well. We interpret these observations as a lifting of the orbital degeneracies. This could be caused by several factors, e.g., impurities in the dot or on its surface affecting the shape of the confining potential, the large strain (3.4%) near the heterostructure interfaces, which may elongate the dot in one or more directions, or the asymmetric gating of the wires, generating a nonuniform electric field across the structure.

The complete lifting of orbital degeneracies would result in an even−odd sequence of large/small addition energies in the CI model. Figure 3c was obtained from a wire where clear even−odd effects are visible. The wire diameter is in this case slightly larger, and hence has very thin tunnel barriers. For this device the even-electron diamonds are truncated due to inelastic co-tunneling.[17] Between the second and third diamond in Figure 3d, the peak conductance is ~0.5 e^2/h, i.e., a regime where higher order tunneling effects indeed would start to contribute. The onset of co-tunneling coincides with the bias required to observe transport through the first excited state of the even-electron diamonds, see Figure 3e. The energy difference between the ground state and the first excited state for this device is 7 meV, which is consistent with the lateral size of the wire. Additional features resembling excited states can be identified at energies lower than the first excited state. However, they occur at energies too low to be related to the energy spectrum of a 60 nm thick nanowire. These features are even more pronounced in the device of Figure 3a and might be due to disorder-induced interference effects in the emitter.

Negative differential resistance (NDR) is observed as dot states are moved out of resonance with the emitter states. The NDR observed here is due to the one-dimensional character of the emitter yielding a sharply peaked density of states (DOS), and to cross-coupling of modes with different lateral quantum numbers. The interference effect mentioned previously also superimposes small corrections to the DOS that may produce additional NDR. When the gate voltage is chosen such that the dot is empty, the NDR is more pronounced with peak-to-valley ratios around 10:1 and peak current densities as large as 100 A/cm^2. From stability plots (Figure 4a) it is observed that the depletion edge of the dot is linearly shifted with the gate and thus the device acts as a resonant tunneling transistor. A small

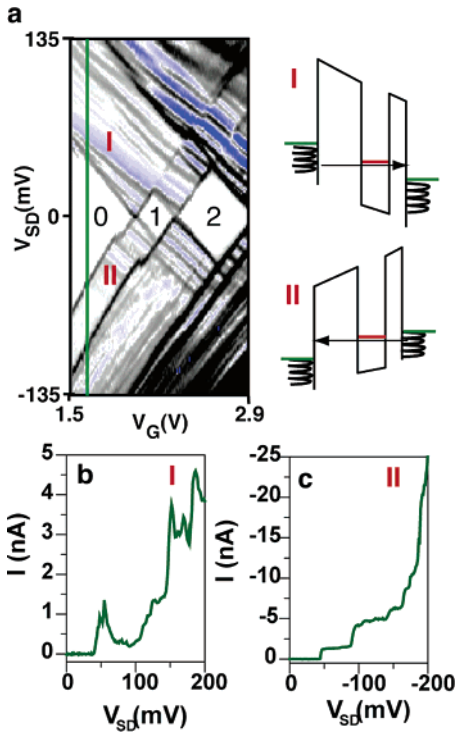

Figure 4. Resonant tunneling and Coulomb blockade. (a) Differential conductance as a function of bias and gate voltage for zero, one, and two electrons on the dot for large bias voltages at 300 mK. The green line indicates the $I-V$ curves shown in (B) and (C). (b) For positive bias voltages (insert I) tunneling occurs to the dot via the thicker barrier and electrons then escape quickly to the collector. Hence, charging effects are weak. Resonances in the transport characteristics (black lines) appear when emitter states are aligned with discrete states in the dot. (c) For negative bias voltages (insert II) electrons tunnel quickly to the dot through the thin barrier, whereas the tunneling rate out of the dot is lower, resulting in charging effects, i.e., a Coulomb staircase.

asymmetry of the two tunnel barriers[18] gives rise to charging effects in the bias direction where electrons tunnel through the thin barrier first, as displayed in Figure 4c. The other bias direction, where the peaked DOS of the emitter is probing the dot states, shows NDR, Figure 4b.

In conclusion, we have presented bottom-up fabrication of few-electron quantum dots in one-dimensional nanowires. Due to the strong nanowire heterostructure confinement, the dots are depleted from electrons unless a positive voltage is applied to the gate. Upon filling, the devices display a shell structure as a result of spin and orbital degeneracies. Combined with the possibilities for parallel production, integration with silicon, and branching, this family of devices becomes a strong candidate for applications. Specifically, we have shown that the unique freedom for band gap engineering in nanowires opens avenues for novel device designs.

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