



EMV®

Level 1 Specifications for Payment Systems

EMV Contactless Interface Specification

Version 3.1
December 2020

Legal Notice

The EMV® Specifications are provided “AS IS” without warranties of any kind, and EMVCo neither assumes nor accepts any liability for any errors or omissions contained in these Specifications. EMVCO DISCLAIMS ALL REPRESENTATIONS AND WARRANTIES, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE AND NON-INFRINGEMENT, AS TO THESE SPECIFICATIONS.

EMVCo makes no representations or warranties with respect to intellectual property rights of any third parties in or in relation to the Specifications. EMVCo undertakes no responsibility to determine whether any implementation of the EMV® Specifications may violate, infringe, or otherwise exercise the patent, copyright, trademark, trade secret, know-how, or other intellectual property rights of third parties, and thus any person who implements any part of the EMV® Specifications should consult an intellectual property attorney before any such implementation.

Without limiting the foregoing, the Specifications may provide for the use of public key encryption and other technology, which may be the subject matter of patents in several countries. Any party seeking to implement these Specifications is solely responsible for determining whether its activities require a license to any such technology, including for patents on public key encryption technology. EMVCo shall not be liable under any theory for any party’s infringement of any intellectual property rights in connection with the EMV® Specifications.

Revision Log – Version 3.1

The following changes have been made since the publication of Version 3.0. Some of the numbering and cross references in this version have been updated to reflect changes introduced by the published bulletins. The numbering of existing requirements did not change, unless explicitly stated otherwise.

Incorporated changes described in the following Specification Updates:

- Specification Bulletin No. 212: Timing Requirements for Time-out Handling
- Specification Bulletin No. 215: Polling Collision Indication
- Specification Bulletin No. 232: Type B Minimum Modulation Index
- Specification Bulletin No. 233: Update to Polling Collision Indication (SB215)
- Specification Bulletin No. 235: Contactless – EMD Immunity for Type A EoS
- Specification Bulletin No. 245: Contactless – IQ Modulation
- Specification Bulletin No. 252: Chaining Invocation & Block Size

Other editorial changes:

- Updated Figure 3.1 to include t_5 .
- Additional editorial fixes not included in SB245 in note immediately following Figure 3.4.
- Editorial fix in first sentence of section 9.4: replaced PICC with PCD.

Contents

EMV Contactless Interface Specification	i
Revision Log – Version 3.1	iii
Contents	v
Figures.....	x
Tables	xii
Requirements	xv
1 General 1	
1.1 Scope and Audience	1
1.2 Related Information.....	1
1.3 Normative References.....	2
1.4 Acknowledgment.....	2
1.5 Definitions	3
1.6 Notational Conventions	6
1.6.1 Abbreviations.....	6
1.6.2 Notations	9
1.6.3 Terminology and Conventions	10
1.6.4 Reserved for Future Use (RFU).....	11
2 Introduction.....	13
2.1 Contactless System	13
2.2 EMV Contactless Level 1 Test Equipment.....	14
2.2.1 EMV – TEST PCD	15
2.2.2 EMV – TEST CMR.....	16
2.2.3 EMV – TEST PICCs	17
2.2.4 IQ Demodulation Test Equipment.....	19
2.3 Landing Plane	20
2.4 Operating Volume	20
2.5 Overview	22
3 Radio Frequency Power and Signal Interface.....	25
3.1 Introduction	25
3.1.1 Transmission and Reception Requirements	25
3.1.2 EMV Contactless Level 1 Test Equipment.....	26
3.1.3 ‘Function Properly’	27
3.1.4 Temperature and Humidity	27
3.1.5 Summary	28

3.2	RF Power	29
3.2.1	PCD Requirements for Power Transfer PCD to PICC	30
3.2.2	PICC Requirements for Power Transfer PCD to PICC	31
3.2.3	Influence of the PICC on the Operating Field	34
3.2.4	PCD Requirement for the Carrier Frequency f_c	36
3.2.5	PICC Requirement for the Carrier Frequency $f_{S,c}$	37
3.2.6	PCD Requirements for Resetting the Operating Field	40
3.2.7	PICC Requirements for Power-off	41
3.2.8	PICC Requirements for Power-on	45
3.2.9	PCD Requirements for Power-off of the Operating Field	46
3.3	Signal Interface PCD to PICC	47
3.3.1	Introduction	47
3.3.2	PCD Requirements for Modulation PCD to PICC – Type A	48
3.3.3	PICC Requirements for Modulation PCD to PICC – Type A	51
3.3.4	PCD Requirements for Modulation PCD to PICC – Type B	53
3.3.5	PICC Requirements for Modulation PCD to PICC – Type B	56
3.4	Signal Interface PICC to PCD	58
3.4.1	Introduction	58
3.4.2	PICC Requirements for Load Modulation	60
3.4.3	PICC Requirements for Subcarrier Modulation – Type A	62
3.4.4	PICC Requirements for Subcarrier Modulation – Type B	63
3.4.5	PCD Requirements for Modulation PICC to PCD	64
3.5	IQ Demodulation	66
3.5.1	Introduction	66
3.5.2	PCD Requirements for IQ Demodulation	66
4	Sequences and Frames	69
4.1	Introduction	69
4.1.1	Sequence	69
4.1.2	Frames	69
4.1.3	Coding Schemes	71
4.2	Bit Rate	73
4.3	Synchronization	74
4.3.1	Type A – Synchronization	74
4.3.2	Type B – Synchronization	74
4.4	Bit Coding	78
4.4.1	Bit Coding PCD → PICC – Type A	78
4.4.2	Bit Coding PICC → PCD – Type A	80
4.4.3	Bit Coding PCD → PICC – Type B	82

4.4.4	Bit Coding PICC → PCD – Type B	83
4.5	Symbol Synchronization.....	85
4.6	De-synchronization	87
4.6.1	Type A – De-synchronization.....	87
4.6.2	Type B – De-synchronization.....	88
4.7	Frames.....	90
4.7.1	Type A – Frame Format.....	90
4.7.2	Type B – Frame Format.....	92
4.7.3	FSD (Frame Size for proximity coupling Device).....	93
4.7.4	FSC (Frame Size for proximity Card).....	94
4.8	Timing Requirements	95
4.8.1	Frame Delay Time PCD → PICC.....	95
4.8.2	Frame Delay Time PICC → PCD	110
4.8.3	Summary	119
4.9	EMD Handling	120
4.9.1	$t_{nn,min}$	120
4.9.2	PCD EMD Handling	123
5	Type A – Commands and Responses	125
5.1	Type A – Command Set	125
5.2	Type A – CRC_A.....	127
5.3	WUPA and REQA	128
5.3.1	WUPA and REQA Command	128
5.3.2	WUPA and REQA Response (ATQA).....	128
5.4	ANTICOLLISION.....	131
5.4.1	ANTICOLLISION Command	131
5.4.2	ANTICOLLISION Response (UID CLn).....	132
5.5	SELECT	133
5.5.1	SELECT Command	133
5.5.2	Response – Select Acknowledge – SAK.....	134
5.6	HLTA.....	135
5.6.1	HLTA Command	135
5.6.2	HLTA Response	135
5.7	Request for Answer to Select (RATS).....	136
5.7.1	RATS Command	136
5.7.2	RATS Response (Answer To Select).....	138
5.8	Protocol Parameter Selection (PPS)	146
5.8.1	PPS Command.....	146

5.8.2 PPS Response	148
6 Type B – Commands and Responses	151
6.1 Type B – Command Set	151
6.2 Type B – CRC_B	152
6.3 WUPB and REQB	153
6.3.1 WUPB and REQB Command	153
6.3.2 WUPB and REQB Response (ATQB)	156
6.4 ATTRIB	164
6.4.1 ATTRIB Command	164
6.4.2 ATTRIB Response	172
6.5 HLTB	174
6.5.1 HLTB Command	174
6.5.2 HLTB Response	174
7 Type A – PICC State Machine	175
7.1 State Diagram	175
7.2 Type A PICC States	178
7.2.1 POWER-OFF State	178
7.2.2 IDLE State	178
7.2.3 READY and READY* States	179
7.2.4 READY' and READY'* States	180
7.2.5 READY" and READY"** States	181
7.2.6 ACTIVE and ACTIVE* States	182
7.2.7 PROTOCOL State	183
7.2.8 HALT State	184
8 Type B – PICC State Machine	185
8.1 State Diagram	185
8.2 Type B PICC States	188
8.2.1 POWER-OFF State	188
8.2.2 IDLE State	188
8.2.3 READY State	189
8.2.4 ACTIVE State	190
8.2.5 HALT State	190
9 PCD Processing	191
9.1 Main Loop	191
9.1.1 Main Loop – Informative	191
9.1.2 Main Loop – Normative	193

9.2	Polling	194
9.3	Collision Detection	199
9.3.1	General Collision Detection	200
9.3.2	Type A Collision Detection.....	201
9.3.3	Type B Collision Detection.....	208
9.4	Activation	210
9.4.1	Type A Activation.....	210
9.4.2	Type B Activation.....	210
9.5	Removal.....	211
9.6	Exception Processing.....	214
10	Half-Duplex Block Transmission Protocol	217
10.1	Block Format.....	217
10.1.1	Block Length.....	218
10.1.2	Prologue Field	218
10.1.3	Information Field.....	221
10.1.4	Epilogue field	221
10.1.5	Protocol Error	221
10.2	Frame Waiting Time Extension	222
10.2.1	Power Level Indicator	222
10.2.2	WTXM	223
10.3	Protocol Operation	226
10.3.1	General Rules.....	226
10.3.2	Chaining	226
10.3.3	Block Numbering Rules	230
10.3.4	Block Handling Rules.....	231
10.3.5	Exception Processing	233
10.3.6	DESELECT Processing	237
Annex A	Values	239
A.1	Operating Volume	239
A.2	RF Power and Signal Interface.....	240
A.3	Set-up Values for Test Equipment.....	243
A.4	Sequences and Frames	244
A.5	PCD Processing.....	245
A.6	Protocol Operation	245
Annex B	Position Conventions	247

Figures

Figure 2.1: PCD and PICC Configuration.....	13
Figure 2.2: EMV – TEST PCD	15
Figure 2.3: EMV – TEST CMR.....	16
Figure 2.4: EMV – TEST PICC 1	18
Figure 2.5: EMV – TEST PICC 3	18
Figure 2.6: Operating Volume	21
Figure 2.7: Communication Protocol Layers	22
Figure 3.1: Lower Level – Type A	50
Figure 3.2: Modulation PCD to PICC – Type B	55
Figure 3.3: Load Modulation	58
Figure 3.4: BPSK	59
Figure 3.5: Start of Subcarrier Modulation – Type A	62
Figure 3.6: Allowed Phase Shifts – Type B	63
Figure 4.1: Frame Format for Type A and Type B.....	70
Figure 4.2: On-Off-Keying.....	71
Figure 4.3: Coding Schemes.....	71
Figure 4.4: PICC Start of Sequence.....	74
Figure 4.5: PCD Start of Sequence.....	75
Figure 4.6: Modified Miller Coding with ASK 100%	78
Figure 4.7: Manchester Coding with OOK.....	80
Figure 4.8: NRZ-L Coding with ASK 10%.....	82
Figure 4.9: NRZ-L Coding with BPSK	83
Figure 4.10: Short Frame.....	90
Figure 4.11: Standard Frame	90
Figure 4.12: Type B Character Format.....	92
Figure 4.13: Type B – Frame Format.....	92
Figure 4.14: FDT _{A,PICC}	96
Figure 4.15: End of PCD Command – Type A	97
Figure 4.16: Start of PICC Response (Positive Modulation) – Type A.....	98
Figure 4.17: Start of PICC Response (Negative Modulation) – Type A	98
Figure 4.18: Start of PICC Response (Example of mixed modulation starting with a positive part cycle) – Type A	99
Figure 4.19: FDT _{B,PICC}	101
Figure 4.20: End of PCD Command – Type B	101
Figure 4.21: Start of PICC Response (Extended Low Phase Change) – Type B	102
Figure 4.22: Start of PICC Response (Extended High Phase Change) – Type B	103
Figure 4.23: Start of Unmodulated Subcarrier of PICC Response (Positive Modulation)	107
Figure 4.24: Start of Unmodulated Subcarrier of PICC Response (Negative Modulation)	107

Figure 4.25: Start of Unmodulated Subcarrier of PICC Response (Example of Mixed Modulation Starting with Positive Part Cycle)	108
Figure 4.26: FDT _{A,PCD}	110
Figure 4.27: End of PICC Response (Positive Modulation) – Type A.....	111
Figure 4.28: End of PICC Response (Negative Modulation) – Type A	111
Figure 4.29: End of PICC Response (Example of mixed modulation ending with a negative part cycle) – Type A	112
Figure 4.30: Start of PCD Command – Type A	112
Figure 4.31: FDT _{B,PCD}	113
Figure 4.32: End of PICC Response (Extended Low Phase Change) – Type B	114
Figure 4.33: End of PICC Response (Extended High Phase Change) – Type B ...	114
Figure 4.34: Start of PCD Command – Type B	115
Figure 4.35: t _{nn,min} for Type A	120
Figure 4.36: t _{nn,min} for Type B	121
Figure 5.1: Position of CRC_A within a Standard Frame.....	127
Figure 6.1: Position of a CRC_B within a Frame	152
Figure 7.1: PICC Type A State Diagram	177
Figure 8.1: PICC Type B State Diagram	187
Figure 9.1: Terminal Main Loop	192
Figure 9.2: Polling.....	195
Figure 9.3: Type A Collision Detection.....	207
Figure 9.4: Type B Collision Detection.....	209
Figure 9.5: Removal of PICC of Type A and PICC of Type B.....	213
Figure 10.1: Block Format.....	217
Figure 10.2: Chaining	229

Tables

Table 1.1: Abbreviations	6
Table 1.2: Notations.....	9
Table 3.1: Configurations Transmit and Receive.....	25
Table 3.2: Measurement of Power Transfer PCD to PICC (PCD Transmission)	30
Table 3.3: Measurement of Power Transfer PCD to PICC (PICC Reception) – Type A	31
Table 3.4: Measurement of Power Transfer PCD to PICC (PICC Reception) – Type B	31
Table 3.5: Measurement of the Influence of the PICC on the Operating Field.....	34
Table 3.6: Measurement of Carrier Frequency f_c (PCD Transmission).....	36
Table 3.7: Measurement of Carrier Frequency $f_{S,c}$ (PICC Reception) – Type A.....	37
Table 3.8: Measurement of Carrier Frequency $f_{S,c}$ (PICC Reception) – Type B.....	38
Table 3.9: Measurement of Resetting the Operating Field	40
Table 3.10: Measurement of PICC Power-off – Type A.....	41
Table 3.11: Measurement of PICC Power-off – Type B.....	42
Table 3.12: Measurement of PICC Power-on.....	45
Table 3.13: Measurement of Power-off of the Operating Field	46
Table 3.14: Measurement of Modulation PCD to PICC – Type A (PCD Transmission)	48
Table 3.15: Measurement of Modulation PCD to PICC – Type A (PICC Reception)	51
Table 3.16: Measurement of Modulation PCD to PICC – Type B (PCD Transmission).....	53
Table 3.17: Measurement of PCD to PICC Modulation – Type B (PICC Reception)	56
Table 3.18: Measurement of Load Modulation Characteristics (PICC Transmission)	60
Table 3.19: Measurement of Modulation PICC to PCD (PCD Reception)	64
Table 3.20: Measurement of IQ Modulation PICC to PCD (PCD Reception).....	66
Table 4.1: Overview of Coding Schemes	72
Table 4.2: $FDT_{A,PICC}$ and Logic Value of Last Bit before EoF	99
Table 4.3: $FDT_{A,PICC}$ and Command Type	99
Table 4.4: Type A – Timings	119
Table 4.5: Type B – Timings	119
Table 5.1: Type A – Command Set.....	125
Table 5.2: Coding of WUPA and REQA within a Short Frame.....	128
Table 5.3: Byte 1 of ATQA	128
Table 5.4: Byte 2 of ATQA	129
Table 5.5: Coding of ANTICOLLISION Command	131
Table 5.6: Coding of SEL.....	131
Table 5.7: UID CLn	132
Table 5.8: Coding of SELECT Command	133
Table 5.9: Coding of SEL.....	133

Table 5.10: Coding of SAK	134
Table 5.11: Coding of HLTA Command	135
Table 5.12: Coding of RATS Command	136
Table 5.13: Format of RATS Parameter Byte (PARAM).....	136
Table 5.14: FSDI to FSD Conversion.....	136
Table 5.15: Structure of the ATS.....	138
Table 5.16: Coding of Format Byte T0	139
Table 5.17: FSCI to FSC Conversion.....	139
Table 5.18: Coding of Interface Byte TA(1).....	141
Table 5.19: Coding of Interface Byte TB(1).....	143
Table 5.20: Coding of Interface Byte TC(1).....	144
Table 5.21: Coding of PPS Command	146
Table 5.22: Coding of PPSS of the PPS Command	147
Table 5.23: Coding of PPS0	147
Table 5.24: Coding of PPS1	147
Table 5.25: Coding of Selected Divisor Integer	148
Table 5.26: Coding of PPS Response.....	148
Table 6.1: Type B – Command Set.....	151
Table 6.2: WUPB and REQB Command Format.....	153
Table 6.3: Coding of PARAM Byte Included in WUPB and REQB Command	154
Table 6.4: ATQB Format.....	156
Table 6.5: Protocol Info Format.....	157
Table 6.6: Bit Rates Supported by the PICC	157
Table 6.7: FSC in Terms of Max_Frame_Size	158
Table 6.8: Protocol_Type.....	159
Table 6.9: Protocol Types Supported by the PICC	159
Table 6.10: Application Data Coding Supported by the PICC	162
Table 6.11: Frame Options Supported by the PICC	162
Table 6.12: ATTRIB Command Format.....	164
Table 6.13: Coding of Param 1 of the ATTRIB Command.....	165
Table 6.14: Coding of Param 2 of the ATTRIB Command.....	166
Table 6.15: FSD in Terms of Max_Frame_Size	166
Table 6.16: Coding of b8 and b7 of Param 2.....	167
Table 6.17: Coding of b6 and b5 of Param 2.....	167
Table 6.18: Coding of Param 3 of the ATTRIB Command.....	168
Table 6.19: Coding of Param 4 of the ATTRIB Command.....	169
Table 6.20: ATTRIB Response Format.....	172
Table 6.21: HLTB Command Format	174
Table 6.22: HLTB Response Format.....	174
Table 10.1: Coding of b8-b7 of PCB	218
Table 10.2: Coding of I-block PCB	219
Table 10.3: Coding of R-block PCB	219

Table 10.4: Coding of S-block PCB.....	220
Table 10.5: Coding of INF Field of an S(WTX) Request.....	222
Table 10.6: Coding of INF Field of an S(WTX) Response	223
Table A.1: Operating Volume.....	239
Table A.2: RF Power and Signal Interface	240
Table A.3: Minimum Value of V_{pp}	242
Table A.4: Set-up Values for EMV Contactless Level 1 Test Equipment.....	243
Table A.5: Sequences and Frames.....	244
Table A.6: PCD Processing	245
Table A.7: Protocol Operation.....	245

Requirements

Requirements 1.1: RFU	11
Requirements 3.1: Power Transfer PCD to PICC (PCD Transmission).....	30
Requirements 3.2: Power Transfer PCD to PICC (PICC Reception).....	33
Requirements 3.3: Influence of the PICC on the Operating Field	35
Requirements 3.4: Carrier Frequency f_c (PCD Transmission)	36
Requirements 3.5: Carrier Frequency $f_{S,c}$ (PICC Reception)	39
Requirements 3.6: Reset Operating Field (PCD Transmission)	40
Requirements 3.7: PICC Power-off.....	44
Requirements 3.8: PICC Power-on.....	45
Requirements 3.9: Power-off of the Operating Field (PCD Transmission).....	46
Requirements 3.10: Modulation PCD to PICC – Type A (PCD Transmission).....	49
Requirements 3.11: Modulation PCD to PICC – Type A (PICC Reception).....	52
Requirements 3.12: Modulation PCD to PICC – Type B (PCD Transmission).....	54
Requirements 3.13: Modulation PCD to PICC – Type B (PICC Reception).....	57
Requirements 3.14: Load Modulation Characteristics (PICC Transmission)	61
Requirements 3.15: Subcarrier Modulation – Type A (PICC Transmission)	62
Requirements 3.16: Subcarrier Modulation – Type B (PICC Transmission)	63
Requirements 3.17: Modulation PICC to PCD (PCD Reception)	65
Requirements 3.18: IQ Modulation PICC to PCD (PCD Reception)	67
Requirements 4.1: Bit Rate.....	73
Requirements 4.2: Synchronization PCD → PICC – Type B	75
Requirements 4.3: Synchronization PICC → PCD – Type B	76
Requirements 4.4: Bit Coding PCD → PICC – Type A.....	79
Requirements 4.5: Loaded State	81
Requirements 4.6: Bit Coding PICC → PCD – Type A.....	81
Requirements 4.7: Bit Coding PCD → PICC – Type B.....	82
Requirements 4.8: Bit Coding PICC → PCD – Type B	84
Requirements 4.9: Type B Character Separation.....	85
Requirements 4.10: Type B Bit Boundaries PCD to PICC.....	85
Requirements 4.11: Type B Bit Boundaries PICC to PCD.....	86
Requirements 4.12: End of Sequence PCD → PICC – Type A	87
Requirements 4.13: End of Sequence PICC → PCD – Type A	87
Requirements 4.14: End of Sequence PCD → PICC – Type B	88
Requirements 4.15: End of Sequence PICC → PCD – Type B	89
Requirements 4.16: Type A – Frame Format.....	91
Requirements 4.17: Type B – Character Format.....	92
Requirements 4.18: FSD	93
Requirements 4.19: FSC	94
Requirements 4.20: FDT _{A,PICC}	100

Requirements 4.21: FDT _{A,PICC,MIN}	100
Requirements 4.22: FDT _{A,PICC} for WUPA, REQA, SELECT, and ANTICOLLISION.....	100
Requirements 4.23: FDT _{B,PICC,MIN}	103
Requirements 4.24: Frame Waiting Time.....	105
Requirements 4.25: Activation Frame Waiting Time	106
Requirements 4.26: FWT _{ATQB} and TR0 _{MAX} for WUPB and REQB Commands.....	109
Requirements 4.27: FDT _{PCD,MIN}	116
Requirements 4.28: SFGT	117
Requirements 4.29: t _{nn,min}	122
Requirements 4.30: PCD EMD Handling	123
Requirements 5.1: Protocol Error – Type A.....	126
Requirements 5.2: CRC_A	127
Requirements 5.3: PCD Handling of ATQA.....	129
Requirements 5.4: UID Length.....	129
Requirements 5.5: Dynamic UID.....	130
Requirements 5.6: PCD Handling of BCC.....	132
Requirements 5.7: Type A PICC Compliance with ISO/IEC 14443-4	134
Requirements 5.8: HLTA Response.....	135
Requirements 5.9: FSDI _{MIN}	136
Requirements 5.10: PICC Handling of RFU values of FSDI.....	137
Requirements 5.11: Support of CID	137
Requirements 5.12: Length Byte TL of the ATS	138
Requirements 5.13: FSCI _{MIN}	139
Requirements 5.14: PCD Handling of RFU values of FSCI.....	139
Requirements 5.15: Format Byte T0 of the ATS.....	140
Requirements 5.16: Format Byte TA(1) of the ATS.....	142
Requirements 5.17: PCD Handling of RFU bit b4 in TA(1).....	142
Requirements 5.18: Interface Byte TB(1) of the ATS	143
Requirements 5.19: Interface Byte TB(1) of the ATS	144
Requirements 5.20: Interface Byte TC(1) of the ATS	145
Requirements 5.21: Historical Bytes of the ATS.....	145
Requirements 5.22: PPS Command	146
Requirements 5.23: PPS1	148
Requirements 5.24: PPS Response.....	148
Requirements 6.1: Protocol Error – Type B.....	151
Requirements 6.2: CRC_B	152
Requirements 6.3: Application Family Indicator (AFI)	153
Requirements 6.4: Number of Slots (N)	154
Requirements 6.5: Support for Extended ATQB.....	155
Requirements 6.6: PUPI in ATQB	156
Requirements 6.7: Application Data Field	156
Requirements 6.8: Bit Rates Supported by the PICC	158

Requirements 6.9: PCD Handling of RFU bit b4 in Bit_Rate_Capability.....	158
Requirements 6.10: FSCI _{MIN}	158
Requirements 6.11: PCD Handling of RFU Values of Max_Frame_Size.....	159
Requirements 6.12: Type B Protocol Type supported by the PICC	160
Requirements 6.13: Minimum TR2.....	161
Requirements 6.14: Maximum Value of FWI for Type B.....	161
Requirements 6.15: Application Data Coding (ADC).....	162
Requirements 6.16: Frame Options (FO).....	162
Requirements 6.17: SFGI	163
Requirements 6.18: PUPI in ATTRIB Command.....	164
Requirements 6.19: Coding of Param 1 of the ATTRIB Command	165
Requirements 6.20: FSDI _{MIN}	166
Requirements 6.21: PICC Handling of RFU values of Max_Frame_Size	166
Requirements 6.22: Setting the Bit Rate for Type B.....	167
Requirements 6.23: Coding and Handling of Param 3 of the ATTRIB Command..	168
Requirements 6.24: Coding of Param 4 of the ATTRIB Command	169
Requirements 6.25: Higher layer – INF	171
Requirements 6.26: CID in ATTRIB Response	172
Requirements 6.27: MBLI in ATTRIB Response	172
Requirements 6.28: Higher layer – Response.....	173
Requirements 7.1: PICC Type A – State Machine	175
Requirements 7.2: Type A – IDLE State	178
Requirements 7.3: Type A – READY and READY* States.....	179
Requirements 7.4: Type A – READY' and READY'' States	180
Requirements 7.5: Type A – READY" and READY"" States	181
Requirements 7.6: Type A – ACTIVE and ACTIVE* States.....	182
Requirements 7.7: Type A – PROTOCOL State	183
Requirements 7.8: Type A – HALT State	184
Requirements 8.1: PICC Type B – State Machine	185
Requirements 8.2: Type B – IDLE State	188
Requirements 8.3: Type B – READY State.....	189
Requirements 8.4: Type B – ACTIVE State	190
Requirements 8.5: Type B – HALT State	190
Requirements 9.1: PCD Requirements Related to the Main Loop.....	193
Requirements 9.2: Polling	196
Requirements 9.3: Collision Detection	200
Requirements 9.4: Type A Collision Detection	201
Requirements 9.5: Type B Collision Detection	208
Requirements 9.6: Type A Activation	210
Requirements 9.7: Type B Activation	210
Requirements 9.8: Removal Procedure for Type A	211
Requirements 9.9: Removal Procedure for Type B	212

Requirements 9.10: Exception Processing.....	214
Requirements 10.1: Coding of S-block PCB	220
Requirements 10.2: Protocol Error.....	221
Requirements 10.3: Power Level Indication	222
Requirements 10.4: RFU Handling of S(WTX) Response	223
Requirements 10.5: Frame Waiting Time Extension	224
Requirements 10.6: General Rules for Half-Duplex Transmission Protocol.....	226
Requirements 10.7: General Chaining Rule.....	226
Requirements 10.8: Chaining Invocation	227
Requirements 10.9: Block Sizes during Chaining.....	228
Requirements 10.10: Block Numbering Rules.....	230
Requirements 10.11: Block Handling Rules for both PCD and PICC	231
Requirements 10.12: Block Handling Rules for the PCD.....	231
Requirements 10.13: Block Handling Rules for the PICC.....	232
Requirements 10.14: Exception Processing – PICC	233
Requirements 10.15: Exception Processing – PCD	234
Requirements 10.16: S(DESELECT) Response	237

1 General

This chapter contains information that helps the reader understand and use this specification.

1.1 Scope and Audience

This specification, the *EMV Level 1 Specifications for Payment Systems, EMV Contactless Interface Specification*, describes the minimum functionality required of Proximity Integrated Circuit Cards (PICCs) and Proximity Coupling Devices (PCDs) to ensure correct operation and interoperability independent of the application to be used. PICCs and PCDs may provide additional proprietary functionality and features, but these are beyond the scope of this specification and interoperability cannot be guaranteed.

This specification is intended for use by manufacturers of PICCs and PCDs, system designers in payment systems, and financial institution staff responsible for implementing financial applications in PICCs and PCDs.

1.2 Related Information

The following EMV documents provide information related to the subjects discussed in this specification. The latest version applies unless a publication date is explicitly stated.

[PCD MANUAL]	<i>EMV Contactless Specifications for Payment Systems – Level 1 – Test Equipment Specifications – PCD Manual</i>
[PICC MANUAL]	<i>EMV Level 1 Specifications for Payment Systems – Contactless Test Equipment Specifications – PICC Manual</i>
[CMR MANUAL]	<i>EMV Contactless Specifications for Payment Systems – Level 1 – Test Equipment Specifications – CMR Manual</i>
[DTE]	<i>EMV Contactless Terminal Level 1 Type Approval – Device Test Environment</i>
[SYMBOL GUIDE]	<i>EMVCo Contactless Symbol Reproduction Guidelines</i>

1.3 Normative References

The following standards contain provisions that are referenced in this specification. The latest version including all published amendments applies unless a publication date is explicitly stated.

- [ISO/IEC 7810] *Identification cards – Physical characteristics.*
- [ISO/IEC 14443-1] *Identification cards – Contactless integrated circuit(s) cards – Proximity cards – Part 1: Physical characteristics.*
- [ISO/IEC 14443-2] *Identification cards – Contactless integrated circuit(s) cards – Proximity cards – Part 2: Radio frequency power and signal interface.*
- [ISO/IEC 14443-3] *Identification cards – Contactless integrated circuit(s) cards – Proximity cards – Part 3: Initialization and anticollision.*
- [ISO/IEC 14443-4] *Identification cards – Contactless integrated circuit(s) cards – Proximity cards – Part 4: Transmission protocol.*
- [ISO/IEC 13239] *Information technology – Telecommunications and information exchange between systems – High-level data link control (HDLC) procedures.*
- [ISO/IEC 10373-6] *Identification cards – Test methods – Part 6: Proximity cards*

1.4 Acknowledgment

Extracts from standards are reproduced on behalf of ISO with the permission of the British Standards Institution under license number 2003SK/099. BSI & ISO publications can be obtained from:

BSI Customer Services

- Phone:** +44 (0) 20 8996 9001
E-mail: cservices@bsi-global.com
Address: 389 Chiswick High Road
London W4 4AL
United Kingdom

1.5 Definitions

The following terms are used in this specification:

Collision	Transmission by two or more PICCs in the same PCD energizing field and during the same time period, such that the PCD is unable to distinguish from which PICC the data originated.
EMV Contactless Level 1 Test Equipment	Equipment for EMV testing, including: <ul style="list-style-type: none">• EMV – TEST CMR• EMV – TEST PCD• EMV – TEST PICCs Formerly referred to as ‘EMV Reference Equipment’.
EMV – TEST CMR	A signal switching and conditioning unit for the EMV test bench; formerly referred to as ‘EMV Reference CMR’.
EMV – TEST PCD	A PCD simulator used for EMV testing; formerly referred to as ‘EMV Reference PCD’.
EMV – TEST PICC	A PICC simulator used for EMV testing; formerly referred to as ‘EMV Reference PICC’.
IQ TEST PICC	A PICC simulator used for EMV testing. It is used for testing IQ demodulation capabilities of a PCD.
Legacy	A device depending on a behaviour permitted by the specification to accommodate existing products in the field. Future versions of the specification may not support that behaviour. A new product should be designed not to rely upon the continued acceptance of that behaviour.
Modulation index	The modulation index of an amplitude modulated signal is defined as: $m_i = ([A(t)]_{MAX} - [A(t)]_{MIN}) / ([A(t)]_{MAX} + [A(t)]_{MIN})$ where $A(t)$ is the envelope of the modulated carrier.
Operating Field	The magnetic field (H_{OV}) created by the PCD within the Operating Volume.

Operating Volume	The 3-dimensional space in which the PCD can communicate with a PICC by means of a magnetic field.
PCD Test Environment	Test environment for testing the PCD requirements related to the RF Power and Signal Interface as described in [DTE].
Protocol error	A syntax or semantic error.
Proximity IC Card (PICC)	Within these specifications, a PICC is considered to be a consumer token into which integrated circuit(s) and coupling means have been placed and in which communication to such integrated circuit(s) is done by inductive coupling in proximity of a coupling device. The consumer token may be a card of the ID 1 form factor (as defined in [ISO/IEC 7810]), a key fob, a mobile phone, or another form factor.
Proximity Coupling Device (PCD)	The peripheral device of the terminal that uses inductive coupling to provide power to the PICC and also to control the data exchange with the PICC.
Semantic error	A valid frame with no syntax error is received when it is not expected (Chapters 7, 8, 9 and 10).
Syntax error	A valid frame is received with an invalid content: In this case the coding of the command or the block within the frame is not consistent with this specification (Chapters 5, 6 and 10).
Terminal	The device used in conjunction with the PICC at the point of transaction to perform a financial transaction. It incorporates the PCD and may also include other components and interfaces (e.g. host communication).
Time-out error	No response has been sent by the PICC within the Frame Waiting Time (FWT).

Transmission error

An invalid frame is detected by the receiver:
Failure of a parity or CRC check, or determination
that any of the signal modulation, the bit coding,
the frame format, or the timing are not consistent
with this specification (Chapters 3 and 4).

1.6 Notational Conventions

1.6.1 Abbreviations

The abbreviations listed in Table 1.1 are used in this specification.

Table 1.1: Abbreviations

Abbreviation	Description
AC	AntiCollision
ACK	Positive ACKnowledgement
ADC	Application Data Coding, Type B
AFI	Application Family Identifier, Type B
ASK	Amplitude Shift Keying
ATQA	Answer To reQuest, Type A
ATQB	Answer To reQuest, Type B
ATS	Answer To Select, Type A
ATTRIB	PICC selection command, Type B
BCC	UID CLn check byte, Type A
BPSK	Binary Phase Shift Keying
BSI	British Standards Institution
CID	Card IDentifier
CLn	Cascade Level n, Type A
CMR	Common Mode Rejection
CT	Cascade Tag, Type A
CRC_A	Cyclic Redundancy Check error detection code for Type A
CRC_B	Cyclic Redundancy Check error detection code for Type B
D	Divisor
DC	Direct Current
EDC	Error Detection Code
EGT	Extra Guard Time, Type B
EMD	Electromagnetic Disturbance
EoF	End of Frame
EoS	End of Sequence
etu	Elementary time unit

Abbreviation	Description
FDT	Frame Delay Time
f_c	Carrier frequency
FO	Frame Option, Type B
f_s	Subcarrier frequency
FSC	Frame Size for proximity Card
FSCI	Frame Size for proximity Card Integer
FSD	Frame Size for proximity coupling Device
FSDI	Frame Size for proximity coupling Device Integer
FWI	Frame Waiting time Integer
FWT	Frame Waiting Time
HLTA	HaLT command, Type A
HLTB	HaLT command, Type B
HLZ	High Linear load
IEC	International Electrotechnical Commission
INF	INFormation field
IQ	In-phase Quadrature
ISO	International Organization for Standardization
LLZ	Low Linear load
LSB	Least Significant Bit
MBL	Maximum Buffer Length
MBLI	Maximum Buffer Length Index
MSB	Most Significant Bit
NAD	Node ADdress
NAK	Negative AcKnowledgement
n.a.	Not Applicable
NLZ	Non Linear load
NRZ-L	Non-Return to Zero, (L for Level)
OOK	On-Off Keying
PCB	Protocol Control Byte
PCD	Proximity Coupling Device (reader)
PICC	Proximity IC Card
PPS	Protocol and Parameter Selection
PPSR	Protocol and Parameter Selection Response

Abbreviation	Description
PPSS	Protocol and Parameter Selection Start
PPS0	Protocol and Parameter Selection parameter 0
PPS1	Protocol and Parameter Selection parameter 1
PUPI	Pseudo-Unique PICC Identifier, Type B
RATS	REQuest for Answer To Select, Type A
REQA	REQuest command, Type A
REQB	REQuest command, Type B
RF	Radio Frequency
RFU	Reserved for Future Use
rms	Root Mean Square
SAK	Select AcKnowledge, Type A
SFGI	Start-up Frame Guard time Integer
SFGT	Start-up Frame Guard Time
SEL	SElect code, Type A
SoF	Start of Frame
SoS	Start of Sequence
UID	Unique IDentifier, Type A
uid _n	Byte number n of UID, Type A
WTX	Waiting Time eXtension
WTXM	Waiting Time eXtension Multiplier
WUPA	Wake UP command, Type A
WUPB	Wake UP command, Type B

1.6.2 Notations

The notations listed in Table 1.2 apply.

Table 1.2: Notations

Notation	Description
'0' to '9' and 'A' to 'F'	Hexadecimal notation. Values expressed in hexadecimal form are enclosed in straight single quotes (i.e. '_'). For example, 27509 decimal is expressed in hexadecimal as '6B75'.
(1001)b	Binary notation. Values expressed in binary form are enclosed in brackets (i.e. _) and followed by a lower case "b". For example, '08' hexadecimal is expressed in binary as (00001000)b.
[...]	Optional part.
xx	Any value.
STATE	States are written in COURIER FONT to distinguish them from the text.

1.6.3 Terminology and Conventions

The following words are used often in this specification and have a specific meaning:

- shall Defines a product or system capability which is mandatory.
- may Defines a product or system capability which is optional or a statement which is informative only and is out of scope for this specification.
- should Defines a product or system capability which is recommended.

The following conventions apply:

Value of Parameters

Throughout the specification, symbols are used to identify the values of parameters. The permitted values of the parameters are listed in Annex A and are written in **Arial bold** to distinguish them in the text. When used to define timings, frequencies, etc., it is the actual value that is intended. For example f_c is the actual carrier frequency from the PCD.

Requirement Numbering

Requirements in this specification are uniquely numbered with the number appearing next to each requirement: For example:

- 5.4.2.1 The PCD shall verify the BCC included in the UID CLn. The PCD shall consider an incorrect BCC as a transmission error.

A requirement may have different numbers in different versions of the specifications. Hence, all references to a requirement should include the version of the specification as well as the requirement's number.

Requirements may include informative statements. In this case the statement is written in the *italic font* and the verb 'may' instead of 'shall' is used.

1.6.4 Reserved for Future Use (RFU)

Requirements 1.1: RFU

PCD and PICC

- 1.6.4.1 A bit specified as Reserved for Future Use (RFU) shall be set as specified, or to (0)b if no indication is given. An entity receiving a bit specified as RFU shall ignore such a bit and shall not change its behaviour, unless explicitly stated otherwise.
- 1.6.4.2 A data field having a value coded on multiple bits or bytes shall not be set to a value specified as RFU. An entity receiving a data field having a value specified as RFU, shall behave as defined by a requirement that specifically addresses the situation, or shall consider it a protocol error if no specific behaviour is defined.

2 Introduction

This chapter includes an introduction to the *EMV Contactless Interface Specification* of the *EMV Level 1 Specifications for Payment Systems*.

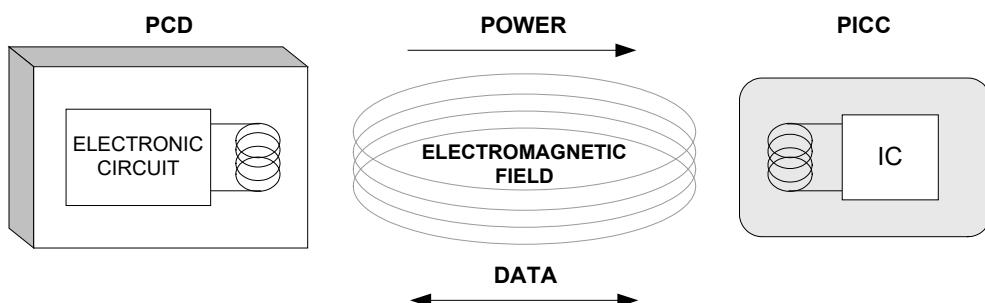
2.1 Contactless System

The basic components of a contactless system are the contactless reader or Proximity Coupling Device (PCD) and a transponder or Proximity IC Card (PICC).

The PCD is an antenna connected to an electronic circuit. The PICC consists of an inductive antenna and an integrated circuit connected to the ends of the antenna. The combination PCD – PICC behaves like a transformer. An alternating current passes through a primary coil (PCD antenna) and creates an electromagnetic field, which induces a current in the secondary coil (PICC antenna). The PICC converts the electromagnetic field (or RF field) transmitted by the PCD into a DC voltage by means of a diode rectifier, and uses the DC voltage to power the PICC's internal circuits. The configuration and tuning of both antennas determines the coupling efficiency from one device to the other.

The PCD and PICC are shown in Figure 2.1.

Figure 2.1: PCD and PICC Configuration



The addition of information to an electronic (or optical) signal carrier is called modulation. A signal carrier is characterized by means of its amplitude, phase, and frequency. Therefore, information can be added to the carrier by means of changing one or more of these characteristics. Modulation methods used in this specification are:

- Amplitude modulation: The level of the signal carrier is varied over time.
- Phase modulation: The flow of the signal carrier is either advanced or delayed temporarily, giving a change in phase.

The RF energy transmitted by the PCD and received by the PICC not only powers up the PICC but is also used to transport the data through modulation of the carrier. The PICC decodes and processes the data and responds to the PCD by means of load modulation.

Load modulation is based on the electromagnetic coupling (i.e. mutual inductance) between PICC and PCD similar to the power transfer and communication from PCD to PICC. The PICC changes the current in its antenna. The current variation in the PICC antenna is sensed by the PCD as a small change in the current in its antenna, typically sensed as a small increase in voltage across a resistor in series with the PCD antenna.

2.2 EMV Contactless Level 1 Test Equipment

The RF power and signal interface part of the specification is specified in terms of the EMV Contactless Level 1 Test Equipment. EMV Contactless Level 1 Test Equipment consists of an EMV – TEST PCD, three EMV – TEST PICCs, and an EMV – TEST CMR (Common Mode Rejection). The purpose of the EMV Contactless Level 1 Test Equipment is to provide a PCD and PICCs that cover the variations in contactless technology. A PCD can therefore be tested against the EMV – TEST PICCs and a PICC can be checked against the EMV – TEST PCD.

There is no requirement to create contactless devices using the architecture, antenna layout, and resonance frequencies used for the EMV – TEST PCD or EMV – TEST PICCs. The EMV Contactless Level 1 Test Equipment is put in place to specify an externally observable behaviour. A PCD or PICC with a completely different design, that creates a similar observable behaviour, can meet the requirements as described in Chapter 3.

Specific test equipment is used to ensure PCDs are able to receive load modulation signals that are comprised of a mixture of amplitude and phase modulation components (e.g. using IQ demodulation methods). Unlike the EMV – TEST PCD, EMV – TEST PICCs and EMV – TEST CMR, the detailed specification of the IQ demodulation test equipment is not in the scope of this specification. However, EMVCo will qualify that the equipment and processes used by accredited laboratories meet the standard required to achieve consistent results.

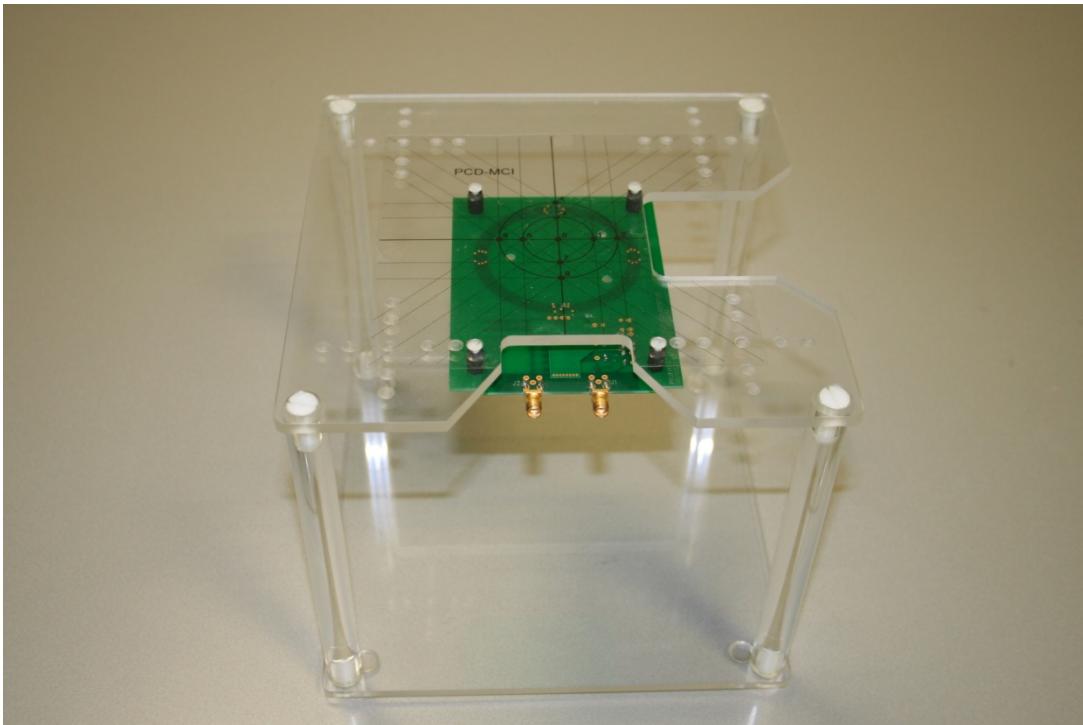
2.2.1 EMV – TEST PCD

The EMV – TEST PCD (Figure 2.2) has a circular antenna of about 7 cm, which is in the small range of antenna sizes encountered in EMV terminals. The circular antenna creates a symmetric field distribution from the z-axis, which simplifies measurements. When fed with 600 mW into its $50\ \Omega$ input impedance at resonance, the EMV – TEST PCD provides a magnetic field which is representative of most PCDs.

The EMV – TEST PCD allows commands to be sent to PICCs when connected to a signal generator. The response from a PICC can be analyzed by means of the EMV – TEST CMR.

The EMV – TEST PCD circuit is mounted in a covered assembly as shown in Figure 2.2.

Figure 2.2: EMV – TEST PCD

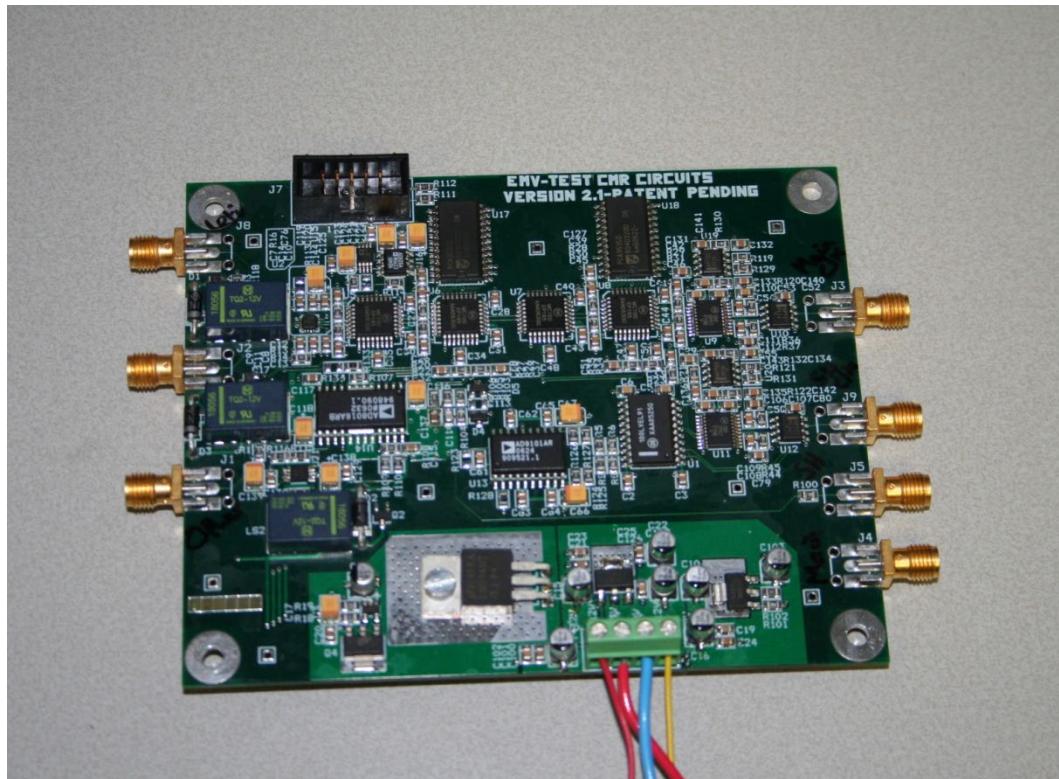


2.2.2 EMV – TEST CMR

The aim of the EMV – TEST CMR is to form a signal switching and conditioning unit for the test bench. It is expected that it would be connected to J2 of the EMV – TEST PCD, J9 of an EMV – TEST PICC and the analogue to digital converter of the test bench.

The EMV – TEST CMR circuit is shown in Figure 2.3.

Figure 2.3: EMV – TEST CMR



2.2.3 EMV – TEST PICCs

There are three EMV – TEST PICCs:

- **EMV – TEST PICC 1**
Tuned to 16.1 MHz
- **EMV – TEST PICC 2**
Tuned to 13.56 MHz
- **EMV – TEST PICC 3**
Tuned to 13.56 MHz

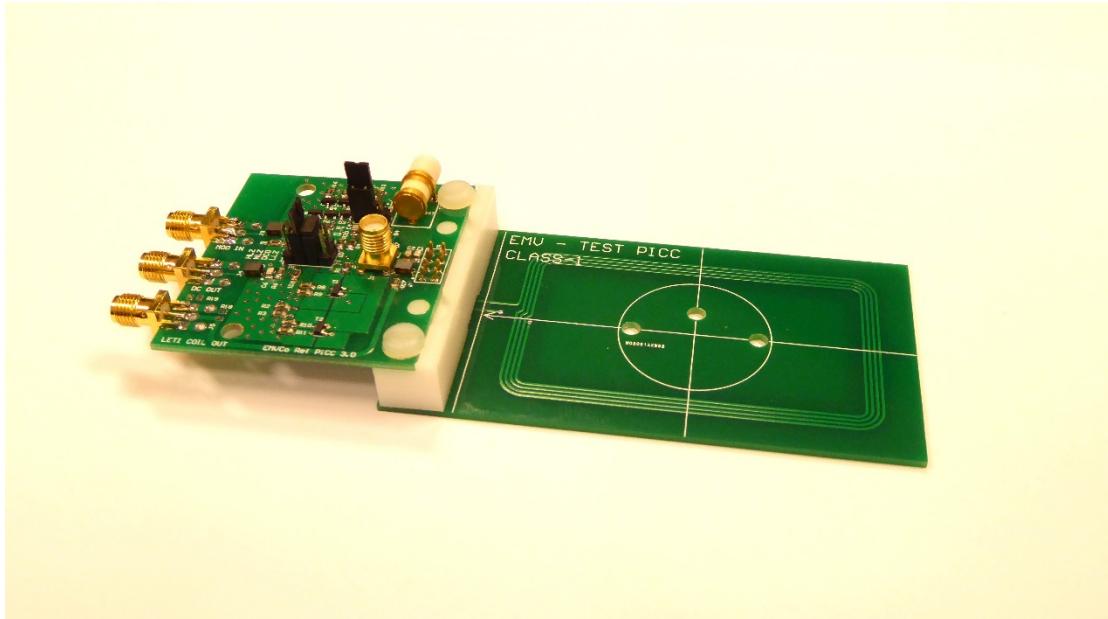
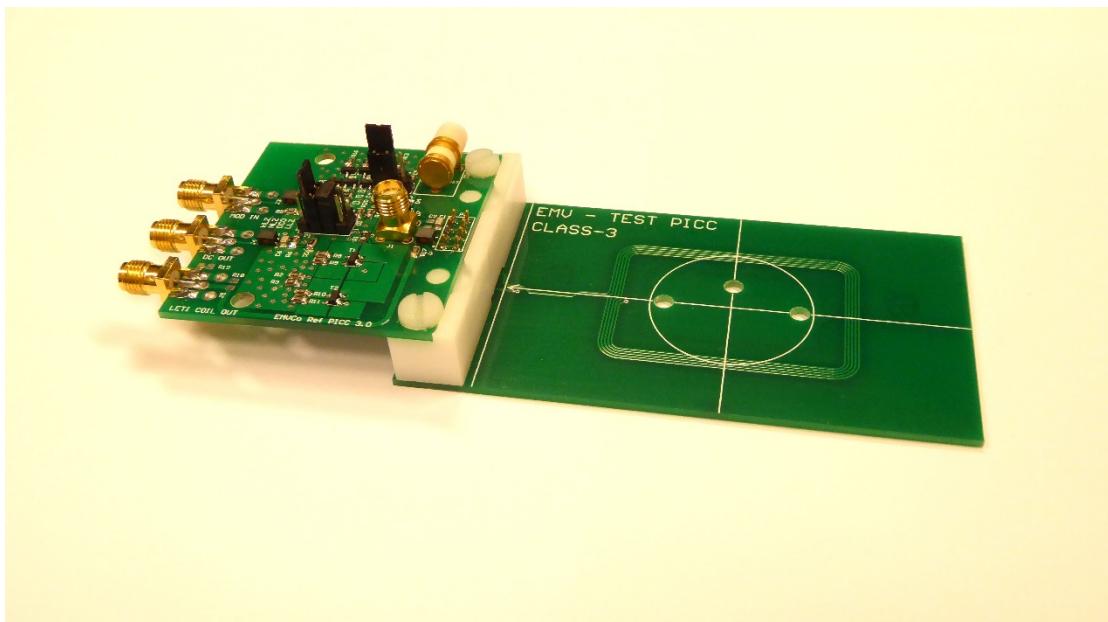
EMV – TEST PICC 1 and EMV – TEST PICC 2 have an ISO/IEC class 1 size antenna similar to those found in ISO/IEC ID-1 cards. The EMV – TEST PICC 3 has an antenna similar to the ISO/IEC class 3.

The EMV – TEST PICCs allow the analysis of the signal as sent out by a PCD. For analyzing the frequency content of these signals, they are equipped with a pickup coil, which is an integral part of the EMV – TEST PICC.

The EMV – TEST PICCs can also send information back to a PCD, using various levels of load modulation.

The EMV – TEST PICCs can be configured with two linear loads (LLZ & HLZ) and a non linear load (NLZ). The non linear load is self-adapting to the magnetic field strength. The (variable) load parameters are set based on the maximum power consumption in current contactless cards. The maximum power consumption represents a worst case scenario for a PCD. It is expected that a PICC will require less power than EMV – TEST PICC 2.

EMV – TEST PICC 1 is shown in Figure 2.4 and EMV – TEST PICC 3 is shown in Figure 2.5.

Figure 2.4: EMV – TEST PICC 1**Figure 2.5: EMV – TEST PICC 3**

2.2.4 IQ Demodulation Test Equipment

The test equipment consists of:

- An IQ TEST PICC using the principle of active load modulation whereby the PICC actively transmits carrier sideband signals to the PCD under test. The load modulation generated in this way is synchronised to the carrier of the PCD under test and is configurable in the amplitudes and phases of the modulation components that are created.
- Associated equipment to detect sequences of commands from the PCD when the IQ TEST PICC is placed in the Operating Volume to ensure responses are transmitted with the correct timing and content and to verify if the PCD functions properly.

2.3 Landing Plane

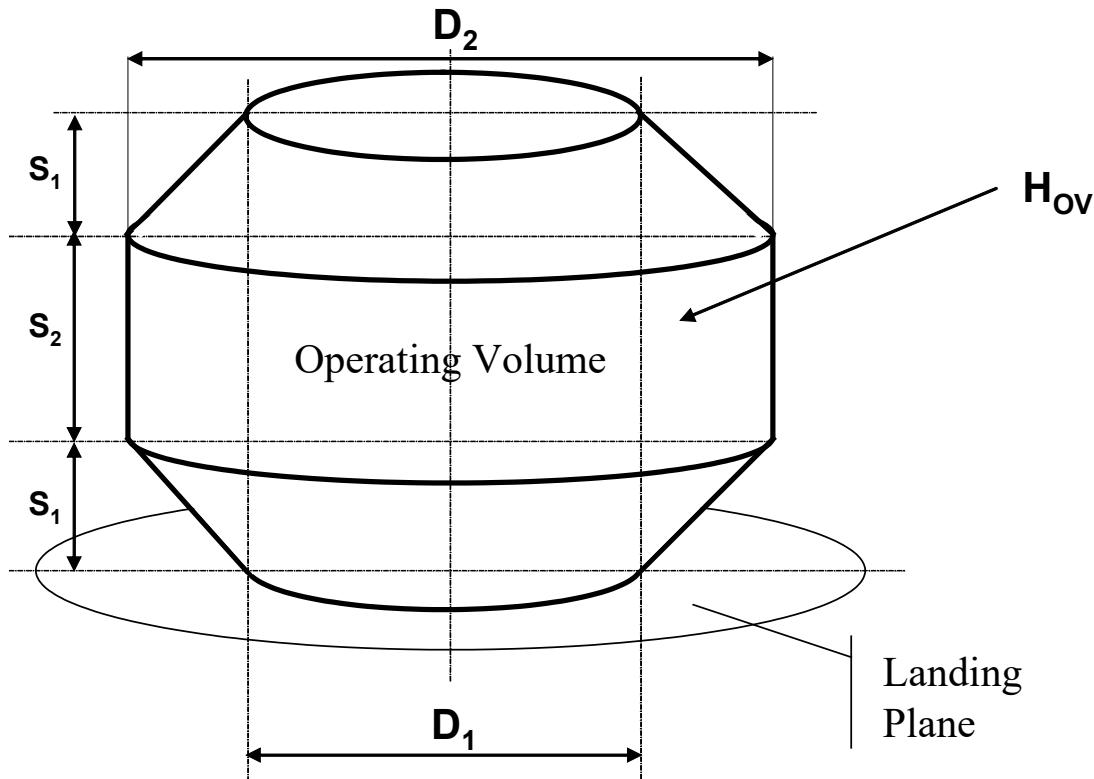
A PCD identifies where a customer should tap the PICC to achieve a successful read. This identified area is referred to as the landing plane. The landing plane is a clearly distinguishable area on the PCD. To ensure a consistent approach of identifying the landing plane, the contactless symbol is placed in the centre of the landing plane.

The rules for the use of the contactless symbol are detailed in [SYMBOL GUIDE].

2.4 Operating Volume

The Operating Volume of a PCD is the 3-dimensional space for which this specification imposes requirements on the magnetic field H_{ov} (Operating Field). The geometry of the Operating Volume is shown in Figure 2.6. The Operating Volume is measured from the centre of the landing plane, along an axis perpendicular to the landing plane. Requirements on this geometry suppose that the PCD is stationary and that the PICC moves slowly (less than 1 m/s) through the Operating Volume. The position of a PICC within the Operating Volume is represented by the quadruplet (r, φ, z, θ) as described in Annex B. The values of the symbols used in Figure 2.6 are defined in Annex A.1.

Figure 2.6: Operating Volume



Any PCD approval testing carried out against this specification will use the centre of the contactless symbol as the reference point to indicate the centre of the Operating Volume $(r,\phi,z) = (0,0,0)$.

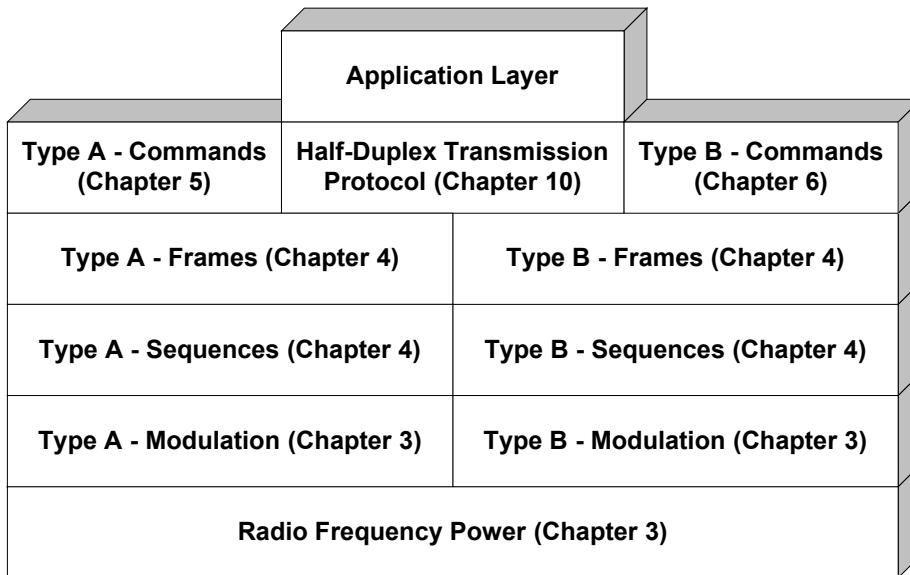
In order to provide the required power to the PICC, the PCD creates a magnetic field strength of at least the specified minimum level. The maximum field strength that a PCD can create is limited to prevent excess dissipation in the PICC. Refer to section 3.2.1 for requirements regarding minimum and maximum field strength.¹

¹ The maximum field strength must also comply with all international and national legal and regulatory requirements.

2.5 Overview

This specification lists the EMV specific communication protocol requirements for PICCs and PCDs based on the protocol as described in ISO/IEC 14443 1-4. The specification uses a layered approach as shown in Figure 2.7.

Figure 2.7: Communication Protocol Layers



Besides the various protocol layers, this document also deals with the specification of the state machine of the PICC and the specification of the PCD processing (polling, collision detection, activation, removal, and exception processing).

This volume is organised into the following chapters and annexes:

Chapter 1 contains general information that helps the reader understand and use this specification.

Chapter 2 contains an introduction to the concepts used in this specification.

Chapter 3 describes the electrical characteristics of the contactless interface between a PICC and PCD. The interface includes the power requirements for the electromagnetic field established by the PCD and the modulation methods for the bi-directional data transfer between the PICC and the PCD. This chapter describes the two ISO/IEC 14443 communication signal interfaces: Type A and Type B. Both communication signal interfaces use different modulation methods for the PCD to PICC and the PICC to PCD communication.

Chapter 4 describes the protocol layers sequence and frame. It specifies the coding techniques used for establishing the symbol alphabets and bit level coding. The ISO/IEC 14443 protocol uses different bit coding techniques for Type A and Type B.

Chapter 4 also specifies the frames used for Type A and Type B. When transmitted between PCD and PICC, data bits are grouped within frames. This chapter lists the specific requirements for Type A and Type B with regard to the frame format, frame size, and timing.

Chapters 5 and 6 specify the commands that are available to the PCD for the polling, collision detection, activation, and removal procedures. Chapter 5 lists the requirements related to Type A commands and responses. Chapter 6 does the same for the Type B commands and responses.

Chapter 7 specifies the state machine of a Type A PICC with regard to polling, collision detection, and PICC activation. Chapter 8 does the same for a Type B PICC. Note that the state machines as defined in this specification do not include the state machine(s) of the application(s) residing on the EMV card.

Chapter 9 specifies the PCD processing during polling, collision detection, PICC activation, and PICC removal. This chapter includes a detailed description of the specific requirement that the PCD does not initiate the transaction if more than one PICC is detected in the Operating Field.

Chapter 10 defines the data transmission protocol. The half-duplex block transmission protocol defined in this chapter is common for Type A and Type B and uses the frame format as defined in Chapter 4. The transmission protocol is used to convey information for use by the application layer. The application layer itself is outside the scope of this specification.

Annex A contains the values of the various parameters for both PICC and PCD as defined throughout the specification. Note that the same parameter may have a different value and tolerance when used by the PICC or the PCD.

Annex B contains the convention used to define the position of a PICC within the Operating Volume.

3 Radio Frequency Power and Signal Interface

This chapter specifies the electrical characteristics of the two signalling schemes (Type A and Type B) of the contactless interface supported by EMV. The interface includes both power and bi-directional communication between a PCD and a PICC.

3.1 Introduction

This chapter specifies the RF power and signal interface requirements for the PCD and PICC. All the requirements included in this chapter are specified with respect to the EMV Contactless Level 1 Test Equipment. Requirements are preceded by a measurement procedure describing how to use the EMV Contactless Level 1 Test Equipment to validate the specific requirement. The remainder of this section explains the approach used for writing the requirements.

3.1.1 Transmission and Reception Requirements

A device, which can be a PCD or a PICC, is either transmitting or receiving. A PCD transmits power and data to a PICC and receives data from this PICC. A PICC receives power as well as data from a PCD and can transmit data to the PCD. The configurations for transmitting and receiving for PCD and PICC are illustrated in Table 3.1.

Table 3.1: Configurations Transmit and Receive

	PCD		PICC	
	Transmit	Receive	Transmit	Receive
Power	✓	n.a.	n.a.	✓
Data	✓	✓	✓	✓

For each device, the requirements related to transmission are such that the value of a transmission parameter falls within a well defined range R_{tx} for the parameter. The requirements on reception are such that the receiver is required to work properly with the value of different parameters varying over a range R_{rx} relevant for each parameter. For interoperability, the ranges for corresponding transmission and reception parameters are defined so that the range R_{tx} is contained within R_{rx} .

3.1.2 EMV Contactless Level 1 Test Equipment

Whether a device meets the transmission requirements is measured by means of the receiver of the appropriate EMV Contactless Level 1 Test Equipment. That is:

- Whether the transmitter of a PCD meets the requirements is measured by means of the EMV – TEST PICCs.
- The quality of the transmitter of a PICC is measured on the EMV – TEST PCD.

Example:

A PCD is required to provide a certain level of power to a PICC. The power delivered by the PCD is measured on the EMV – TEST PICCs. The value of the power level measured on an EMV – TEST PICC is required to fall within range $R_{tx,power}$.

Whether a device meets the reception requirements is measured by having the appropriate EMV Contactless Level 1 Test Equipment transmit a range of values for a number of parameters. That is:

- Whether the receiver of a PCD meets the requirements is measured by having the EMV – TEST PICCs transmit different levels of load modulation.
- The quality of the receiver of a PICC is verified by having the EMV – TEST PCD transmit different levels of modulation.

In order to set up the transmitter of the EMV Contactless Level 1 Test Equipment, the receiver of the matching EMV Contactless Level 1 Test Equipment is used. That is:

- The load modulation level of an EMV – TEST PICC is characterized with respect to the EMV – TEST PCD.
- The modulation level of the EMV – TEST PCD is characterized with respect to the EMV – TEST PICCs.

Example:

A PICC is required to work with a certain power level provided by a PCD. The EMV – TEST PCD generates different power levels, varying over a range $R_{rx,power}$. The power level of the EMV – TEST PCD is set up with respect to an EMV – TEST PICC. This means that $R_{rx,power}$ is a value measured on the EMV – TEST PICC and that the power level of the signal generator feeding the EMV – TEST PCD is increased/decreased until the correct (voltage) level is reached on the EMV – TEST PICC.

The power and data transmission characteristics of a PCD can be tested in isolation as it is a master device. Testing the characteristics of a PICC cannot be done in isolation, as it is a slave device, requiring stimulation from a PCD. For testing the transmission characteristics, the PICC will receive commands from the EMV – TEST PCD. Signal parameters on the EMV – TEST PCD will have a value within the allowed R_x range to ensure a response from the PICC.

3.1.3 ‘Function Properly’

For both a PCD and a PICC, checking the data reception characteristics depends on some kind of acknowledgement by the device that the data was received. For a PCD, sending the next command (=data transmission) in the overall flow implies that the response from the EMV – TEST PICC was understood. For a PICC, a change in internal state implies that the command from the PCD was understood.

For the remainder of the specification, the wording ‘function properly’ will be used for a PCD sending the next command, following a response created by the EMV – TEST PICC.

‘Function properly’ is also used for a PICC receiving a command generated by the EMV – TEST PCD. For the purpose of this specification, the receiver of a PICC is considered to function properly if the processing of a command sent by the EMV – TEST PCD results in the required change in the internal state of the PICC corresponding the command. Examples of a change in internal state are:

- Changing the state of the state machine of the PICC (making it capable of processing the next command)
- Changing the internal memory of the PICC (volatile or non-volatile memory)

3.1.4 Temperature and Humidity

Unless specified otherwise, all measurements described in this chapter take place in an environment of temperature at $23^{\circ}\text{C} \pm 3^{\circ}\text{C}$ and of relative humidity of 40% to 60%.

3.1.5 Summary

The approach explained above leads to the following with regard to power and data transfer:

- Power provided by a PCD is measured on the EMV – TEST PICCs.
- Data transmission by a PCD (e.g. modulation depth) is measured on the EMV – TEST PICCs.
- Data reception by a PCD (load modulation sensitivity) is measured by creating different signals through the EMV – TEST PICCs. To determine the levels and characteristics of the signal generated by the EMV – TEST PICCs, the signal is first characterized with respect to the EMV – TEST PCD.
- Data transmission by a PICC is measured on the EMV – TEST PCD, with the EMV – TEST PCD providing a power level and command characteristics characterized with respect to the EMV – TEST PICCs.
- Power and data reception sensitivity of a PICC are measured by means of the EMV – TEST PCD, with the EMV – TEST PCD sending commands with power levels and modulation characteristics at the border of the tolerance interval R_{rx} . Again, for setting these extreme values, the power and command characteristics produced by the EMV – TEST PCD are characterized with respect to the EMV – TEST PICCs.

3.2 RF Power

This section specifies the requirements for the power transfer from PCD to PICC through the electromagnetic field created by the PCD.

All measurements described in this section are performed with the EMV – TEST PCD and the EMV – TEST PICCs calibrated as specified in [PCD MANUAL] and [PICC MANUAL]. The position of a PICC within the Operating Volume is indicated according to the convention specified in Annex B.

3.2.1 PCD Requirements for Power Transfer PCD to PICC

This section specifies the PCD requirement for power transfer from PCD to PICC. The PCD creates an energizing RF field (the Operating Field) that enables the PICC to enter an operational state. Table 3.2 describes the measurement procedure for the power transfer from PCD to PICC.

Table 3.2: Measurement of Power Transfer PCD to PICC (PCD Transmission)

Step #	Action
Step 1	Activate the PCD to emit the carrier without any modulation by using the PCD Test Environment.
Step 2	Place the EMV – TEST PICC 1 in the Operating Volume of the PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.
Step 3	Measure the mean value of the voltage at J1 of the EMV – TEST PICC 1.
Step 4	Repeat Step 1 to Step 3 with EMV – TEST PICC 2 and EMV – TEST PICC 3.

Requirements 3.1: Power Transfer PCD to PICC (PCD Transmission)

PCD

- 3.2.1.1 Within the Operating Volume, the PCD shall generate a voltage V_{ov} at J1 of the EMV – TEST PICC.²
The voltage V_{ov} shall be measured as described in Table 3.2.
Refer to Annex A.2 for the value of V_{ov} .

² This requirement remains valid also when the PCD polls for other technologies as described in section 9.2.

3.2.2 PICC Requirements for Power Transfer PCD to PICC

This section specifies the PICC requirement for power transfer from PCD to PICC. Table 3.3 and Table 3.4 describe the measurement procedures that verify whether the PICC functions properly in the Operating Field of the EMV – TEST PCD with field strength H_{ov} .

Table 3.3: Measurement of Power Transfer PCD to PICC (PICC Reception) – Type A

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.
Step 2	Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ to the extremes of the range specified in Annex A.3 at J1 of the EMV – TEST PICC 1.
Step 3	Configure EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $t_{s,1}$, $t_{s,2}$, $t_{s,3}$ and $t_{s,4}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 4	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD and verify whether the PICC functions properly.

Table 3.4: Measurement of Power Transfer PCD to PICC (PICC Reception) – Type B

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.

Step #	Action
Step 2	Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ to the extremes of the range specified in Annex A.3 at J1 of the EMV – TEST PICC 1.
Step 3	Configure EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s1,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 4	Remove EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $0 \leq z < 2$ cm and verify whether the PICC functions properly.
Step 5	Remove the PICC from the Operating Volume of the EMV – TEST PCD. Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s2,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 6	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $2 \leq z < 3$ cm and verify whether the PICC functions properly.
Step 7	Remove the PICC from the Operating Volume of the EMV – TEST PCD. Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s3,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 8	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD and place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $3 \leq z \leq 4$ cm and verify whether the PICC functions properly.

Requirements 3.2: Power Transfer PCD to PICC (PICC Reception)

PICC

- 3.2.2.1 A PICC shall function properly within the Operating Volume of the EMV – TEST PCD provided the EMV – TEST PCD has been set up as described in Table 3.3 and Table 3.4.
-

3.2.3 Influence of the PICC on the Operating Field

Due to the electromagnetic coupling (i.e. mutual inductance) between the PICC and PCD antennas, the PICC changes the Operating Field created by the PCD when brought into the Operating Volume. The magnetic field strength within the Operating Volume will decrease due to the extra load caused by the PICC. This section lists the PICC requirement limiting the maximum load a PICC is allowed to present to a PCD.

The load of a PICC is measured by the voltage drop $\Delta V_{\text{SENSE,PICC}}$ ($= V_{\text{SENSE,FREE AIR}} - V_{\text{SENSE,PICC}}$) at J2 of the EMV – TEST PCD caused by the presence of the PICC in the Operating Volume as described in Table 3.5.

Table 3.5: Measurement of the Influence of the PICC on the Operating Field

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in position ($r=0$, $\phi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.
Step 2	Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage defined by the minimum value of $V_{s,ov}$ specified in Annex A.3 at J1 of the EMV – TEST PICC 1.
Step 3	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD.
Step 4	Measure $V_{\text{SENSE,FREE AIR}}$ (peak to peak) at J2 of the EMV – TEST PCD.
Step 5	Place the PICC in the Operating Volume of the EMV – TEST PCD and measure $V_{\text{SENSE,PICC}}$ (peak to peak) at J2 of the EMV – TEST PCD.
Step 6	Configure the EMV – TEST PICC 2 with NLZ.
Step 7	Remove the PICC from the Operating Volume of the EMV – TEST PCD. Place the EMV – TEST PICC 2 in the Operating Volume of the EMV – TEST PCD centred on the z-axis at the same height as the PICC in Step 5 and measure $V_{\text{SENSE,TESTPICC2}}$ (peak to peak) at J2 of the EMV – TEST PCD.

Requirements 3.3: Influence of the PICC on the Operating Field

PICC

- 3.2.3.1 When placed in the Operating Volume of the EMV TEST PCD, the loading caused by the PICC shall be equal to or less than the loading caused by the EMV – TEST PICC 2.

The associated parameter $\Delta V_{SENSE R}$ is defined as the ratio between the loading of the PICC to the loading of the EMV – TEST PICC 2.

$$\Delta V_{SENSE,PICC} = V_{SENSE,FREE AIR} - V_{SENSE,PICC}$$

$$\Delta V_{SENSE,TESTPICC2} = V_{SENSE,FREE AIR} - V_{SENSE,TESTPICC2}$$

$$\Delta V_{SENSE R} = \Delta V_{SENSE,PICC} / \Delta V_{SENSE,TESTPICC2}$$

$V_{SENSE,FREE AIR}$, $V_{SENSE,PICC}$ and $V_{SENSE,TESTPICC2}$ shall be measured as described in Table 3.5.

Refer to Annex A.2 for the value of $\Delta V_{SENSE R}$.

3.2.4 PCD Requirement for the Carrier Frequency f_c

This section specifies the PCD requirement for the frequency of the Operating Field (i.e. the carrier frequency f_c) created by the PCD. Table 3.6 describes how to measure f_c .

Table 3.6: Measurement of Carrier Frequency f_c (PCD Transmission)

Step #	Action
Step 1	Activate the PCD to emit the carrier without any modulation by using the PCD Test Environment.
Step 2	Place the EMV – TEST PICC 1 in the Operating Volume of the PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.
Step 3	Capture the signal at the output of the pickup coil (J9) of the EMV – TEST PICC 1 and measure the frequency of the carrier.

Requirements 3.4: Carrier Frequency f_c (PCD Transmission)

PCD

3.2.4.1 The frequency of the Operating Field (carrier frequency) provided by the PCD shall be f_c .

The frequency shall be measured as described in Table 3.6.

Refer to Annex A.2 for the value of f_c .

3.2.5 PICC Requirement for the Carrier Frequency $f_{s,c}$

This section specifies the PICC requirement for the frequency of the Operating Field (i.e. the carrier frequency f_c). Table 3.7 and Table 3.8 describe the measurement procedures that verify whether a PICC functions properly in the Operating Field of the EMV – TEST PCD with a carrier frequency $f_{s,c}$.

Table 3.7: Measurement of Carrier Frequency $f_{s,c}$ (PICC Reception) – Type A

Step #	Action
Step 1	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.</p> <p>Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ to the extremes of the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ within the range specified in Annex A.3 at J1 of the EMV – TEST PICC 1.</p>
Step 2	Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $t_{s,1}$, $t_{s,2}$, $t_{s,3}$ and $t_{s,4}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 3	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD and verify whether the PICC functions properly.

Table 3.8: Measurement of Carrier Frequency $f_{s,c}$ (PICC Reception) – Type B

Step #	Action
Step 1	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.</p> <p>Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ to the extremes of the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ within the range specified in Annex A.3 at J1 of the EMV – TEST PICC 1.</p>
Step 2	<p>Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s1,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.</p>
Step 3	<p>Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $0 \leq z < 2$ cm and verify whether the PICC functions properly.</p>
Step 4	<p>Remove the PICC from the Operating Volume of the EMV – TEST PCD. Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD.</p> <p>Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s2,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.</p>
Step 5	<p>Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $2 \leq z < 3$ cm and verify whether the PICC functions properly.</p>
Step 6	<p>Remove the PICC from the Operating Volume of the EMV – TEST PCD. Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD.</p> <p>Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s3,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.</p>

Step #	Action
Step 7	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $3 \leq z \leq 4$ cm and verify whether the PICC functions properly.

Requirements 3.5: Carrier Frequency $f_{s,c}$ (PICC Reception)

PICC

- 3.2.5.1 When placed in the Operating Volume of the EMV – TEST PCD, a PICC shall function properly at a carrier frequency $f_{s,c}$ provided the EMV – TEST PCD has been set up as described in Table 3.7 and Table 3.8.

3.2.6 PCD Requirements for Resetting the Operating Field

This section specifies how the PCD performs a reset of the Operating Field.

Table 3.9 describes how to measure whether the Operating Field is correctly reset by the PCD.

Table 3.9: Measurement of Resetting the Operating Field

Step #	Action
Step 1	Activate the PCD to emit the carrier without any modulation by using the PCD Test Environment.
Step 2	Place the [ISO/IEC 10373-6] calibration coil 1 in the Operating Volume of the PCD.
Step 3	Request the PCD to reset the Operating Field by using the PCD Test Environment.
Step 4	Capture the (open circuit) voltage signal at the output of the [ISO/IEC 10373-6] calibration coil 1 from the start until the end of the reset.

Requirements 3.6: Reset Operating Field (PCD Transmission)

PCD

- 3.2.6.1 When the PCD resets the Operating Field, then within the Operating Volume, the PCD shall not generate any field for a time t_{RESET} .

Refer to Annex A.5 for the value of t_{RESET} .

3.2.7 PICC Requirements for Power-off

This section specifies the power-off requirements for the PICC. Table 3.10 and Table 3.11 describe the measurement procedures.

Table 3.10: Measurement of PICC Power-off – Type A

Step #	Action
Step 1	Place the [ISO/IEC 10373-6] calibration coil 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD.
Step 2	Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates an (open circuit) voltage $V_{s,ov,RESET}$ (rms) to the extremes of the range specified in Annex A.3 at the output of the [ISO/IEC 10373-6] calibration coil 1. The current settings of the signal generator are further on referenced as $V_{GEN,RESET}$.
Step 3	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ at J1 of the EMV – TEST PICC 1 within the range specified in Annex A.3.
Step 4	Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $t_{s,1}$, $t_{s,2}$, $t_{s,3}$ and $t_{s,4}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 5	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD and send the appropriate commands to put a PICC of Type A in the PROTOCOL state (refer to Chapter 7).
Step 6	Regulate the signal generator back to $V_{GEN,RESET}$ for a time t_{RESET} before re-applying a power level $V_{s,ov}$ within the range specified in Annex A.3. Wait for a time t_P and verify if the PICC is in IDLE state. Refer to Annex A.5 for the values of t_{RESET} (PICC value) and t_P (PCD value).

Table 3.11: Measurement of PICC Power-off – Type B

Step #	Action
Step 1	Place the [ISO/IEC 10373-6] calibration coil 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD.
Step 2	<p>Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates an (open circuit) voltage $V_{s,ov,RESET}$ (rms) to the extremes of the range specified in Annex A.3 at the output of the [ISO/IEC 10373-6] calibration coil 1.</p> <p>The current settings of the signal generator are further referenced as $V_{GEN,RESET}$.</p>
Step 3	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.</p> <p>Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ at J1 of the EMV – TEST PICC 1 within the range specified in Annex A.3.</p>
Step 4	Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s1,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 5	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $0 \leq z < 2$ cm and send the appropriate commands to put a PICC of Type B in the ACTIVE state (refer to Chapter 8).
Step 6	<p>Regulate the signal generator back to $V_{GEN,RESET}$ for a time t_{RESET} before re-applying a power level $V_{s,ov}$ within the range specified in Annex A.3. Wait for a time t_P and verify if the PICC is in IDLE state.</p> <p>Refer to Annex A.5 for the values of t_{RESET} (PICC value) and t_P (PCD value).</p>

Step #	Action
Step 7	<p>Remove the PICC from the Operating Volume of the EMV – TEST PCD.</p> <p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD.</p> <p>Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s2,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.</p>
Step 8	<p>Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $2 \leq z < 3$ cm and send the appropriate commands to put a PICC of Type B in the ACTIVE state (refer to Chapter 8).</p>
Step 9	<p>Regulate the signal generator back to $V_{GEN,RESET}$ for a time t_{RESET} before re-applying a power level $V_{s,ov}$ within the range specified in Annex A.3. Wait for a time t_P and verify if the PICC is in IDLE state.</p> <p>Refer to Annex A.5 for the values of t_{RESET} (PICC value) and t_P (PCD value).</p>
Step 10	<p>Remove the PICC from the Operating Volume of the EMV – TEST PCD.</p> <p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD.</p> <p>Configure the EMV – TEST PICC 1 with LLZ. Modulate the carrier to obtain modulation characteristics $m_{s3,i}$, $t_{s,f}$ and $t_{s,r}$ within the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.</p>
Step 11	<p>Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $3 \leq z \leq 4$ cm and send the appropriate commands to put a PICC of Type B in the ACTIVE state (refer to Chapter 8).</p>
Step 12	<p>Regulate the signal generator back to $V_{GEN,RESET}$ for a time t_{RESET} before re-applying a power level $V_{s,ov}$ within the range specified in Annex A.3. Wait for a time t_P and verify if the PICC is in IDLE state.</p> <p>Refer to Annex A.5 for the values of t_{RESET} (PICC value) and t_P (PCD value).</p>

Requirements 3.7: PICC Power-off

PICC

- 3.2.7.1 A PICC shall return to the **POWER-OFF** state no later than t_{RESET} after the Operating Field is switched off as specified in Table 3.10 and Table 3.11.

Refer to Annex A.5 for the value of t_{RESET} .

3.2.8 PICC Requirements for Power-on

This section specifies the power-on requirements for the PICC. Table 3.12 describes the measurement procedure.

Table 3.12: Measurement of PICC Power-on

Step #	Action
Step 1	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.</p> <p>Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ within the range specified in Annex A.3 at J1 of the EMV – TEST PICC 1.</p>
Step 2	Configure EMV – TEST PICC 1 with LLZ. Set up the EMV – TEST PCD to obtain modulation characteristics as specified in Annex A.3.
Step 3	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD and verify that the PICC goes from POWER-OFF state to IDLE state (refer to Chapter 7 and Chapter 8) no later than t_P .

Requirements 3.8: PICC Power-on

PICC

- 3.2.8.1 If a PICC in **POWER-OFF** state is placed in the Operating Volume of the EMV – TEST PCD, it shall enter the **IDLE** state no later than t_P , provided the EMV – TEST PCD has been set up as described in Table 3.12.

Refer to Annex A.5 for the value of t_P .

3.2.9 PCD Requirements for Power-off of the Operating Field

This section specifies how the PCD performs a power-off of the Operating Field. Table 3.13 describes how to measure whether the power-off of the Operating Field is correctly performed by the PCD.

Table 3.13: Measurement of Power-off of the Operating Field

Step #	Action
Step 1	Activate the PCD to emit the carrier without any modulation by using the PCD Test Environment.
Step 2	Place the [ISO/IEC 10373-6] calibration coil 1 in the Operating Volume of the PCD.
Step 3	Request the PCD to perform a power-off of the Operating Field by using the PCD Test Environment.
Step 4	Capture the signal at the output of [ISO/IEC 10373-6] calibration coil 1 for at least a time $t_{POWEROFF}$ from the start of the power-off.

Requirements 3.9: Power-off of the Operating Field (PCD Transmission)

PCD

- 3.2.9.1 When the PCD performs a power-off of the Operating Field, then within the Operating Volume, the PCD shall not generate any field for at least a time $t_{POWEROFF}$.

Refer to Annex A.5 for the value of $t_{POWEROFF}$.

3.3 Signal Interface PCD to PICC

This section specifies the modulation methods used by Type A and Type B for the communication PCD to PICC. It deals with:

- The data transmission characteristics of the PCD
- The reception capabilities of the PICC to interpret the data transmission of the PCD

3.3.1 Introduction

The ISO/IEC 14443 standard defines two possible modulation types, called Type A and Type B. For communication from PCD to PICC, both Type A and Type B use Amplitude Shift Keying (ASK). The amplitude of the carrier is switched between V_1 and V_2 , creating a lower level when the field is at value V_2 . The requirements of the lower level as well as of the envelope of the carrier for the two modulation types of ISO/IEC 14443 are defined in this section.

All measurements described in this section are performed with the EMV – TEST PCD and the EMV – TEST PICCs calibrated as specified in [PCD MANUAL] and [PICC MANUAL]. The position of a PICC within the Operating Volume is indicated according to the convention specified in Annex B.

3.3.2 PCD Requirements for Modulation PCD to PICC – Type A

Type A communication from PCD to PICC uses the modulation principle of ASK 100%. The carrier is turned on and off, creating a lower level when turned off. In practice, it will result in a modulation depth of 95% or higher. The lower level for Type A modulation is referred to as “pause” by [ISO/IEC 14443-2]. Table 3.14 describes how to measure the Type A modulation characteristics of a PCD.

Table 3.14: Measurement of Modulation PCD to PICC – Type A (PCD Transmission)

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in the Operating Volume of the PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with LLZ.
Step 2	Send Type A frames by means of the PCD Test Environment.
Step 3	Capture the Type A frames sent by the PCD at the output of the pickup coil (J9) of the EMV – TEST PICC 1 and analyze the modulation characteristics.
Step 4	Repeat Step 1 to Step 3 with EMV – TEST PICC 1 configured with HLZ.
Step 5	Repeat Step 1 to Step 4 with EMV – TEST PICC 2 and EMV – TEST PICC 3.

For this section, V represents the envelope of the signal measured at the output of the pickup coil (J9) of the EMV – TEST PICC, placed in the Operating Volume of the PCD. V_1 is the level measured immediately before the falling edge preceding a lower level of modulation from the PCD. The V_1 level is defined afresh for each lower level of the modulation.

V_2 , V_3 and V_4 are defined as follows:

$$V_2 = 0.05V_1$$

$$V_3 = 0.6V_1$$

$$V_4 = 0.9V_1$$

The falling edge is that part of the envelope V, where V decreases from V_4 to V_2 . The rising edge is that part of the envelope V, where V increases from V_2 to V_4 .

Requirements 3.10: Modulation PCD to PICC – Type A (PCD Transmission)

PCD

3.3.2.1 The PCD shall modulate the Operating Field in the Operating Volume in such a way that the signal measured at the output of the pickup coil (J9) of the EMV – TEST PICC has the following characteristics (see also Figure 3.1):

- The time between V_4 of the falling edge and V_2 of the rising edge shall be t_1 .
- If V does not decrease monotonically from V_4 to V_2 , the time between a local maximum and the time of passing the same value before the local maximum shall be t_5 . This shall only apply if the local maximum is greater than V_2 .
- V shall remain less than V_2 for a time t_2 .
- V shall increase monotonically to V_3 in a time t_4 .
- V shall increase monotonically to V_4 in a time t_3 .

The modulation characteristics shall be measured as described in Table 3.14.

Refer to Annex A.2 for the values of t_1 , t_2 , t_3 , t_4 and t_5 .

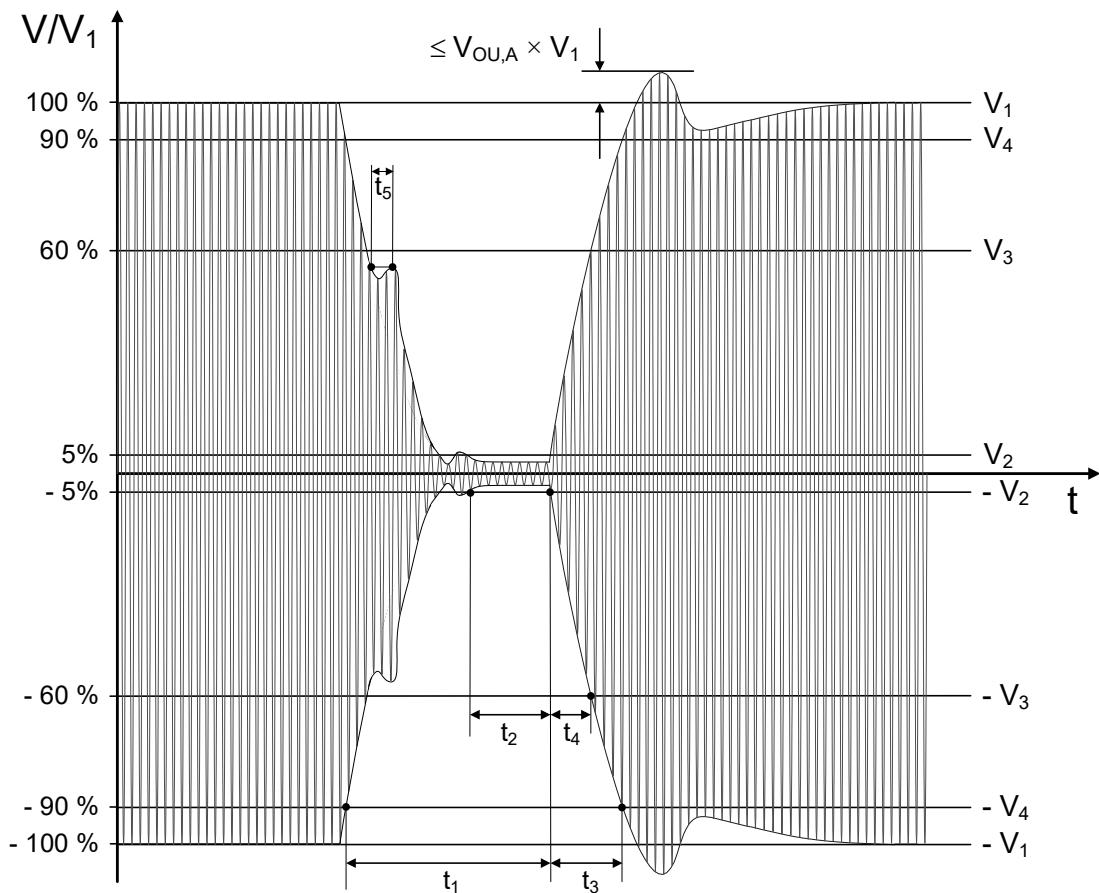
3.3.2.2 The PCD shall modulate the Operating Field in the Operating Volume in such a way that the signal measured at the output of the pickup coil (J9) of the EMV – TEST PICC has the following characteristics (see also Figure 3.1):

- Ringing following the falling edge shall remain below $V_{ou,A}V_1$.
- Overshoots immediately following the rising edge shall remain within $(1 \pm V_{ou,A})V_1$.

The modulation characteristics shall be measured as described in Table 3.14.

Refer to Annex A.2 for the value of $V_{ou,A}$.

Figure 3.1: Lower Level – Type A



3.3.3 PICC Requirements for Modulation PCD to PICC – Type A

This section lists the requirements for the reception capabilities of a PICC of Type A. Table 3.15 describes the measurement procedure that verifies whether a PICC functions properly with the EMV – TEST PCD that applies Type A modulation characteristics at the border of the tolerance interval.

Table 3.15: Measurement of Modulation PCD to PICC – Type A (PICC Reception)

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ. Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ within the range specified in Annex A.3 at J1 of the EMV – TEST PICC 1.
Step 2	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with LLZ.
Step 3	Modulate the carrier to obtain modulation characteristics $t_{s,1}$, $t_{s,2}$, $t_{s,3}$ and $t_{s,4}$ to the extremes of the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 4	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD.
Step 5	Place the PICC in the Operating Volume of the EMV – TEST PCD and verify whether the PICC functions properly.

Requirements 3.11: Modulation PCD to PICC – Type A (PICC Reception)

PICC

- 3.3.3.1 When placed in the Operating Volume of the EMV – TEST PCD, a PICC of Type A shall function properly provided the EMV – TEST PCD has been set up as described in Table 3.15.
-

3.3.4 PCD Requirements for Modulation PCD to PICC – Type B

Type B communication from PCD to PICC uses the modulation principle of ASK 10%. The amplitude of the carrier is reduced to create a lower level with a modulation index m_i . The requirements on the lower level as well as on the envelope of the carrier are defined below. Table 3.16 describes how to measure the Type B modulation characteristics of a PCD.

Table 3.16: Measurement of Modulation PCD to PICC – Type B (PCD Transmission)

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in the Operating Volume of the PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with LLZ.
Step 2	Send Type B frames by means of the PCD Test Environment.
Step 3	Capture the Type B frames sent by the PCD at the output of the pickup coil (J9) of the EMV – TEST PICC 1 and analyze the modulation characteristics.
Step 4	Repeat Step 1 to Step 3 with EMV – TEST PICC 1 configured with HLZ.
Step 5	Repeat Step 1 to Step 4 with EMV – TEST PICC 2 and EMV – TEST PICC 3.

For this section, V represents the envelope of the signal measured at the output of the pickup coil (J9) of the EMV – TEST PICC, placed in the Operating Volume of the PCD.

V_1 is the level measured immediately before the falling edge preceding a lower level of modulation from the PCD. V_2 is the level measured immediately before the rising edge that follows the lower level. The V_1 and V_2 levels are defined afresh for each lower level of modulation.

The modulation index (m_i), V_3 and V_4 are defined as follows:

$$m_i = \frac{V_1 - V_2}{V_1 + V_2}$$

$$V_3 = V_1 - 0.1(V_1 - V_2)$$

$$V_4 = V_2 + 0.1(V_1 - V_2)$$

Requirements 3.12: Modulation PCD to PICC – Type B (PCD Transmission)

PCD

3.3.4.1 The PCD shall modulate the Operating Field in the Operating Volume in such a way that the signal measured at the output of the pickup coil (J9) of the EMV – TEST PICC has the following characteristics (see also Figure 3.2):

- The modulation index (m_i) of the signal shall be mod_i .
- V shall decrease monotonically from V_3 to V_4 (i.e. the falling edge) in a time t_f .
- V shall increase monotonically from V_4 to V_3 (i.e. the rising edge) in a time t_r .
- The rising and falling edges of the modulation shall be monotonic.

The modulation characteristics shall be measured as described in Table 3.16.

Refer to Annex A.2 for the values of mod_i , t_f and t_r .

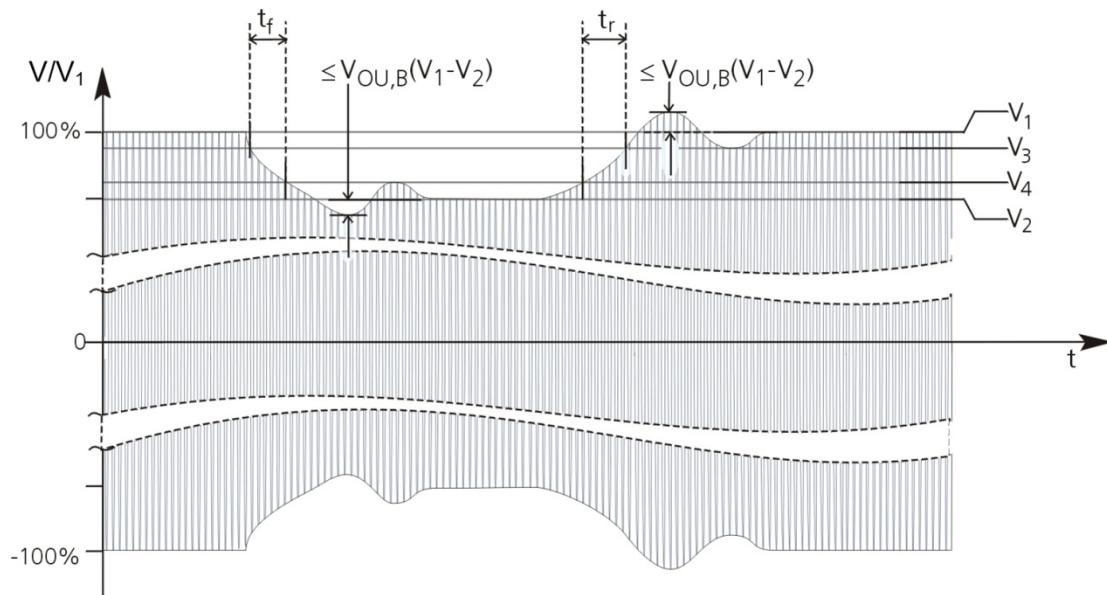
3.3.4.2 The PCD shall modulate the Operating Field in the Operating Volume in such a way that the signal measured at the output of the pickup coil (J9) of the EMV – TEST PICC has the following characteristics (see also Figure 3.2):

- Overshoots and undershoots immediately following the falling or rising edges shall be less than $V_{ou,B}(V_1-V_2)$.

The modulation characteristics shall be measured as described in Table 3.16.

Refer to Annex A.2 for the value $V_{ou,B}$.

Figure 3.2: Modulation PCD to PICC – Type B



3.3.5 PICC Requirements for Modulation PCD to PICC – Type B

This section lists the requirements for the reception capabilities of a PICC of Type B. Table 3.17 describes the measurement procedure that verifies whether a PICC functions properly with the EMV – TEST PCD that applies Type B modulation characteristics at the border of the tolerance interval.

Table 3.17: Measurement of PCD to PICC Modulation – Type B (PICC Reception)

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ. Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov}$ within the range specified in Annex A.3 at J1 of the EMV – TEST PICC 1.
Step 2	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with LLZ.
Step 3	Modulate the carrier to obtain modulation characteristics $m_{s1,i}$, $t_{s,f}$ and $t_{s,r}$ to the extremes of the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 4	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD.
Step 5	Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $0 \leq z < 2$ cm and verify whether the PICC functions properly.
Step 6	Remove the PICC from the Operating Volume of the EMV – TEST PCD. Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with LLZ.

Step #	Action
Step 7	Modulate the carrier to obtain modulation characteristics $m_{s2,i}$, $t_{s,f}$ and $t_{s,r}$ to the extremes of the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 8	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD.
Step 9	Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $2 \leq z < 3$ cm and verify whether the PICC functions properly.
Step 10	Remove the PICC from the Operating Volume of the EMV – TEST PCD. Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with LLZ.
Step 11	Modulate the carrier to obtain modulation characteristics $m_{s3,i}$, $t_{s,f}$ and $t_{s,r}$ to the extremes of the range specified in Annex A.3. The modulation characteristics are measured at J9 of the EMV – TEST PICC 1.
Step 12	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD.
Step 13	Place the PICC in the Operating Volume of the EMV – TEST PCD in a position with $3 \leq z \leq 4$ cm and verify whether the PICC functions properly.

Requirements 3.13: Modulation PCD to PICC – Type B (PICC Reception)**PICC**

- 3.3.5.1 When placed in the Operating Volume of the EMV – TEST PCD, a PICC of Type B shall function properly, provided the EMV – TEST PCD has been set up as described in Table 3.17.

3.4 Signal Interface PICC to PCD

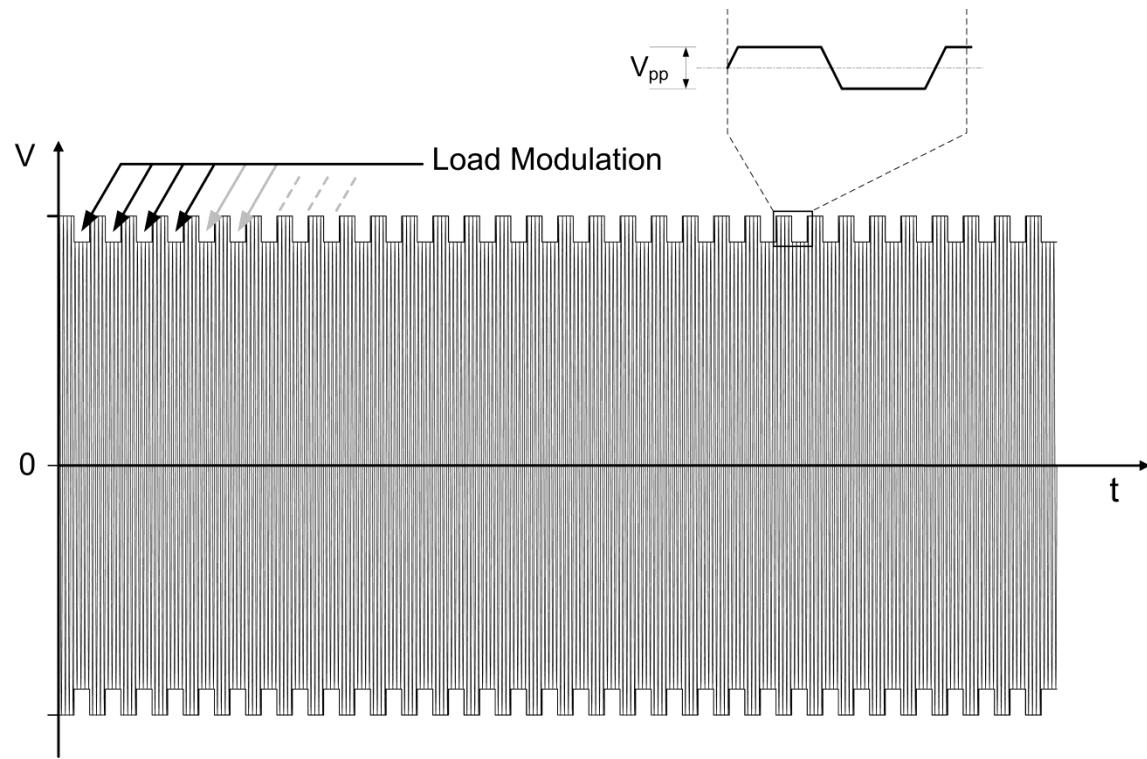
This section specifies the modulation methods used by Type A and Type B for the communication PICC to PCD. It deals with:

- The data transmission characteristics of the PICC
- The reception capabilities of the PCD to interpret the data transmission of the PICC

3.4.1 Introduction

For the communication from PICC to PCD, both Type A and Type B use load modulation as shown in Figure 3.3. The carrier frequency f_c is used to derive a subcarrier with frequency f_s equal to $f_c/16$ (~847 kHz). Switching a load on and off at this frequency creates the subcarrier causing a different current to flow through the antenna of the PICC when in the loaded state than when in the unloaded state (the unloaded state of the subcarrier is the stable state when the PICC is not sending bits). This difference in current in the PICC antenna is sensed by the PCD.

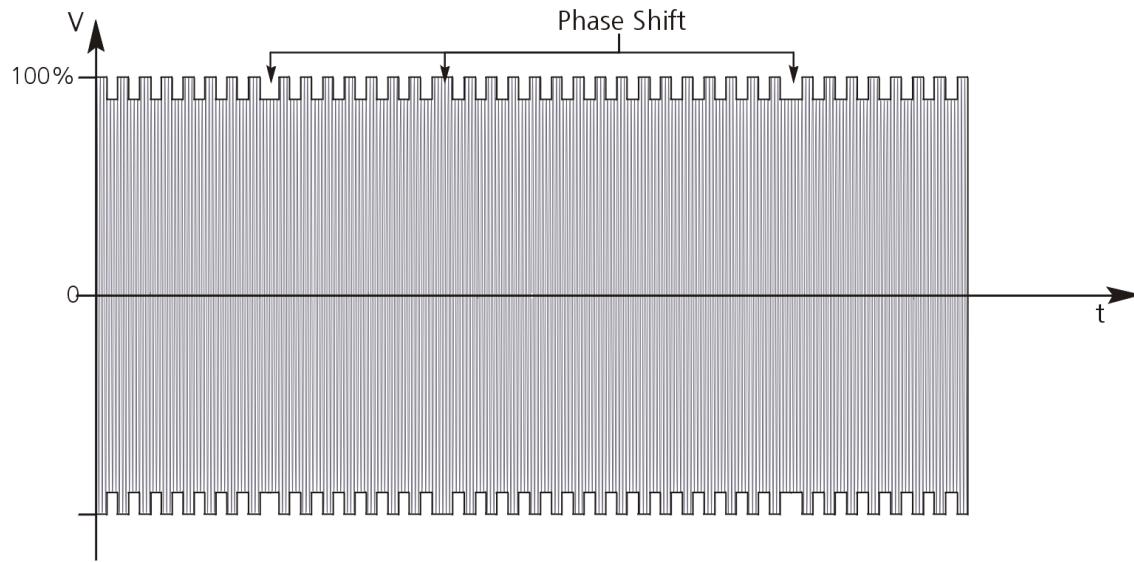
Figure 3.3: Load Modulation



Type A modulates the subcarrier using On-Off Keying (OOK).

Type B modulates the subcarrier using Binary Phase Shift Keying (BPSK) as shown in Figure 3.4. BPSK uses two signal phases: 0 degrees and 180 degrees. If the phase of the wave does not change with regard to a reference phase, then the signal state stays the same (low or high). If the phase of the wave changes by 180 degrees (i.e. the phase reverses) then the signal state changes. The reference phase is referred to as $\emptyset 0$.

Figure 3.4: BPSK



Note that, although this specification mainly considers load modulation on a purely amplitude basis, in reality the load modulation produced by a PICC has a mixture of amplitude and phase modulation components and consequently this specification also contains requirements that PCDs are able to receive load modulation signals that are comprised of a mixture of amplitude and phase modulation components, e.g. by using IQ demodulation.

All measurements described in this section are performed with the EMV – TEST PCD and the EMV – TEST PICCs calibrated as specified in [PCD MANUAL] and [PICC MANUAL]. The position of a PICC within the Operating Volume is indicated according to the convention specified in Annex B.

3.4.2 PICC Requirements for Load Modulation

This section lists the load modulation requirements for the PICC. Table 3.18 describes how to measure the load modulation characteristics of a PICC.

**Table 3.18: Measurement of Load Modulation Characteristics
(PICC Transmission)**

Step #	Action
Step 1	Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ. Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov,LM}$ at J1 of the EMV – TEST PICC 1. Refer to Annex A.3 for the value of $V_{s,ov,LM}$.
Step 2	Configure EMV – TEST PICC 1 with LLZ. Set up the EMV – TEST PCD to obtain modulation characteristics as specified in Annex A.3.
Step 3	Remove the EMV – TEST PICC 1 from the Operating Volume of the EMV – TEST PCD. Place the PICC in the Operating Volume of the EMV – TEST PCD.
Step 4	Send Type A frames appropriate to the state of the PICC to a PICC of Type A or Type B frames appropriate to the state of the PICC to a PICC of Type B.
Step 5	Capture the response from the PICC at J2 of the EMV – TEST PCD and measure the load modulation (V_{pp}) with the EMV – TEST CMR.

Requirements 3.14: Load Modulation Characteristics (PICC Transmission)

PICC

3.4.2.1 When put in the Operating Volume of the EMV – TEST PCD, the PICC shall modulate the Operating Field in such a way that the signal measured as described in Table 3.18 has the following characteristics:

- The frequency f_s of the signal shall be $f_c/16$.
- The amplitude (V_{pp}) of the signal shall be V_{pp} (peak to peak).

Refer to Annex A.2 for the value of V_{pp} .

3.4.3 PICC Requirements for Subcarrier Modulation – Type A

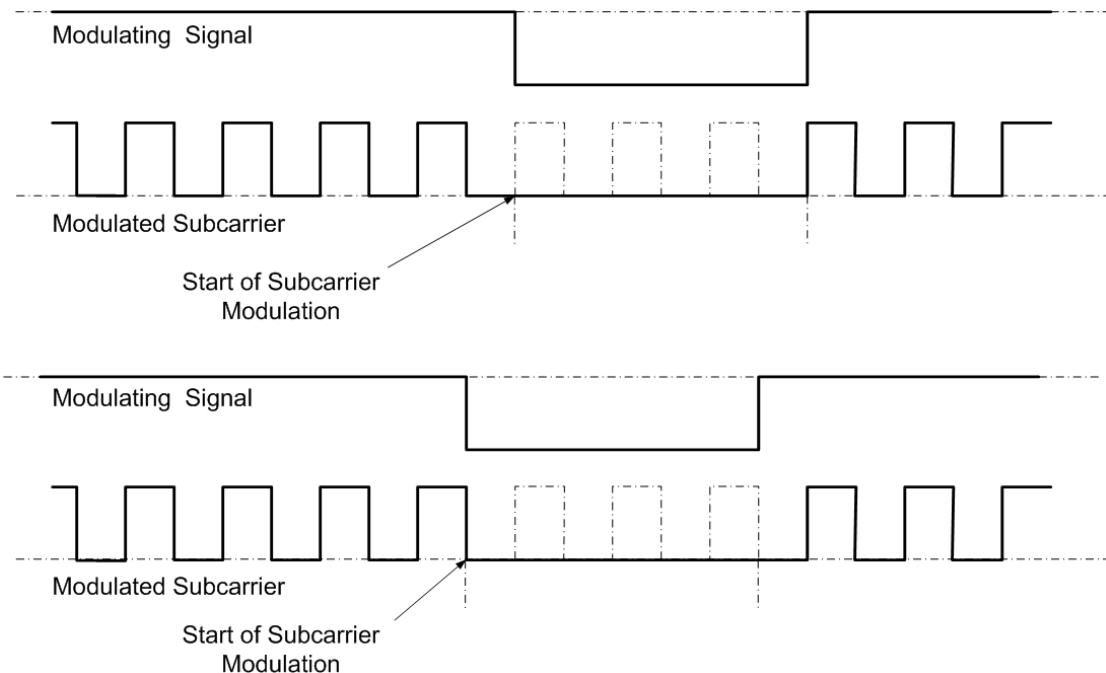
This section lists the PICC requirements for the modulation of the subcarrier for the communication from PICC to PCD for Type A.

Requirements 3.15: Subcarrier Modulation – Type A (PICC Transmission)

PICC

- 3.4.3.1 A PICC of Type A shall modulate the subcarrier using On-Off Keying (OOK).
- 3.4.3.2 When modulating the subcarrier, a PICC of Type A shall only start the modulation with a defined phase relation to the subcarrier: that is, on the rising or falling edge of the subcarrier (see Figure 3.5).

Figure 3.5: Start of Subcarrier Modulation – Type A



3.4.4 PICC Requirements for Subcarrier Modulation – Type B

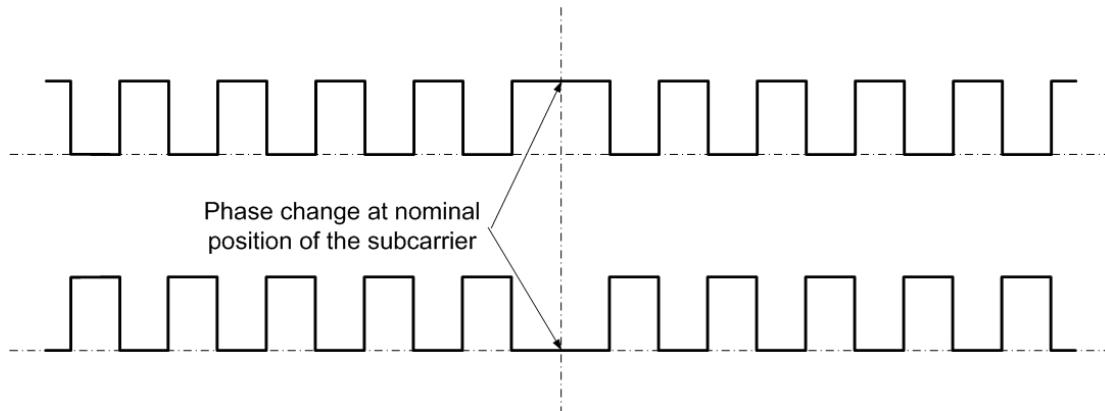
A PICC of Type B modulates the subcarrier using BPSK. Before the PICC sends information to the PCD by means of phase shifts, PICC and PCD first establish a reference phase ϕ_0 . Then the PICC can start modulating the subcarrier: a change of logic level is denoted by a phase shift of 180° of the subcarrier.

Requirements 3.16: Subcarrier Modulation – Type B (PICC Transmission)

PICC

- 3.4.4.1 A PICC of Type B shall modulate the subcarrier using BPSK.
- 3.4.4.2 A PICC of Type B shall generate a subcarrier only when data is to be transmitted.
- 3.4.4.3 Phase shifts shall only occur at nominal positions of rising or falling edges of the subcarrier (refer to Figure 3.6).

Figure 3.6: Allowed Phase Shifts – Type B



3.4.5 PCD Requirements for Modulation PICC to PCD

This section lists the requirements for the reception capabilities of a PCD to interpret the modulation applied by the PICC. Table 3.19 describes the measurement procedure that verifies whether a PCD functions properly with the EMV – TEST PICCs that apply modulation characteristics at the border of the tolerance interval.

Table 3.19: Measurement of Modulation PICC to PCD (PCD Reception)

Step #	Action
Step 1	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.</p> <p>Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov,Lm}$ at J1 of the EMV – TEST PICC 1.</p> <p>Refer to Annex A.3 for the value of $V_{s,ov,Lm}$.</p>
Step 2	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=0$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Configure the EMV – TEST PICC 1 with NLZ.</p>
Step 3	<p>Connect a square wave generator to J2 of the EMV – TEST PICC 1 with a frequency of 847 kHz ($f_c/16$). Regulate in such a way that the square wave modulates the carrier with amplitude $V_{s1,pp}$ (peak to peak) with positive sense (where the loaded state causes an increase in the observed voltage) measured at J2 of the EMV – TEST PCD with the EMV – TEST CMR.</p> <p>Refer to Annex A.3 for the value of $V_{s1,pp}$.</p>
Step 4	<p>Place the EMV – TEST PICC 1 in the Operating Volume of the PCD in a position with $0 \leq z \leq 2$ cm.</p>
Step 5	<p>Request the PCD to send a valid command to the EMV – TEST PICC 1 by means of the PCD Test Environment. Return a correct response by means of the EMV – TEST PICC 1 and verify if the PCD functions properly. Perform the measurement for Type A and Type B.</p>
Step 6	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Configure the EMV – TEST PICC 1 with NLZ.</p>

Step #	Action
Step 7	Connect a square wave generator to J2 of the EMV – TEST PICC 1 with a frequency of 847 kHz ($f_c/16$). Regulate in such a way that the square wave modulates the carrier with amplitude $V_{S2,pp}$ (peak to peak) with positive sense measured at J2 of the EMV – TEST PCD with the EMV – TEST CMR. Refer to Annex A.3 for the value of $V_{S2,pp}$.
Step 8	Place the EMV – TEST PICC 1 in the Operating Volume of the PCD in a position with $2 < z \leq 4$ cm.
Step 9	Request the PCD to send a valid command to the EMV – TEST PICC 1 by means of the PCD Test Environment. Return a correct response by means of the EMV – TEST PICC 1 and verify if the PCD functions properly. Perform the measurement for Type A and Type B.
Step 10	Repeat steps 2 to 9 but in steps 3 and 7 regulate the square wave generator connected to J2 of the EMV – TEST PICC 1 in such a way that the square wave modulates the carrier with negative sense (where the loaded state causes a decrease in the observed voltage).
Step 11	Repeat Step 2 to Step 10 with EMV – TEST PICC 2 and EMV – TEST PICC 3.

Requirements 3.17: Modulation PICC to PCD (PCD Reception)**PCD**

- 3.4.5.1 The PCD shall function properly with the EMV – TEST PICCs provided the EMV – TEST PICCs have been set up as described in Table 3.19.

3.5 IQ Demodulation

3.5.1 Introduction

Requirements in section 3.4 consider load modulation on a purely amplitude basis. In reality the load modulation produced by a PICC has a mixture of amplitude and phase modulation components and consequently, for successful operation, PCDs must be able to receive load modulation signals that are comprised of a mixture of amplitude and phase modulation components, e.g. by using IQ demodulation methods.

3.5.2 PCD Requirements for IQ Demodulation

This section lists the requirements for the reception capabilities of a PCD to interpret IQ modulated load modulation applied by the PICC. Table 3.20 describes the measurement procedure that verifies whether a PCD functions properly with the IQ TEST PICC that applies load modulation comprised of a mixture of amplitude and phase modulation components.

The modulation angle defined by the phase relationship between the carrier frequency f_c and the lower and upper sideband frequencies ($f_c - f_s$) and ($f_c + f_s$) for the subcarrier frequency f_s is designated Φ_{LM} . Upon synchronisation the modulation angle of the phase relationship at the start of a frame is designated $\Phi_{LM,INIT}$.

Table 3.20: Measurement of IQ Modulation PICC to PCD (PCD Reception)

Step #	Action
Step 1	<p>Place the EMV – TEST PICC 1 in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Apply no modulation to J2 of the EMV – TEST PICC 1. Configure the EMV – TEST PICC 1 with NLZ.</p> <p>Connect input J1 of the EMV – TEST PCD with a signal generator V generating a carrier signal with frequency $f_{s,c}$ within the range specified in Annex A.3. Regulate the signal generator V in such a way that it generates a mean voltage $V_{s,ov,LM}$ at J1 of the EMV – TEST PICC 1.</p> <p>Refer to Annex A.3 for the value of $V_{s,ov,LM}$.</p>

Step #	Action
Step 2	Place the IQ TEST PICC in position ($r=0$, $\varphi=0$, $z=2$, $\theta=0$) of the Operating Volume of the EMV – TEST PCD. Adjust the load modulation such that when measured at J2 of the EMV – TEST PCD: <ul style="list-style-type: none">• The sidebands ($f_c - f_s$) and ($f_c + f_s$) have amplitudes such that the difference in amplitude is not more than 20%• Φ_{LM} is set to $\Phi_{LM,INIT}$ optimised to maximise the amplitude V_{pp} of the load modulation when measured on a purely amplitude basis• The amplitude of V_{pp} is $V_{S2,pp,IQ}$ (peak to peak) Refer to Annex A.3 for the value of $V_{S2,pp,IQ}$
Step 3	Place the IQ TEST PICC in the Operating Volume of the PCD in a position with $2 < z \leq 4$ cm.
Step 4	Request the PCD to send a valid command to the IQ TEST PICC by means of the PCD Test Environment. Return a correct response by means of the IQ TEST PICC with Φ_{LM} in the range between 0° and 360° and verify if the PCD functions properly.
Step 5	Repeat steps 2 to 4 for Type A and Type B.

Requirements 3.18: IQ Modulation PICC to PCD (PCD Reception)**PCD**

3.5.2.1 The PCD shall function properly with the IQ TEST PICC provided the IQ TEST PICC has been set up as described in Table 3.20.

4 Sequences and Frames

This chapter describes the protocol layers sequence and frame. It specifies the coding techniques used for establishing the symbol alphabets and bit level coding.

4.1 Introduction

4.1.1 Sequence

An incoming signal, being valid according to this specification, is named a sequence. A receiving device needs information how to recognize a sequence to be demodulated and when to begin and stop demodulation. Furthermore, if a phase modulation method is applied, then it is necessary to establish a common phase reference between sender and receiver, i.e. sender and receiver are synchronized.

As a result, depending on the technology (Type A or Type B) a sequence optionally starts with a specific wave pattern, named Start of Sequence (SoS), and optionally ends with a specific wave pattern, named End of Sequence (EoS).

SoS and EoS help the receiving device to synchronize with the sender and to identify a valid sequence, and therefore, allow to extract information included in the sequence. The information transported in a sequence is a collection of bits included in a frame, as specified in section 4.7.

4.1.2 Frames

Data transmitted between PCD and PICC is grouped within frames. The format of a frame is different for Type A and Type B.

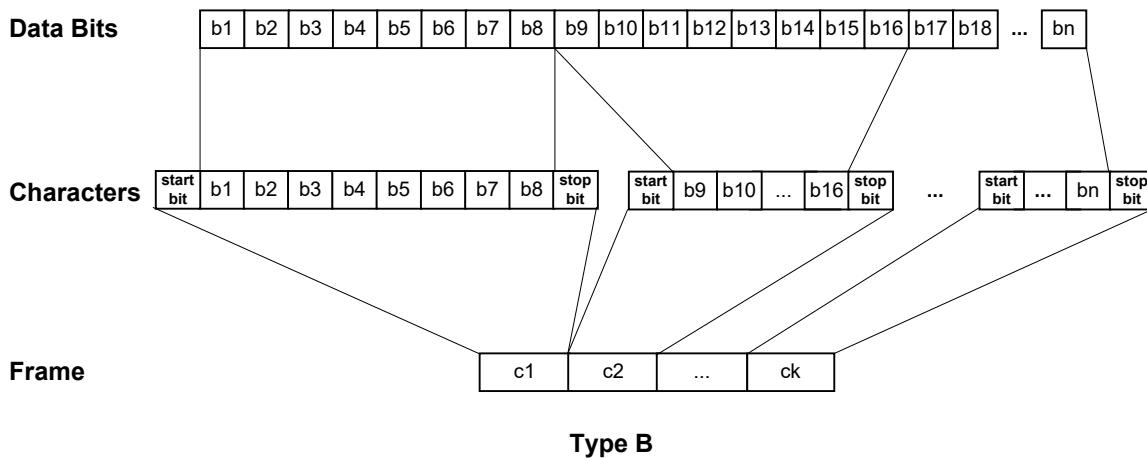
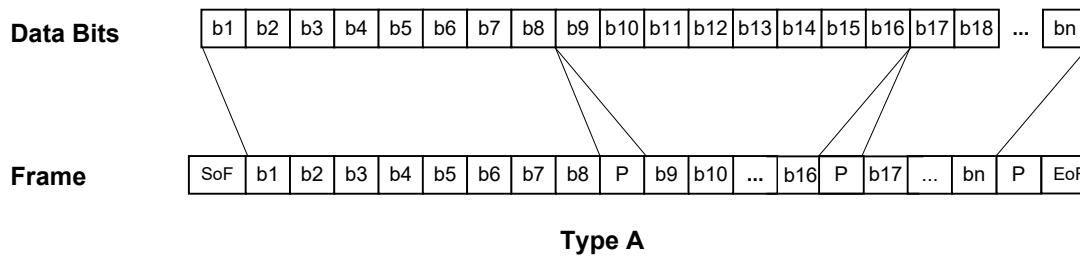
Type A groups data bits together in a frame by adding a Start of Frame (SoF), an End of Frame (EoF) and a parity bit (P) to the end of each data byte (= 8 data bits) (except for the short frames). EoF is only used for PCD to PICC communication. Type A does not use EoF for PICC to PCD communication.

Type B is a character based protocol and groups data bytes (= 8 data bits) first together in characters. A character consists of a start bit, 8 data bits, and a stop bit. The characters are then transmitted as frames. Type-B does not use SoF or EoF.

Both protocols assume data is encoded in bytes (i.e. the number of data bits is a multiple of 8) and transmit data bits LSB (or b1) first. The commands and data further on in this specification are however defined in the conventional manner, with MSB (or b8) on the left and LSB (or b1) on the right. Bytes are numbered in the opposite order: Byte 1 is the leftmost or most significant byte. Bytes are transferred most significant byte first.

Figure 4.1 illustrates the Type A and the Type B frame format.

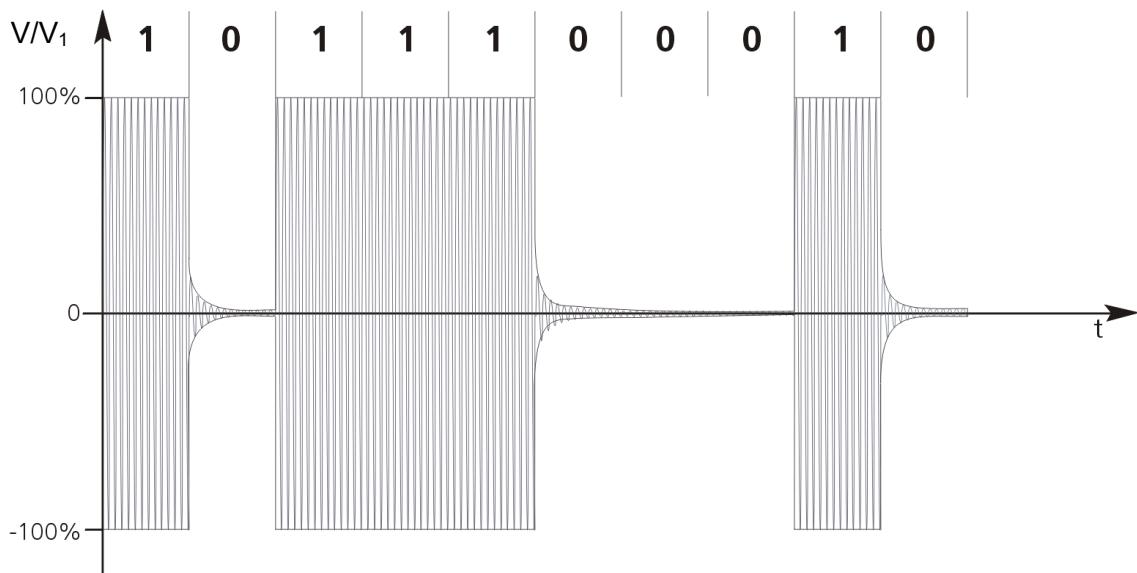
Figure 4.1: Frame Format for Type A and Type B



4.1.3 Coding Schemes

In digital communication systems, digital data is converted into transmittable symbols. Typically, these symbols are made out of trains of pulses (or lower levels). The most obvious way to transmit data is to turn the sender's switch on to send a 1 and off to send a 0. This coding scheme is called On-Off-Keying (OOK).

Figure 4.2: On-Off-Keying

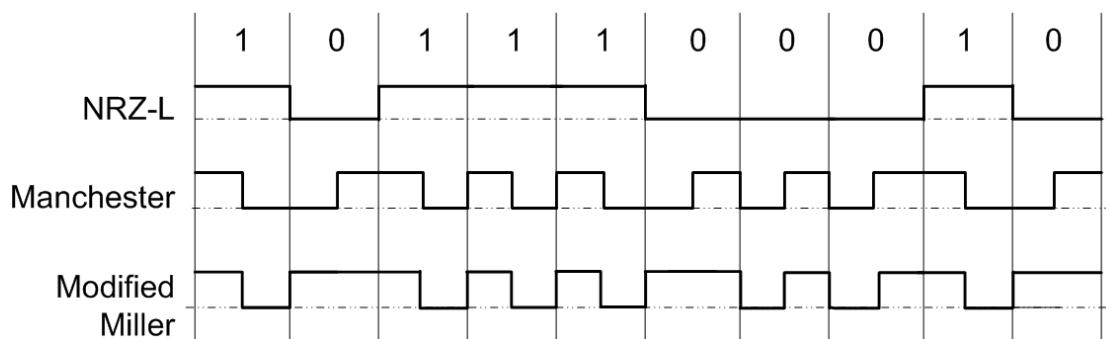


Because of the difficulty in determining the difference between a zero bit and the transmitter actually switching off, the data signal needs some additional rules. The coding methods used in this specification are:

- NRZ-L code
- Manchester code
- Modified Miller code

Examples of NRZ-L, Manchester and Modified Miller are shown in Figure 4.3.

Figure 4.3: Coding Schemes



Type A and Type B use different coding schemes. Table 4.1 gives an overview of the different coding schemes.

Table 4.1: Overview of Coding Schemes

Communication	Type A	Type B
PCD→PICC	Modified Miller	NRZ-L
PICC→PCD	Manchester	NRZ-L

4.2 Bit Rate

The timing of a digital signal is indicated by means of elementary time units (etu). For this specification, 1 etu equals one bit period, i.e. the time to transmit one unit of information.

For communication PCD → PICC, the etu is defined as follows:

$$1 \text{ etu} = 128 / (f_c \times D_{\text{PCD} \rightarrow \text{PICC}})$$

For communication PICC → PCD, the etu is defined as follows:

$$1 \text{ etu} = 8 / (f_s \times D_{\text{PICC} \rightarrow \text{PCD}})$$

where f_c is the frequency of the carrier generated by the PCD and f_s is the frequency of the subcarrier generated by the PICC (see Chapter 3). The initial value of the divisors $D_{\text{PCD} \rightarrow \text{PICC}}$ and $D_{\text{PICC} \rightarrow \text{PCD}}$ is 1, giving an initial bit rate of 106 kbit/s. The initial etu is defined as follows:

$$1 \text{ etu} = 128 / f_c = 8 / f_s$$

Requirements 4.1: Bit Rate

PCD and PICC

- 4.2.1.1 For this version of the specification, the bit rate for the communication shall be $f_c/128$ (~106 kbit/s) in both directions (i.e. $D_{\text{PCD} \rightarrow \text{PICC}} = D_{\text{PICC} \rightarrow \text{PCD}} = 1$).
-

4.3 Synchronization

4.3.1 Type A – Synchronization

Type A does not have a synchronization sequence. For PCD to PICC communication Type A uses 100% ASK. The lower level is a sufficient trigger to start the demodulation and to indicate the start of the first symbol.

For PICC to PCD communication, the communication is synchronous and grid aligned. The start of a sequence is determined by counting the number of carrier cycles elapsed since the last lower level of the command.

4.3.2 Type B – Synchronization

Figure 4.4 shows the start of the PICC response sequence after the end of a PCD command sequence.

Figure 4.4: PICC Start of Sequence

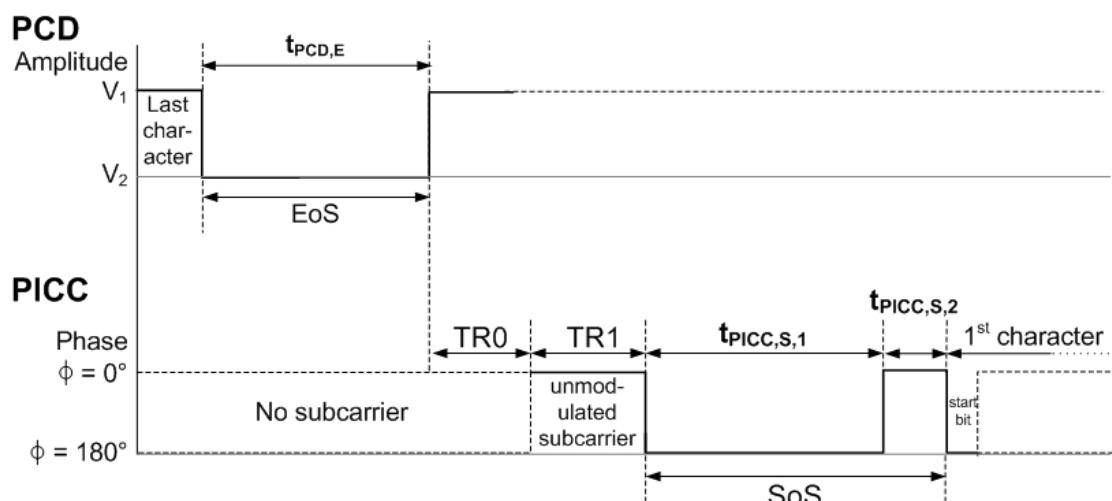
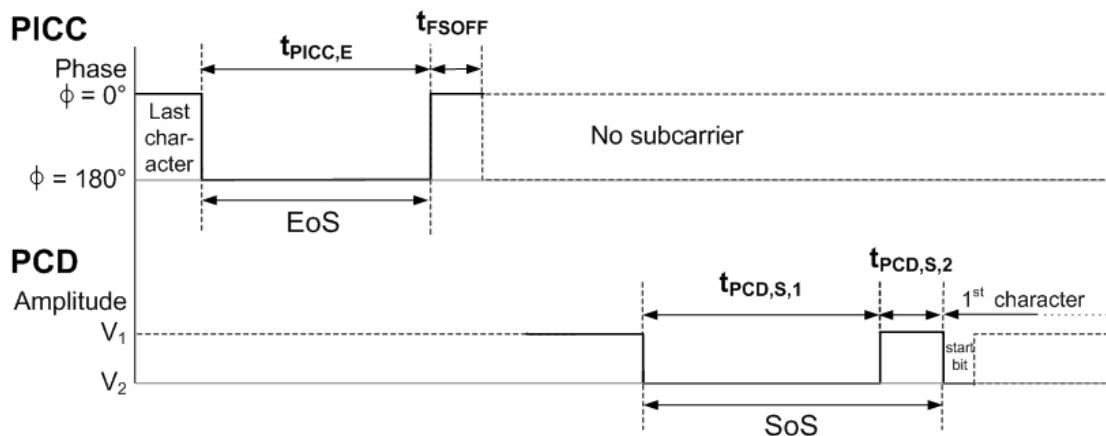


Figure 4.5 shows the start of a new PCD command sequence after the end of a PICC response sequence.

Figure 4.5: PCD Start of Sequence



Requirements 4.2: Synchronization PCD → PICC – Type B

PCD	PICC
<p>4.3.2.1 The PCD shall code SoS as follows:</p> <ul style="list-style-type: none"> • $t_{PCD,S,1}$ with carrier low (modulation applied), followed by $t_{PCD,S,2}$ with carrier high (no modulation applied) <p>Refer to Annex A.4 for the values of $t_{PCD,S,1}$ and $t_{PCD,S,2}$.</p>	<p>4.3.2.2 The PICC shall decode SoS as follows:</p> <ul style="list-style-type: none"> • If the carrier is low (modulation applied) for $t_{PCD,S,1}$, followed by $t_{PCD,S,2}$ with carrier high (no modulation applied), then the PICC shall decode that as SoS.

Requirements 4.3: Synchronization PICC → PCD – Type B

PCD	PICC
<p>4.3.2.3 For establishing a phase reference \emptyset_0, the PCD shall proceed as follows:</p> <ul style="list-style-type: none"> • After any command from the PCD, the PCD shall ignore any subcarrier generated by the PICC during a time $TR0_{MIN}$. • The subcarrier as detected during $TR1$ shall be taken as phase reference \emptyset_0. <p><i>If after $TR1_{MAX}$ no phase transition is detected, then the PCD may resort to exception processing (transmission error).</i></p> <p><i>If a phase transition is detected before $TR1_{MIN}$, then the PCD may resort to exception processing (transmission error).</i></p>	<p>4.3.2.4 For establishing a phase reference \emptyset_0, the PICC shall proceed as follows:</p> <ul style="list-style-type: none"> • After any command from the PCD a minimum guard time $TR0_{MIN}$ shall apply in which the PICC shall not generate a subcarrier. <p>Refer to Annex A.4 for the value of $TR0_{MIN}$.</p> <ul style="list-style-type: none"> • Following the guard time $TR0$, the PICC shall then generate a subcarrier with no phase transition for a synchronization time $TR1$. This establishes a subcarrier phase reference \emptyset_0. <p>Refer to Annex A.4 for the minimum and maximum value of $TR1$ ($TR1_{MIN}$ and $TR1_{MAX}$).</p>

PCD	PICC
<p>4.3.2.5 If after the synchronization time TR1, the PCD detects:</p> <ul style="list-style-type: none"> • a subcarrier phase transition $\emptyset 0$ to $\emptyset 0+180^\circ$ • followed by a subcarrier with phase $\emptyset 0+180^\circ$ for $t_{PICC,S,1}$ • followed by a subcarrier phase transition $\emptyset 0+180^\circ$ to $\emptyset 0$ • followed by the subcarrier with phase $\emptyset 0$ for $t_{PICC,S,2}$ <p>then the PCD shall decode this as SoS.</p>	<p>4.3.2.6 After the synchronization time TR1, the PICC shall code the SoS as follows:</p> <ul style="list-style-type: none"> • subcarrier phase transition $\emptyset 0$ to $\emptyset 0+180^\circ$ • followed by a subcarrier with phase $\emptyset 0+180^\circ$ for $t_{PICC,S,1}$ • followed by a subcarrier phase transition $\emptyset 0+180^\circ$ to $\emptyset 0$ • followed by subcarrier with phase $\emptyset 0$ for $t_{PICC,S,2}$ <p>Refer to Annex A.4 for the values of $t_{PICC,S,1}$ and $t_{PICC,S,2}$.</p>

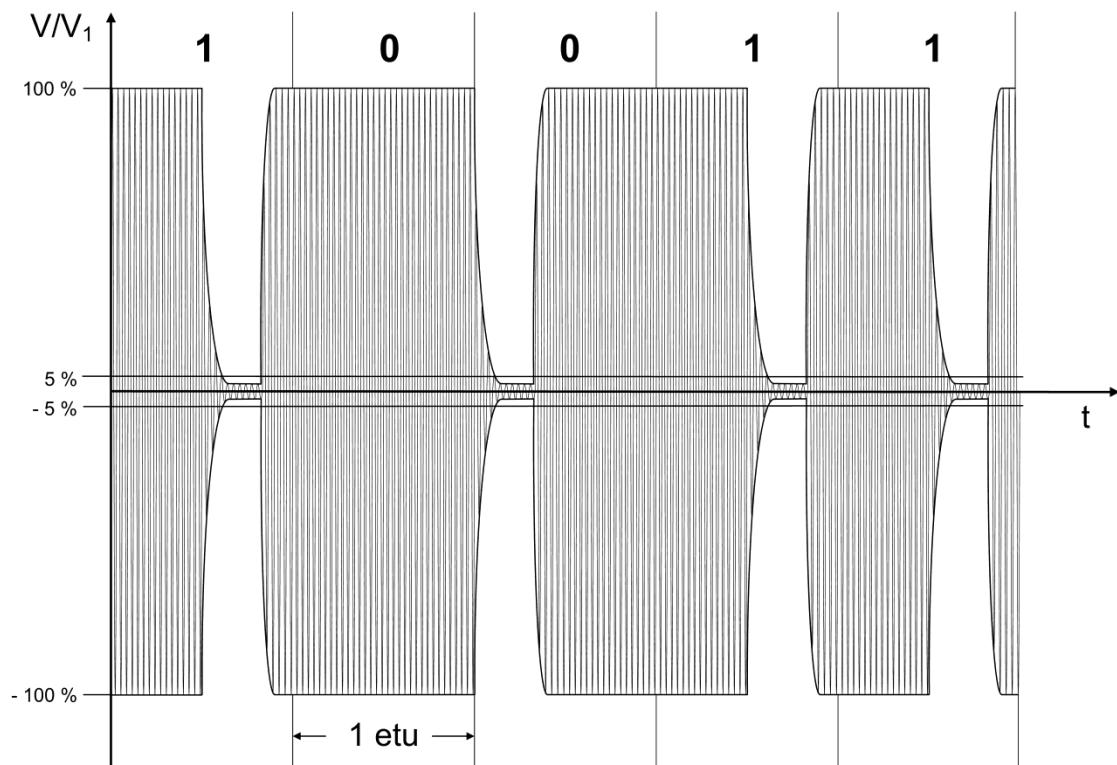
4.4 Bit Coding

This section specifies how logical values are assigned for Type A.

4.4.1 Bit Coding PCD → PICC – Type A

The bit coding used by the PCD is Modified Miller coding with ASK 100% modulation (see Figure 4.6).

Figure 4.6: Modified Miller Coding with ASK 100%



The following symbols are defined:

- Symbol X: After half the bit duration a lower level occurs.
- Symbol Y: For the full bit duration no modulation occurs.
- Symbol Z: At the beginning of the bit duration a lower level occurs.

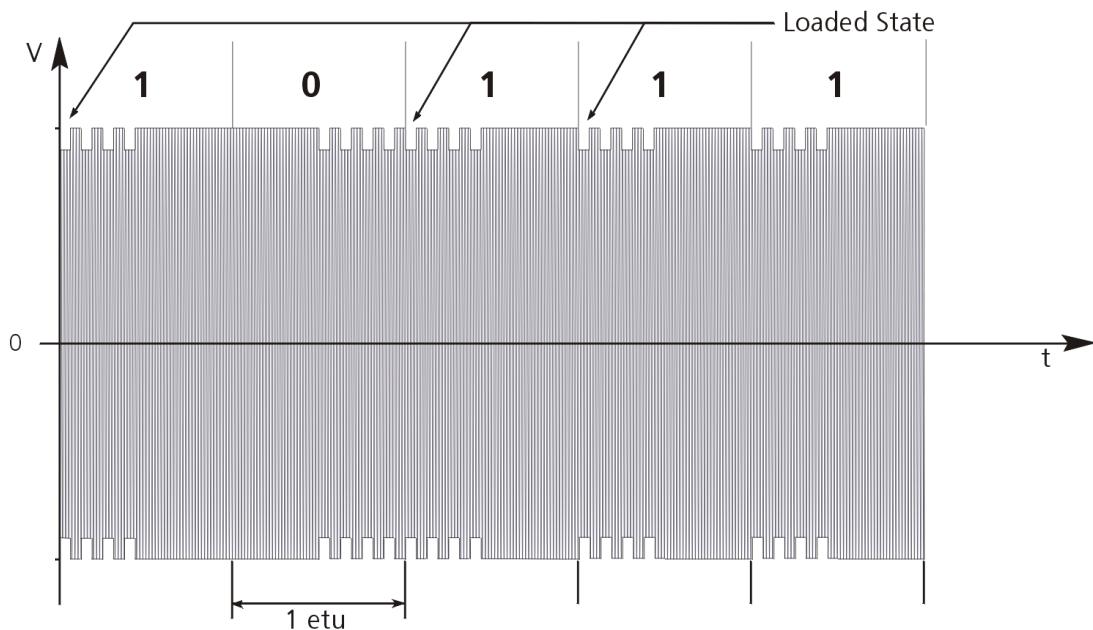
Requirements 4.4: Bit Coding PCD → PICC – Type A

PCD	PICC
<p>4.4.1.1 The PCD shall code Logic “0” and Logic “1” as follows:</p> <ul style="list-style-type: none"> • Logic “1”: symbol X • Logic “0”: symbol Y <p>with the following exceptions:</p> <ul style="list-style-type: none"> • Symbol Z shall be used to code the first Logic “0” (SoF). • If there are two or more contiguous Logic “0”s, symbol Z shall be used from the second Logic “0” on. 	<p>4.4.1.2 The PICC shall decode Logic “0” and Logic “1” as follows:</p> <ul style="list-style-type: none"> • The first symbol Z shall be decoded as Logic “0”. • If the PICC detects symbol X, then it shall decode this as Logic “1”. • If the PICC detects symbol Y after symbol X, then it shall decode this as Logic “0”. • If the PICC detects symbol Z after symbol Y, then it shall decode this as Logic “0”. • If the PICC detects symbol Z after symbol Z, then it shall decode this as Logic “0”.

4.4.2 Bit Coding PICC → PCD – Type A

The bit coding used by the PICC is Manchester coding with OOK subcarrier modulation (see Figure 4.7).

Figure 4.7: Manchester Coding with OOK



The following symbols are defined:

- Symbol D: The carrier is modulated with the subcarrier for the first half of the bit duration and is not modulated for the remaining part of the bit duration.
- Symbol E: The carrier is not modulated with the subcarrier for the first half of the bit duration and is modulated for the second half of the bit duration.
- Symbol F: The carrier is not modulated with the subcarrier for one bit duration.

Requirements 4.5: Loaded State

PCD	PICC
<p><i>If the PCD senses the carrier modulated for the first half of the bit duration and the bit period does not start with the loaded state of the subcarrier, then the PCD may resort to exception processing (transmission error). Note that the transmission error is suppressed by the EMD handling defined in section 4.9.2 if the transmission error is detected when less than 4 bytes have been received from the PICC.</i></p>	<p>4.4.2.1 If the carrier is modulated with the subcarrier for the first half of the bit duration (symbol D), then the bit period shall start with the loaded state of the subcarrier (see Figure 4.7).</p>

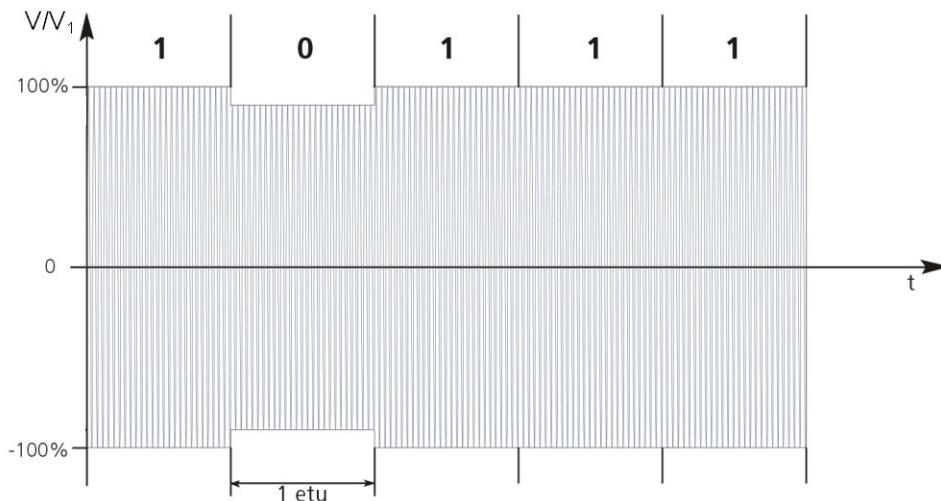
Requirements 4.6: Bit Coding PICC → PCD – Type A

PCD	PICC
<p>4.4.2.2 The PCD shall decode Logic “0” and Logic “1” as follows:</p> <ul style="list-style-type: none"> • If the PCD detects symbol D, then it shall decode this as Logic “1”. • If the PCD detects symbol E, then it shall decode this as Logic “0”. 	<p>4.4.2.3 The PICC shall code Logic “0” and Logic “1” as follows:</p> <ul style="list-style-type: none"> • Logic “1”: symbol D • Logic “0”: symbol E

4.4.3 Bit Coding PCD → PICC – Type B

The bit coding used by the PCD is NRZ-L coding with ASK 10% modulation (see Figure 4.8).

Figure 4.8: NRZ-L Coding with ASK 10%



The following symbols are defined:

Symbol L: The carrier is low (modulation applied) for the full bit duration.

Symbol H: The carrier is high (no modulation applied) for the full bit duration.

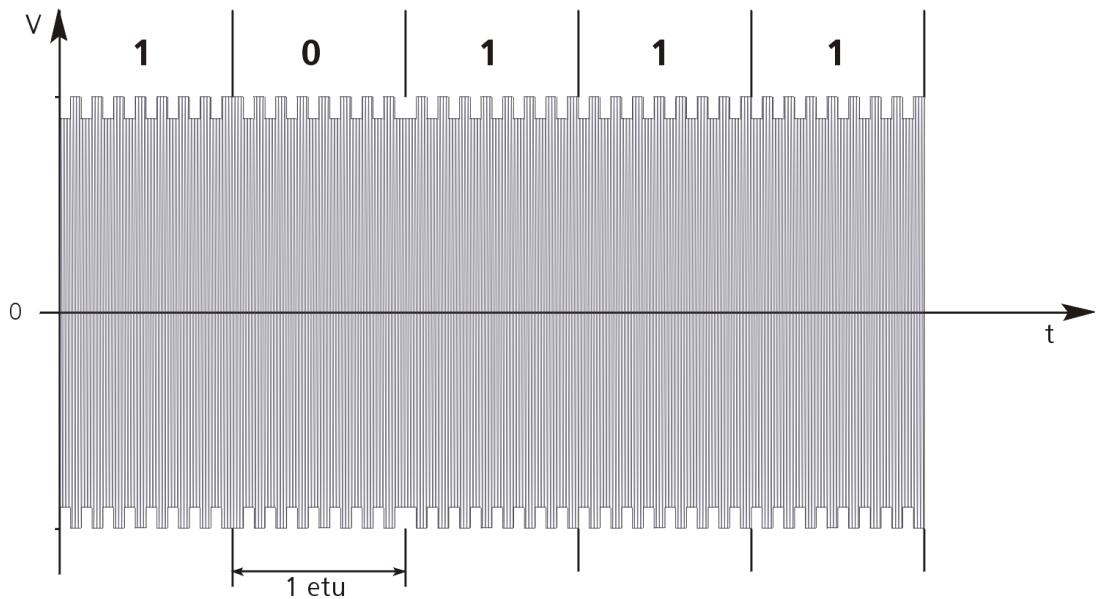
Requirements 4.7: Bit Coding PCD → PICC – Type B

PCD	PICC
<p>4.4.3.1 The PCD shall code Logic “0” and Logic “1” as follows:</p> <ul style="list-style-type: none"> • Logic “0”: symbol L • Logic “1”: symbol H 	<p>4.4.3.2 The PICC shall decode Logic “0” and Logic “1” as follows:</p> <ul style="list-style-type: none"> • If PICC detects symbol L, it shall decode this as Logic “0”. • If PICC detects symbol H, it shall decode that as Logic “1”.

4.4.4 Bit Coding PICC → PCD – Type B

Bit coding by the PICC is NRZ-L with BPSK modulation where a change of logic level is denoted by a phase shift (180°) of the subcarrier (see Figure 4.9).

Figure 4.9: NRZ-L Coding with BPSK



Requirements 4.8: Bit Coding PICC → PCD – Type B

PCD	PICC
<p>4.4.4.1 If the PCD detects:</p> <ul style="list-style-type: none"> • one of the following subcarrier phase transitions: $\emptyset 0$ to $\emptyset 0$ $\emptyset 0+180^\circ$ to $\emptyset 0$ • followed by the subcarrier with phase $\emptyset 0$ for the full bit duration <p>then the PCD shall decode this as Logic “1”.</p>	<p>4.4.4.2 The PICC shall code the following as Logic “1”:</p> <ul style="list-style-type: none"> • one of the following subcarrier phase transitions: $\emptyset 0$ to $\emptyset 0$ $\emptyset 0+180^\circ$ to $\emptyset 0$ • a subcarrier with phase $\emptyset 0$ for the full bit duration
<p>4.4.4.3 If the PCD detects:</p> <ul style="list-style-type: none"> • one of the following subcarrier phase transitions: $\emptyset 0$ to $\emptyset 0+180^\circ$ $\emptyset 0+180^\circ$ to $\emptyset 0+180^\circ$ • followed by the subcarrier with phase $\emptyset 0+180^\circ$ for the full bit duration <p>then the PCD shall decode this as Logic “0”.</p>	<p>4.4.4.4 The PICC shall code the following as Logic “0”:</p> <ul style="list-style-type: none"> • one of the following subcarrier phase transitions: $\emptyset 0$ to $\emptyset 0+180^\circ$ $\emptyset 0+180^\circ$ to $\emptyset 0+180^\circ$ • a subcarrier with phase $\emptyset 0+180^\circ$ for the full bit duration

4.5 Symbol Synchronization

Type A does not require synchronization before symbols. For Type B the separation between one character and the next is defined as the Extra Guard Time (EGT).

Requirements 4.9: Type B Character Separation

PCD and PICC

- 4.5.1.1 The time between 2 consecutive characters sent by the PCD to the PICC shall be EGT_{PCD} .

Refer to Annex A.4 for the value of EGT_{PCD} .

- 4.5.1.2 The time between 2 consecutive characters sent by the PICC to the PCD shall be EGT_{PICC} .

Refer to Annex A.4 for the value of EGT_{PICC} .

The separation between two bits within a character occurs according to the following requirements:

Requirements 4.10: Type B Bit Boundaries PCD to PICC

PCD	PICC
4.5.1.3 The PCD shall apply bit boundaries within a character between $n \text{ etu} - 4/f_c$ and $n \text{ etu} + 4/f_c$. Where n is the number of bit boundaries after the start bit falling edge ($1 \leq n \leq 9$).	4.5.1.3a The PICC shall accept bit boundaries within a character between $n \text{ etu} - 8/f_c$ and $n \text{ etu} + 8/f_c$. Where n is the number of bit boundaries after the start bit falling edge ($1 \leq n \leq 9$).

Requirements 4.11: Type B Bit Boundaries PICC to PCD

PCD	PICC
4.5.1.4a The PCD shall accept bit boundaries within a character at nominal positions of rising or falling edges of the subcarrier. The PCD shall accept bit boundaries that occur at n etu. Where n is the number of bit boundaries after the start bit falling edge ($1 \leq n \leq 9$).	4.5.1.4 The PICC shall apply bit boundaries within a character at nominal positions of rising or falling edges of the subcarrier. The bit boundaries shall occur at n etu. Where n is the number of bit boundaries after the start bit falling edge ($1 \leq n \leq 9$).

4.6 De-synchronization

De-synchronization is based on a violation of the regular encoding/decoding rules for a Logic “0” and a Logic “1”.

4.6.1 Type A – De-synchronization

Requirements 4.12: End of Sequence PCD → PICC – Type A

PCD	PICC
4.6.1.1 The PCD shall code EoS as follows: <ul style="list-style-type: none">• EoS: symbol Y	4.6.1.2 The PICC shall decode EoS as follows: <ul style="list-style-type: none">• If the PICC detects symbol Y after symbol Y, then it shall decode the last symbol Y as EoS.• If the PICC detects symbol Y after symbol Z, then it shall decode symbol Y as EoS.

Requirements 4.13: End of Sequence PICC → PCD – Type A

PCD	PICC
4.6.1.3 The PCD shall decode EoS as follows: <ul style="list-style-type: none">• If the PCD detects symbol F, then it shall decode this as EoS.	4.6.1.4 The PICC shall code EoS as follows: <ul style="list-style-type: none">• EoS: symbol F

4.6.2 Type B – De-synchronization

Requirements 4.14: End of Sequence PCD → PICC – Type B

PCD	PICC
4.6.2.1 The PCD shall code EoS as follows: <ul style="list-style-type: none">• EoS: a time $t_{PCD,E}$ with carrier low (modulation applied), followed by a transition to carrier high. The EoS shall come immediately after the last bit of the last data character (i.e. \mathbf{EGT}_{PCD} does not apply).	4.6.2.2 The PICC shall decode EoS as follows: <ul style="list-style-type: none">• If the carrier is low (modulation applied) for a time $t_{PCD,E}$, followed by a transition to carrier high (no modulation applied), then the PICC shall decode that as EoS. 4.6.2.2a The PICC shall decode a correctly coded EoS that follows the last bit of the last data character within a time \mathbf{EGT}_{PCD} as an EoS.

Requirements 4.15: End of Sequence PICC → PCD – Type B

PCD	PICC
<p>4.6.2.3 If the PCD detects:</p> <ul style="list-style-type: none"> • a subcarrier phase transition $\emptyset 0$ to $\emptyset 0+180^\circ$ • followed by the subcarrier with phase $\emptyset 0+180^\circ$ for a time $t_{PICC,E}$ • followed by a subcarrier phase transition $\emptyset 0+180^\circ$ to \emptyset <p>then the PCD shall decode this as EoS.</p>	<p>4.6.2.4 The PICC shall code the following as EoS:</p> <ul style="list-style-type: none"> • a subcarrier phase transition $\emptyset 0$ to $\emptyset 0+180^\circ$ • followed by a subcarrier with phase $\emptyset 0+180^\circ$ for a time $t_{PICC,E}$ • followed by a subcarrier phase transition $\emptyset 0+180^\circ$ to $\emptyset 0$ <p>The EoS shall come immediately after the last bit of the last data character (i.e. EGT_{PICC} does not apply).</p> <p>Refer to Annex A.4 for the value of $t_{PICC,E}$.</p>
<p>4.6.2.5 After EoS, the PCD shall be capable of supporting a PICC that maintains the subcarrier on for a time t_{FSOFF}.</p> <p><i>After the EoS, if the PICC maintains the subcarrier on for a time greater than t_{FSOFF}, then the PCD may resort to exception processing (transmission error).</i></p>	<p>4.6.2.6 After EoS, the PICC shall maintain the subcarrier on for a time t_{FSOFF} and shall then turn the subcarrier off.</p> <p>Refer to Annex A.4 for the value of t_{FSOFF}.</p>
<p><i>If the subcarrier is turned off at the same time as the phase transition $\emptyset 0+180^\circ$ to $\emptyset 0$ (i.e. $t_{FSOFF} = 0$), then the stopping of the subcarrier represents the end of the EoS.</i></p>	

4.7 Frames

This section specifies the frames used for Type A and Type B. It lists the specific requirements for Type A and Type B with regard to the frame format and frame size.

4.7.1 Type A – Frame Format

This section defines the frame format used for Type A. Type A uses two types of frames: short frame and standard frame. The short frame is used to initiate communication. The standard frame is used for data exchange.

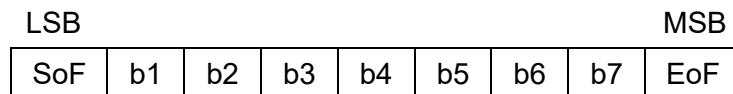
Short Frame

A short frame is used to initiate communication and consists of the following (see also Figure 4.10):

- Start of Frame (SoF)
- 7 data bits transmitted LSB first
- End of Frame (EoF)

No parity is added.

Figure 4.10: Short Frame

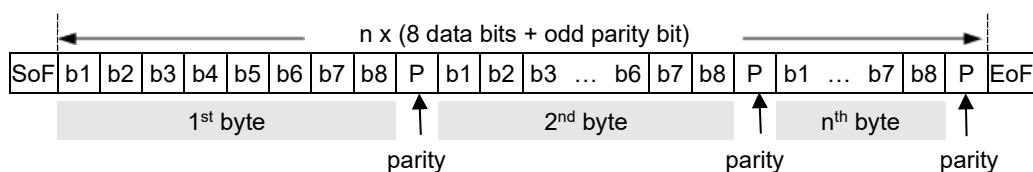


Standard Frame

Standard frames are used for data exchange and consists of the following (see also Figure 4.11):

- SoF
- $n \times (8 \text{ data bits} + \text{odd parity bit})$, with $n \geq 1$.
- EoF (PCD to PICC communication only)

Figure 4.11: Standard Frame



Requirements 4.16: Type A – Frame Format

PCD and PICC

4.7.1.1 A frame shall start with SoF.

For PCD to PICC communication the SoF shall be a Logic “0”.

For PICC to PCD communication the SoF shall be a Logic “1”.

4.7.1.2 For PCD to PICC communication, a frame shall end with EoF.
The EoF shall be a Logic “0”.

4.7.1.3 Each 8 data bits in a frame shall be followed by an odd parity bit.
The parity bit P shall be set such that the number of 1s is odd in
(b1 to b8, P).

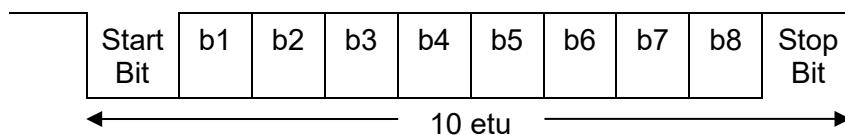
4.7.2 Type B – Frame Format

This section defines the character and frame format used for Type B.

Character Format

Data communication between the PICC and PCD is performed using an LSB first data format. Each 8 data bits are transmitted with a Logic “0” start bit and a Logic “1” stop bit as shown in Figure 4.12.

Figure 4.12: Type B Character Format



Requirements 4.17: Type B – Character Format

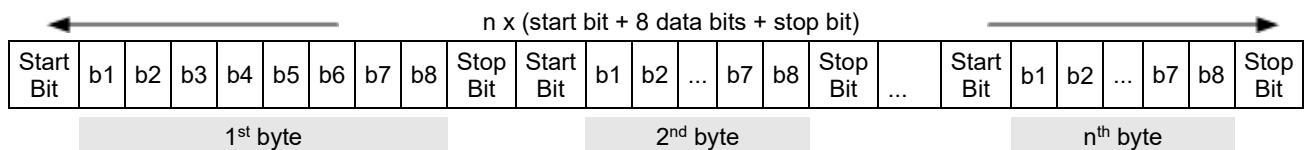
PCD and PICC

- 4.7.2.1 A character shall consist of a start bit (Logic “0”), 8 data bits, and a stop bit (Logic “1”). The stop bit, start bit, and each data bit shall be one elementary time unit (etu).

Frame Format

The characters sent between a PCD and a PICC are sent as frames (see Figure 4.13). Type B does not use SoF and EoF.

Figure 4.13: Type B – Frame Format



4.7.3 FSD (Frame Size for proximity coupling Device)

The FSD defines the maximum size of a frame the PCD is able to receive. FSD is expressed in number of data bytes included in the frame. For Type A, the PCD indicates FSD to the PICC by FSDI with the RATS command (see section 5.7.1). A Type B PCD indicates FSD to the PICC by Param 2 in the ATTRIB command (see section 6.4.1).

Requirements 4.18: FSD

PCD	PICC
4.7.3.1 The PCD shall be capable of accepting frames with FSD data bytes. The PCD shall resort to exception processing (protocol error) if it receives a frame with more than FSD data bytes.	4.7.3.2 The PICC shall only send frames with a number of data bytes less than or equal to FSD.
4.7.3.3 The FSD supported by the PCD shall be at least FSD_{MIN} .	4.7.3.4 The PICC shall be capable of supporting a PCD with FSD greater than or equal to FSD_{MIN} . <i>The PICC may support a PCD with FSD less than FSD_{MIN}.</i>

4.7.4 FSC (Frame Size for proximity Card)

The FSC defines the maximum size of a frame accepted by the PICC. FSC is expressed in number of data bytes included in the frame. For Type A the PICC indicates FSC to the PCD by FSCI in T0 of the ATS (see section 5.7.2). A Type B PICC indicates FSC to the PCD by Max_Frame_Size in the ATQB (see section 6.3.2).

Requirements 4.19: FSC

PCD	PICC
4.7.4.1 The PCD shall only send frames with a number of data bytes less than or equal to FSC.	4.7.4.2 The PICC shall be capable of accepting frames with FSC data bytes. <i>The PICC may resort to exception processing (protocol error) if it receives a frame with more than FSC data bytes. If blocks containing more than FSC data bytes are accepted, they should be handled correctly.</i>
4.7.4.3 The PCD shall be capable of sending frames in accordance with an FSC greater than or equal to FSC_{MIN} .	4.7.4.4 The FSC supported by the PICC shall be at least FSC_{MIN} .

4.8 Timing Requirements

This section specifies the requirements for the different Frame Delay Times for Type A and Type B. The Frame Delay Time (FDT) is defined as the time between two sequences transmitted in opposite directions.

This section uses the term ‘command’ to indicate a command sequence sent by the PCD and the term ‘response’ to indicate a response sequence sent by the PICC.

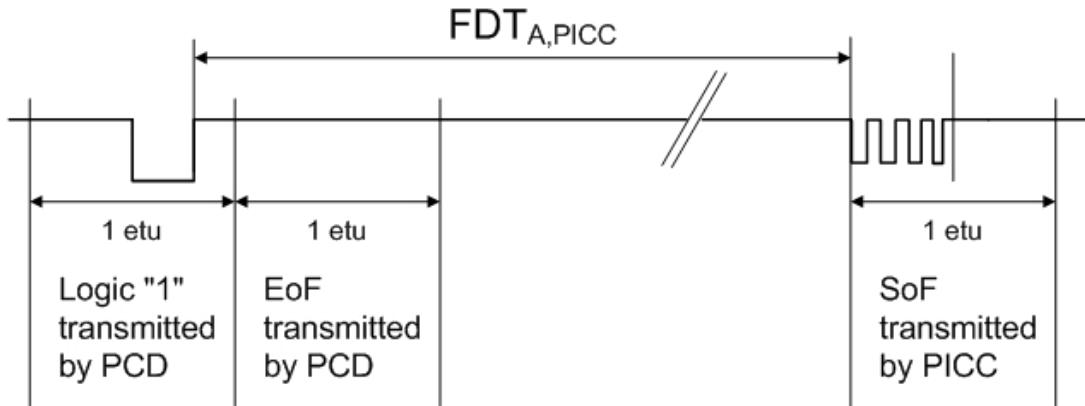
4.8.1 Frame Delay Time PCD → PICC

The Frame Delay Time PCD → PICC ($FDT_{PCD \rightarrow PICC}$) defines the time between the end of a PCD command and the start of the PICC response.

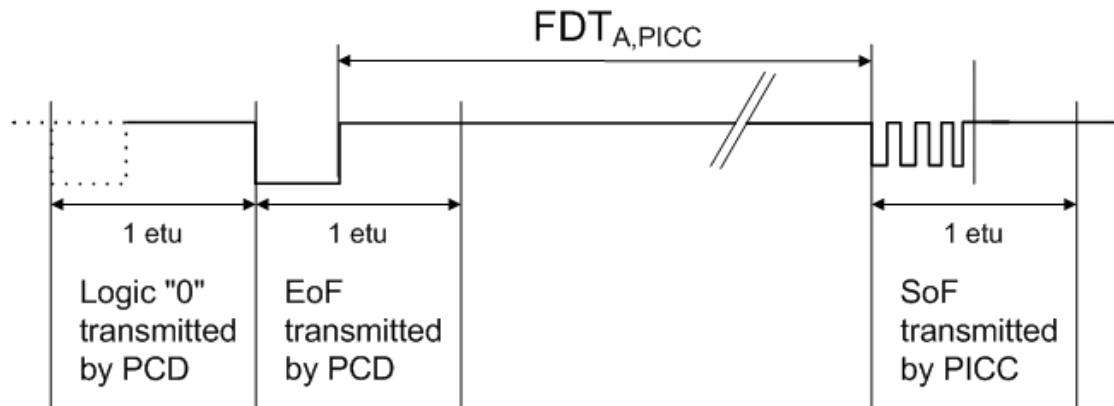
FDT_{A,PICC}

For Type A, $FDT_{A,PICC}$ is measured from the rising edge of the last lower level of the PCD command to the start of the SoF of the PICC response. The $FDT_{A,PICC}$ depends on the logic value of the last bit before the EoF transmitted by the PCD. The $FDT_{A,PICC}$ is shown in Figure 4.14.

Figure 4.14: FDT_{A,PICC}



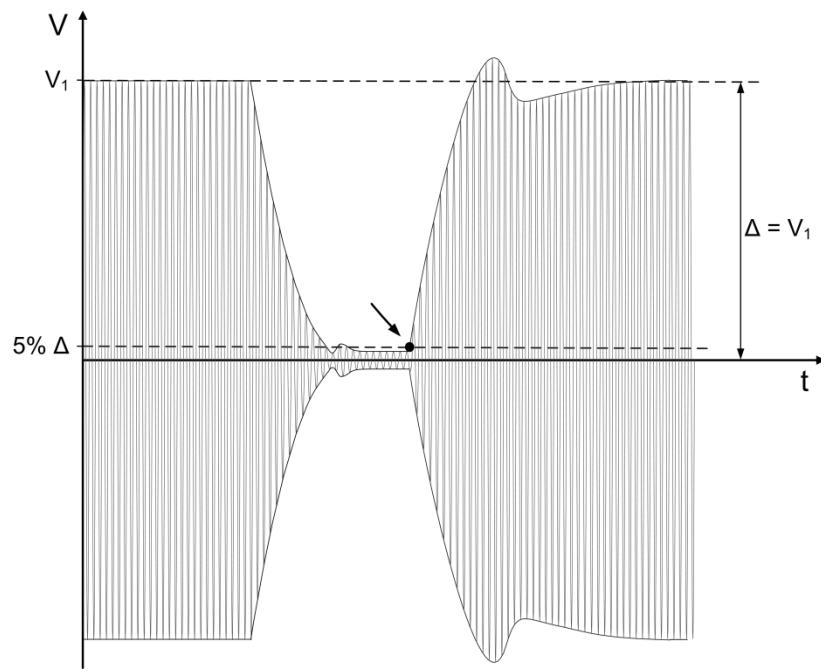
(a) Last bit before EoF is Logic "1"



(b) Last bit before EoF is Logic "0"

The end of the last lower level of a PCD command is the point where the rising edge of the last lower level of the signal envelope passes through the 5% threshold as shown in Figure 4.15.

Figure 4.15: End of PCD Command – Type A



The start of the SoF of the PICC response begins at the start of the first detectable edge of the modulation of the signal envelope. Figure 4.16 shows the starting point for positive modulation, Figure 4.17 for negative modulation.

Figure 4.16: Start of PICC Response (Positive Modulation) – Type A

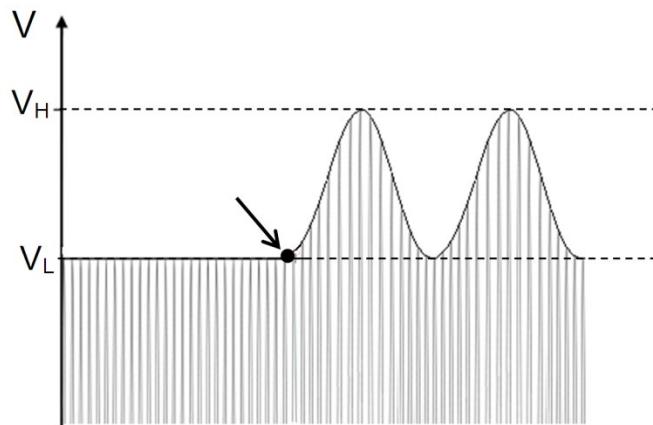
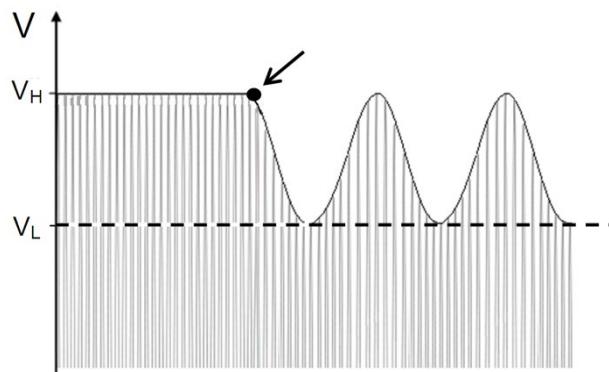
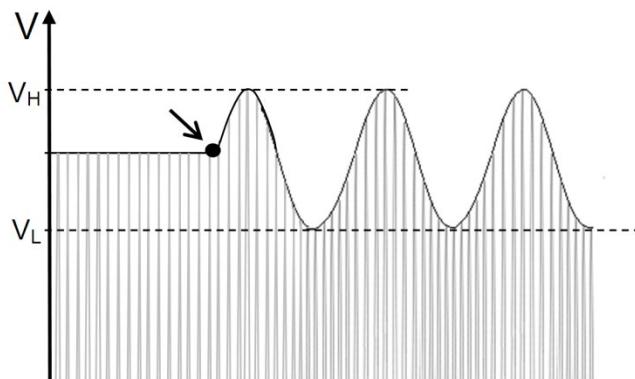


Figure 4.17: Start of PICC Response (Negative Modulation) – Type A



For positive or negative modulation, when observed using the EMV-TEST PCD, the signal envelope may appear to be neither 100% positive nor 100% negative (mixed) in any proportion and start with either a positive or negative part cycle – see Figure 4.18.

Figure 4.18: Start of PICC Response (Example of mixed modulation starting with a positive part cycle) – Type A



The $FDT_{A,PICC}$ depends on the logic value of the last bit before the EoF transmitted by the PCD as defined in Table 4.2.

Table 4.2: $FDT_{A,PICC}$ and Logic Value of Last Bit before EoF

Logic Value	$FDT_{A,PICC}$
“0”	$(n \times 128 + 20) / f_c$
“1”	$(n \times 128 + 84) / f_c$

The value of n is an integer and depends on the command type as defined in Table 4.3. The different commands are detailed in Chapter 5.

Table 4.3: $FDT_{A,PICC}$ and Command Type

Command Type	n
WUPA	9
REQA	
ANTICOLLISION	
SELECT	
All other commands	≥ 9

Requirements 4.20: FDT_{A,PICC}

PCD	PICC
4.8.1.1 Following the end of a PCD command, the PCD shall be able to receive the start of a PICC response at a time aligned to the grid as defined in Figure 4.14, Table 4.2, and Table 4.3 with a tolerance of $-1/f_c$ to $0.4\mu s + 1/f_c$.	4.8.1.2 The PICC shall align the first modulation edge within the start bit of a PICC response to the grid as defined in Figure 4.14, Table 4.2, and Table 4.3 with a tolerance of 0 to $0.4\mu s$.

Requirements 4.21: FDT_{A,PICC,MIN}

PCD
4.8.1.3 Following the end of a PCD command, the PCD shall ignore any response from the PICC during a time $FDT_{A,PICC,MIN} - 128/f_c$.

For the commands WUPA, REQA, SELECT, and ANTICOLLISION, the PICC always responds exactly at $FDT_{A,PICC,MIN}$ ($= FDT_{A,PICC}$ as defined in Table 4.2 with $n = 9$).

Requirements 4.22: FDT_{A,PICC} for WUPA, REQA, SELECT, and ANTICOLLISION

PCD	PICC
4.8.1.4 For the initialization commands WUPA, REQA, SELECT, and ANTICOLLISION, the PCD shall consider the receipt of a response after $FDT_{A,PICC,MIN}$ as a time-out error.	4.8.1.5 For the initialization commands WUPA, REQA, SELECT, and ANTICOLLISION, the PICC shall respond at $FDT_{A,PICC,MIN}$.

FDT_{B,PICC}

For Type B, FDT_{B,PICC} is measured from the end of the EoS of the PCD command to the start of the SoS of the PICC response as shown in Figure 4.19.

$$FDT_{B,PICC} = TR0 + TR1$$

Figure 4.19: FDT_{B,PICC}

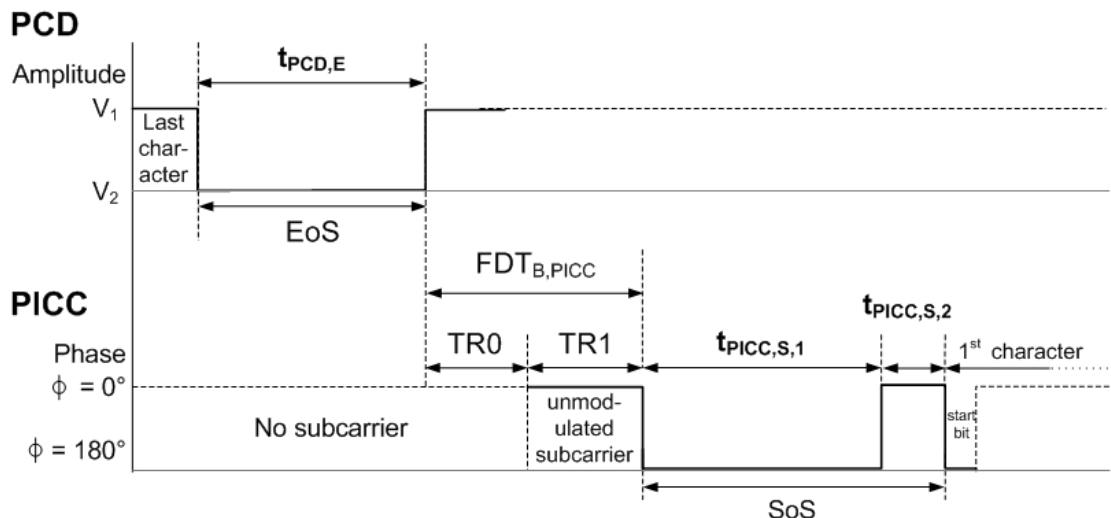
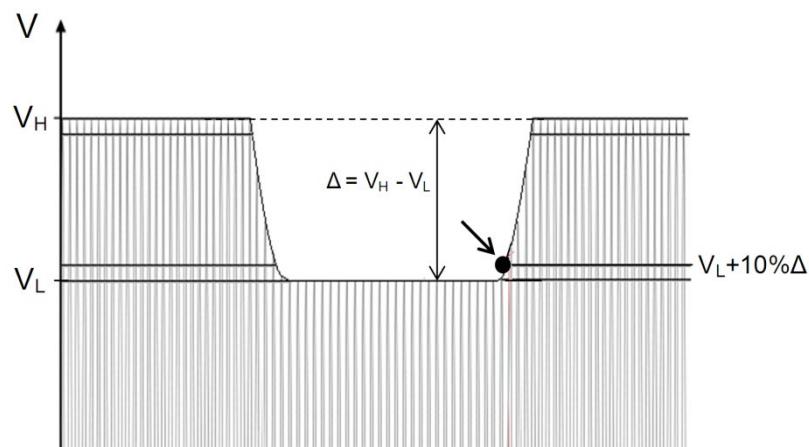


Figure 4.20 indicates the end of the EoS of the PCD command. It is the point where the last modulation of the signal envelope passes through the 10% level of the Δ threshold (Δ is the difference between modulated and unmodulated signal levels).

Figure 4.20: End of PCD Command – Type B



The start of the SoS of the PICC response begins at the nominal position of the start of the first phase shifted subcarrier cycle.

- For positive modulation and an initial phase of 0° (extended low phase change) the nominal position is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local minimum (as shown in Figure 4.21) plus the addition of $1/f_s$ (or $16/f_c$).
- For positive modulation and an initial phase of 180° (extended high phase change) the nominal position is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local maximum (as shown in Figure 4.22) plus the addition of $1/f_s$ (or $16/f_c$).
- For negative modulation and an initial phase of 0° (extended high phase change) the nominal position is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local maximum (as shown in Figure 4.22) plus the addition of $1/f_s$ (or $16/f_c$).
- For negative modulation and an initial phase of 180° (extended low phase change) the nominal position is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local minimum (as shown in Figure 4.21) plus the addition of $1/f_s$ (or $16/f_c$).

Figure 4.21: Start of PICC Response (Extended Low Phase Change) – Type B

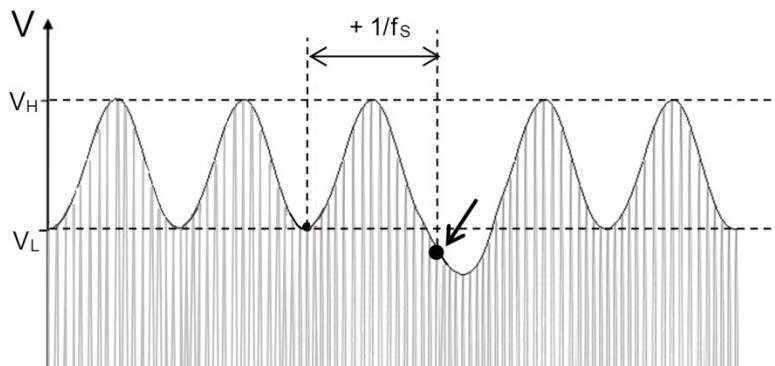
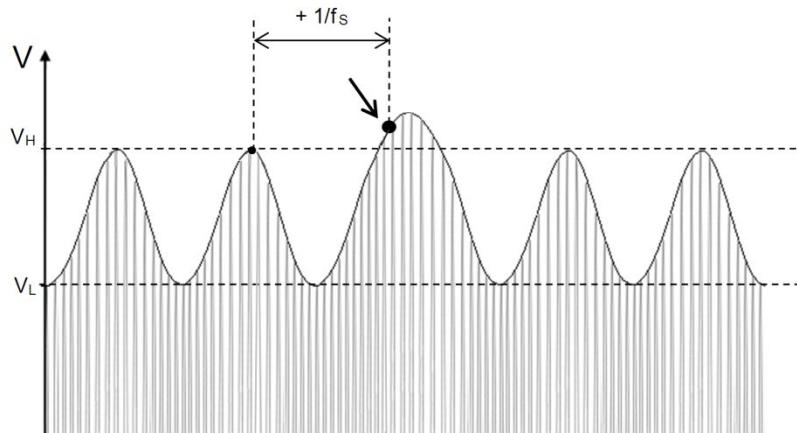


Figure 4.22: Start of PICC Response (Extended High Phase Change) – Type B



The minimum time a PICC is required to wait before sending the SoS of its response after the end of a PCD command ($FDT_{B,PICC,MIN}$) is defined by $TR0_{MIN} + TR1_{MIN}$.

Requirements 4.23: $FDT_{B,PICC,MIN}$

PCD	PICC
4.8.1.6 Following the EoS of a PCD command, the PCD shall be able to receive the SoS of the PICC response with a minimum interval between the EoS of the PCD command and the SoS of the PICC response of $FDT_{B,PICC,MIN}$.	4.8.1.7 Following the EoS of a PCD command, the PICC shall wait at least a time $FDT_{B,PICC,MIN}$ before sending the SoS of its response.

FDT_{PICC,MAX}

The maximum time within which a PICC is required to start its response after the end of a PCD command ($FDT_{PICC,MAX}$) is defined by the Frame Waiting Time (FWT). The definition of the FWT is common for Type A and Type B and defines the maximum value for $FDT_{A,PICC}$ and $FDT_{B,PICC}$ (except for WUPA, REQQA, SELECT, ANTICOLLISION, RATS, WUPB, and REQB).

The FWT is calculated by the following formula:

$$FWT = (256 \times 16 / f_c) \times 2^{FWI}$$

where the value of FWI has the range from 0 to 14. The FWI for Type B is located in the ATQB as defined in section 6.3.2. The FWI for Type A is located in the interface byte TB(1) of the ATS as defined in section 5.7.2.

Examples:

- FWI = 0, then FWT ≈ 302 μs
- FWI = 7, then FWT ≈ 39 ms

Requirements 4.24: Frame Waiting Time

PCD	PICC
<p>4.8.1.8 The PCD shall wait at least $\text{FWT} + \Delta\text{FWT}$ for a response from the PICC (except for WUPA, REQQA, SELECT, ANTICOLLISION, RATS, WUPB, and REQB).</p> <p>If the PCD does not receive a response from the PICC within $\text{FWT} + \Delta\text{FWT} + \Delta T_{\text{PCD}}$, then the PCD shall consider this as a time-out error.</p> <p>Refer to Annex A.4 for the values of ΔFWT and ΔT_{PCD}.</p> <p><i>Between $\text{FWT} + \Delta\text{FWT}$ and $\text{FWT} + \Delta\text{FWT} + \Delta T_{\text{PCD}}$, the PCD may accept the response of the PICC or may generate a time-out error.</i></p>	<p>4.8.1.9 The PICC shall start its response after the end of a PCD command within the FWT (except for WUPA, REQQA, SELECT, ANTICOLLISION, RATS, WUPB, and REQB).</p>
<p>4.8.1.10 The PCD shall support a PICC having an FWT less than or equal to FWT_{MAX}.</p>	<p>4.8.1.11 The maximum FWT of the PICC shall be FWT_{MAX}. Refer to Annex A.4 for the value of FWT_{MAX}.</p>

FDT_{A,PICC,MAX} for RATS Command

For the Type A – RATS command (see section 5.7.1), the PICC is required to start sending its response within FWT_{ACTIVATION} (activation frame waiting time).

Requirements 4.25: Activation Frame Waiting Time

PCD	PICC
<p>4.8.1.12 For the Type A – RATS command, the PCD shall wait at least FWT_{ACTIVATION} for a response from the PICC.</p> <p>If the PCD does not receive a response from the PICC within FWT_{ACTIVATION} + ΔT_{PCD}, then the PCD shall consider this is as a time-out error.</p> <p>Refer to Annex A.4 for the value of ΔT_{PCD}.</p> <p><i>Between FWT_{ACTIVATION} and FWT_{ACTIVATION} + ΔT_{PCD}, the PCD may accept the response of the PICC or may generate a time-out error.</i></p>	<p>4.8.1.13 For the Type A – RATS command, the PICC shall start its response within FWT_{ACTIVATION}. Refer to Annex A.4 for the value of FWT_{ACTIVATION}.</p>

TR0

For Type B, TR0 is measured from the EoS of the PCD command to the start of unmodulated subcarrier of the PICC response as shown in Figure 4.20 above and Figure 4.23, Figure 4.24 and Figure 4.25 below.

Figure 4.23: Start of Unmodulated Subcarrier of PICC Response (Positive Modulation)

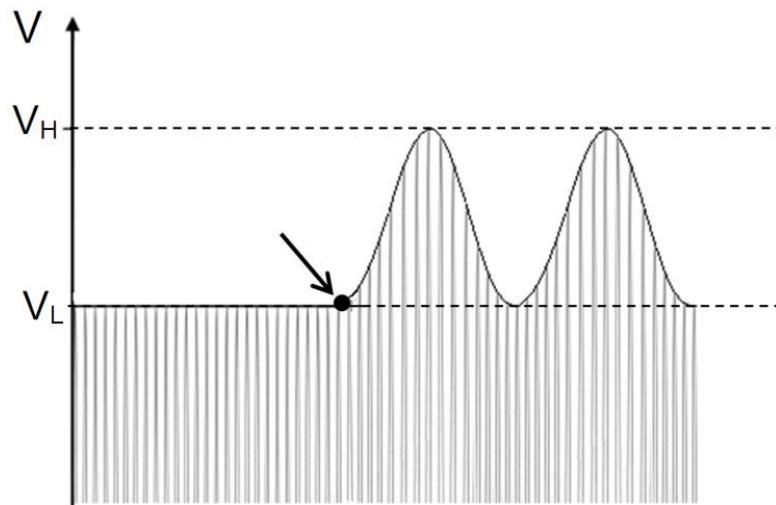
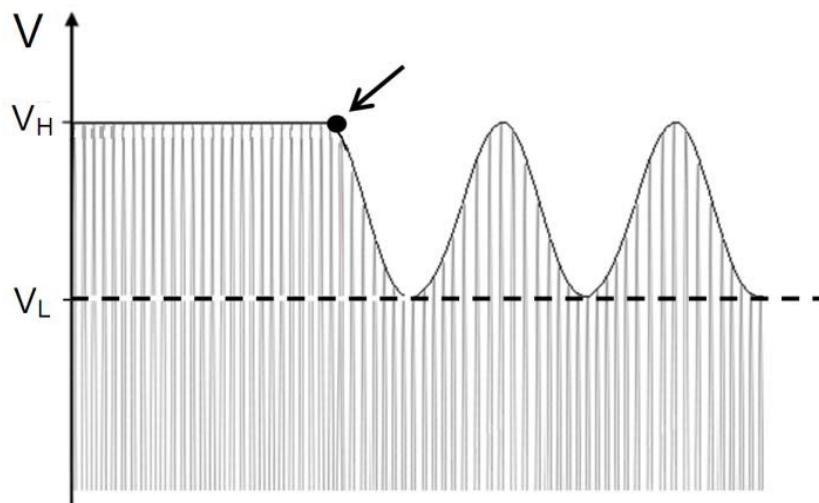
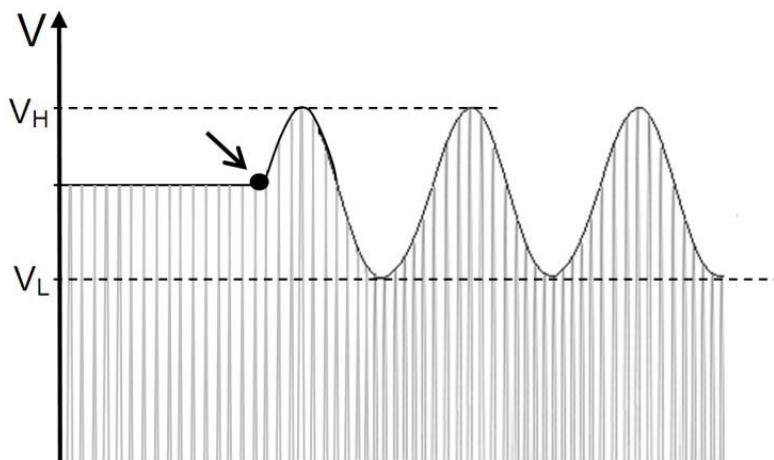


Figure 4.24: Start of Unmodulated Subcarrier of PICC Response (Negative Modulation)



**Figure 4.25: Start of Unmodulated Subcarrier of PICC Response
(Example of Mixed Modulation Starting with Positive Part Cycle)**



FDT_{B,PICC,MAX} and TR0_{MAX} for WUPB and REQB Commands

For the Type B – WUPB and REQB commands (see section 6.3.1), the PICC starts the unmodulated subcarrier within TR0_{MAX,ATQB}.

Requirements 4.26: FWT_{ATQB} and TR0_{MAX} for WUPB and REQB Commands

PCD	PICC
<p>4.8.1.14 For the Type B – WUPB and REQB commands, the PCD shall wait at least FWT_{ATQB} for a response from the PICC.</p> <p>If the PCD does not receive a response from the PICC within FWT_{ATQB} + ΔT_{PCD}, then the PCD shall consider this is as a time-out error.</p> <p>Refer to Annex A.4 for the value of FWT_{ATQB} and ΔT_{PCD}.</p> <p><i>Between FWT_{ATQB} and FWT_{ATQB} + ΔT_{PCD}, the PCD may accept the response of the PICC or may generate a time-out error.</i></p> <p><i>If the PCD does not detect the start of the subcarrier from the PICC before TR0_{MAX,ATQB}, then the PCD may consider this is as a time-out error.</i></p>	<p>4.8.1.15 For the Type B – WUPB and REQB commands, the PICC shall start the unmodulated subcarrier within TR0_{MAX,ATQB}.</p> <p>Refer to Annex A.4 for the value of TR0_{MAX,ATQB}.</p>

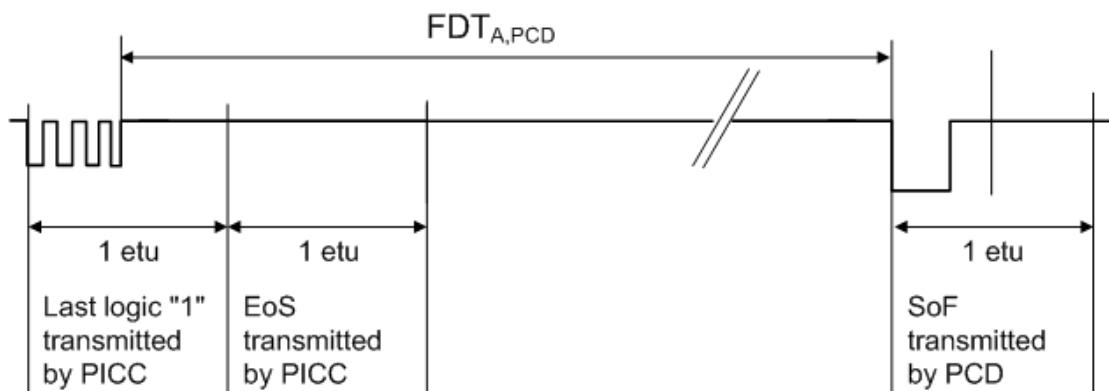
4.8.2 Frame Delay Time PICC → PCD

The Frame Delay Time PICC → PCD (FDT_{PCD}) defines the time between the end of a PICC response and the start of a new PCD command.

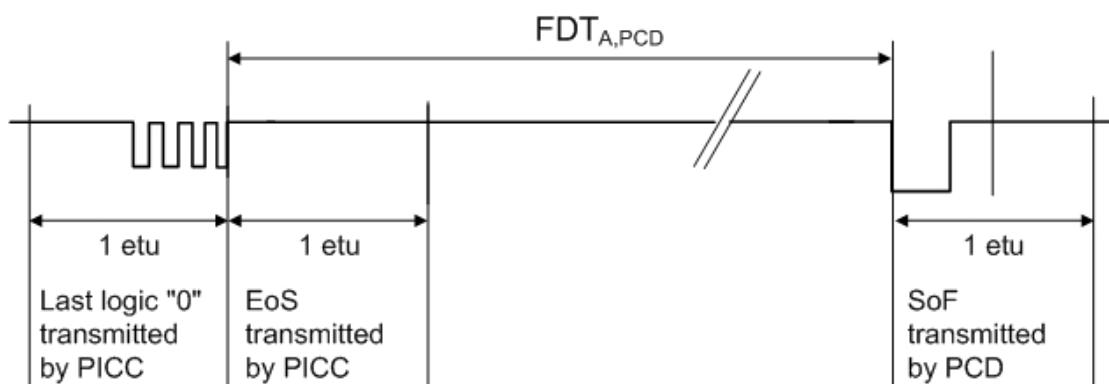
FDT_{A,PCD}

For Type A, FDT_{A,PCD} is measured from the last modulation transmitted by the PICC to the start of the lower level within the SoF of the next command transmitted by the PCD as shown in Figure 4.26.

Figure 4.26: FDT_{A,PCD}



(a) Last transmitted data bit is logic "1"



(b) Last transmitted data bit is logic "0"

The end of the last subcarrier modulation transmitted by the PICC corresponds to the end of the last detectable edge of the modulation of the signal envelope. Figure 4.27 shows the end for positive modulation and Figure 4.28 for negative modulation.

Figure 4.27: End of PICC Response (Positive Modulation) – Type A

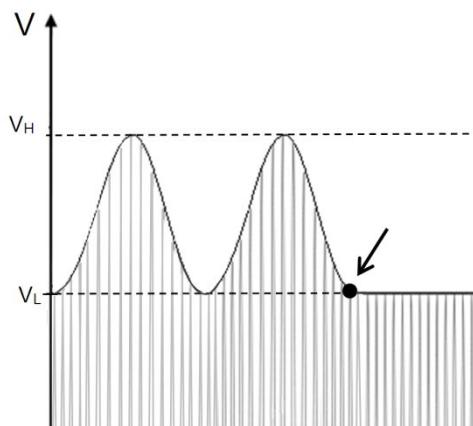
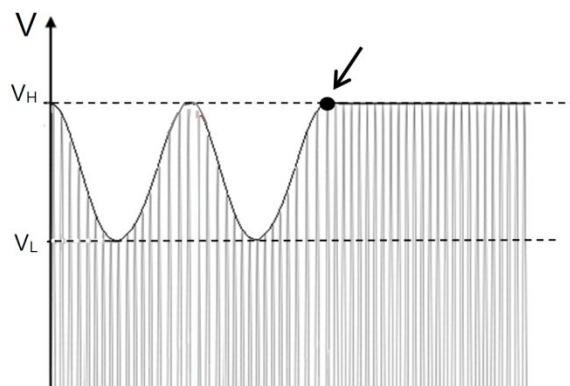
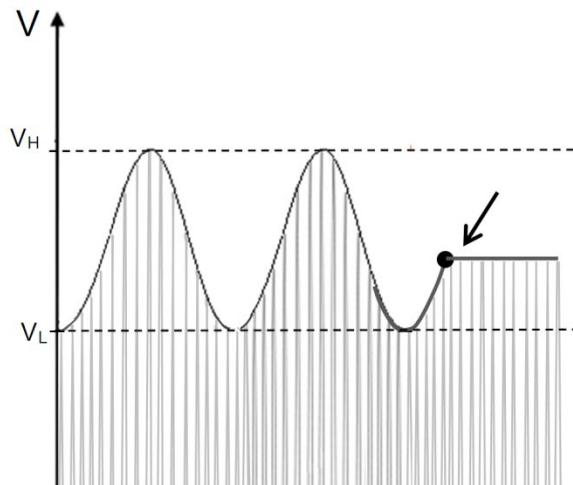


Figure 4.28: End of PICC Response (Negative Modulation) – Type A



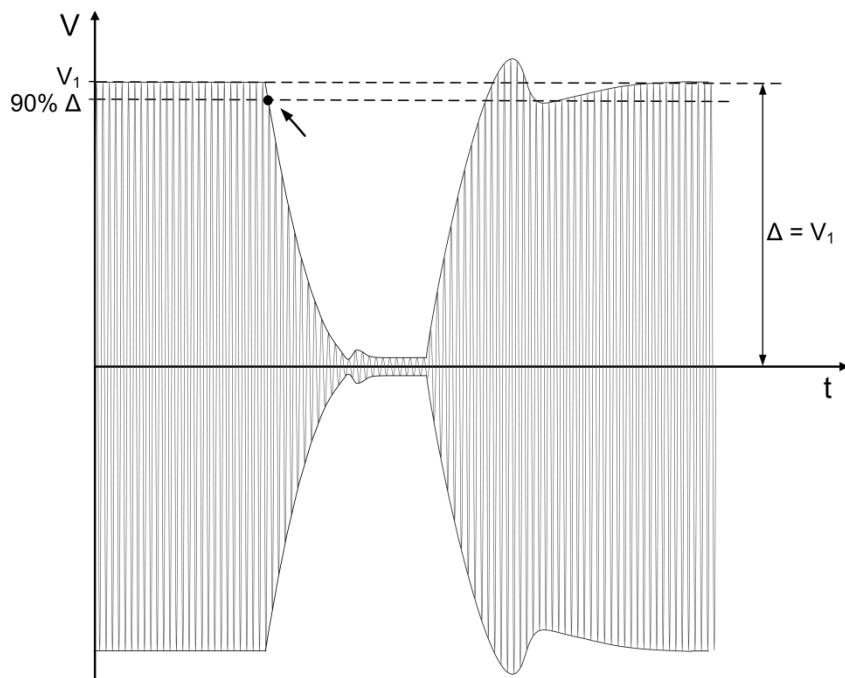
For positive or negative modulation, when observed using the EMV-TEST PCD, the signal envelope may appear to be neither 100% positive nor 100% negative (mixed) in any proportion and end with either a positive or negative part cycle – see Figure 4.29.

Figure 4.29: End of PICC Response (Example of mixed modulation ending with a negative part cycle) – Type A



The start of the lower level of the SoF of a PCD command is the point where the falling edge of the signal envelope passes through the 90% threshold as shown in Figure 4.30.

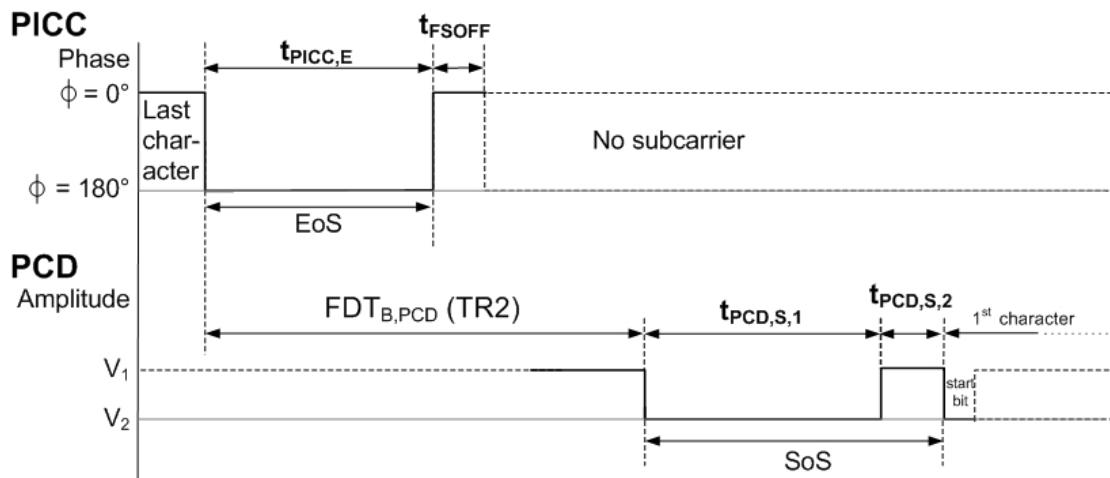
Figure 4.30: Start of PCD Command – Type A



FDT_{B,PCD}

For Type B, FDT_{B,PCD} is measured from the start of the EoS transmitted by the PICC to the SoS transmitted by the PCD as shown in Figure 4.31. FDT_{B,PCD} is also referred to as TR2.

Figure 4.31: FDT_{B,PCD}



The start of the EoS of the PICC response begins at the nominal position of the start of the first phase shifted subcarrier cycle (of the EoS).

- For extended low phase change the nominal position is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local minimum (as shown in Figure 4.32) plus the addition of $1/f_s$ (or $16/f_c$).
- For extended high phase change the nominal position is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local maximum (as shown in Figure 4.33) plus the addition of $1/f_s$ (or $16/f_c$).

Note that EoS is treated in isolation and there is no distinguishable difference between positive and negative modulation.

Figure 4.32: End of PICC Response (Extended Low Phase Change) – Type B

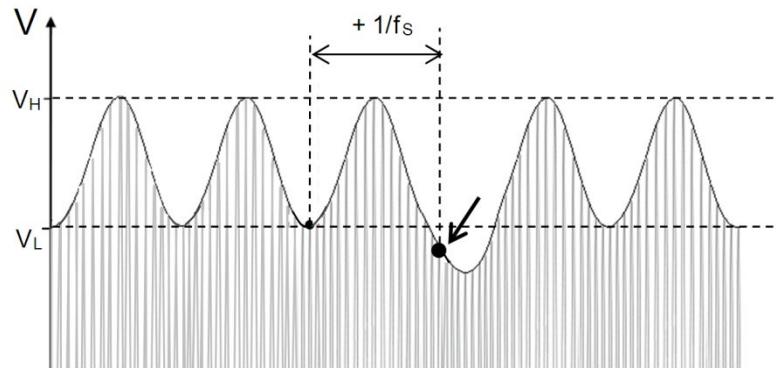
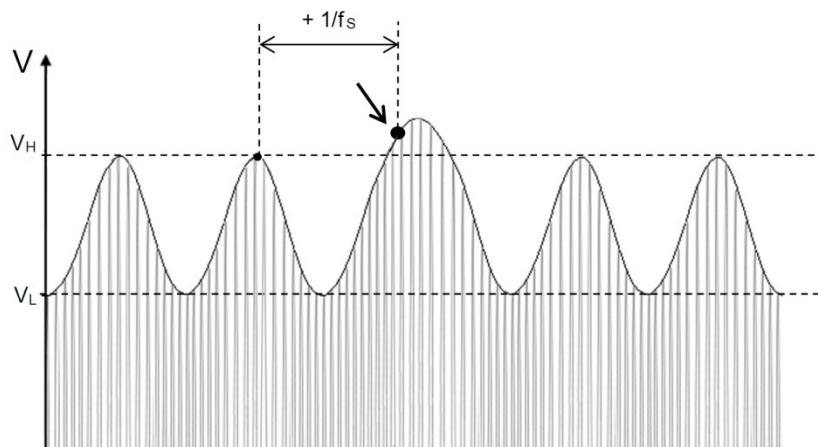
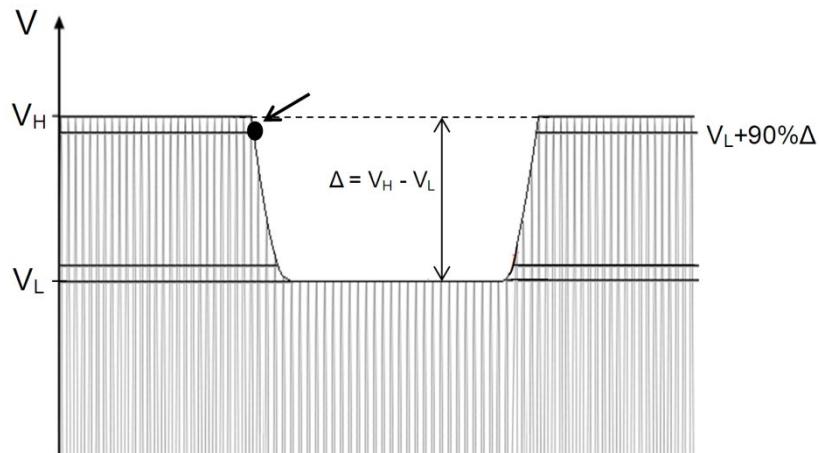


Figure 4.33: End of PICC Response (Extended High Phase Change) – Type B



The start of the SoS of the PCD command is when the first modulation of the signal envelope passes through the 90% level of the Δ threshold (Δ is the difference between modulated and unmodulated signal levels) as shown in Figure 4.34.

Figure 4.34: Start of PCD Command – Type B



FDT_{PCD,MIN}

FDT_{PCD,MIN} is the minimum time the PCD is required to wait before sending the start of a new PCD command after the end of the PICC response (except after the RATS and ATTRIB response when a guard time (SFGT) is requested by the PICC). FDT_{PCD,MIN} defines the minimum value for FDT_{A,PCD} and FDT_{B,PCD} and is FDT_{A,PCD,MIN} for a Type A PICC and FDT_{B,PCD,MIN} for a Type B PICC.

Requirements 4.27: FDT_{PCD,MIN}

PCD	PICC
<p>4.8.2.1 Following the end of a PICC response, the PCD shall wait at least a time FDT_{A,PCD,MIN} before transmitting the start of a new Type A PCD command and at least FDT_{B,PCD,MIN} before transmitting the start of a new Type B PCD command.</p> <p>Refer to Annex A.4 for the value of FDT_{A,PCD,MIN} and FDT_{B,PCD,MIN}.</p>	<p>4.8.2.2 Following the end of a PICC response, the PICC shall be able to receive the start of a new PCD command with a minimum interval between the end of the PICC response and the start of the new PCD command of FDT_{A,PCD,MIN} for a Type A command and FDT_{B,PCD,MIN} for a Type B command.</p> <p><i>If the start of a new Type A PCD command is received before FDT_{A,PCD,MIN}, or a new Type B PCD command before FDT_{B,PCD,MIN}, then the PICC may consider this as a transmission error.</i></p>

SFGT

For Type A, the SFGT is the guard time needed by the PICC before it is ready to receive the next command after it has sent the ATS (see section 5.7.2). For Type B, the SFGT is the guard time needed by the PICC before it is ready to receive the next command after it has sent the ATTRIB response (see section 6.4.2).

The SFGT is calculated by the following formula:

$$\text{SFGT} = (256 \times 16 / f_c) \times 2^{\text{SFGI}}$$

where SFGI has the range from 1 to 14. If the PICC returns SFGI equal to zero or SFGI is not returned, then no SFGT is needed and FDT_{PCD,MIN} applies.

For Type A, the SFGI is returned by the PICC in the interface byte TB(1) of the ATS (see section 5.7.2). For Type B, the SFGI is returned by the PICC in the ATQB (see section 6.3.2).

Requirements 4.28: SFGT

PCD	PICC
4.8.2.3 If the PICC returns an SFGI different from zero, the PCD shall wait at least SFGT + ΔSFGT before sending the next command after the PICC has sent the ATS (for Type A) or ATTRIB response (for Type B). Refer to Annex A.4 for the value of ΔSFGT .	4.8.2.4 If the PICC returns an SFGI different from zero, then following the ATS (for Type A) or ATTRIB response (for Type B), the PICC shall be able to receive the start of a new PCD command with a minimum interval between the end of the response and the start of the new PCD command of SFGT. <i>If the start of a new PCD command is received before SFGT, then the PICC may consider this as a transmission error.</i>

PCD	PICC
4.8.2.5 If the PCD returns an SFGI equal to zero or SFGI is not returned, the PCD shall wait at least $FDT_{PCD,MIN}$ before sending the next command after the PCD has sent the ATS (for Type A) or ATTRIB response (for Type B).	4.8.2.6 If the PCD returns an SFGI equal to zero or does not return an SFGI, then following the ATS (for Type A) or ATTRIB response (for Type B), the PCD shall be able to receive the start of a new PCD command with a minimum interval between the end of the response and the start of the new PCD command of $FDT_{PCD,MIN}$. <i>If the start of a new PCD command is received before $FDT_{PCD,MIN}$, then the PCD may consider this as a transmission error.</i>

4.8.3 Summary

Table 4.4 gives an overview of the minimum and maximum values for the Type A – Frame Delay Times.

Table 4.4: Type A – Timings

FDT _A	Minimum	Maximum
FDT _{A,PCD}	FDT _{A,PCD,MIN}	n.a.
FDT _{A,PICC}	FDT _{A,PICC} with n = 9 (see Table 4.2)	<ul style="list-style-type: none"> • FDT_{A,PICC} with n = 9 for WUPA, REQA, ANTICOLLISION, and SELECT • FWT_{ACTIVATION} for RATS • FWT for all other commands

Table 4.5 gives an overview of the minimum and maximum values for the Type B – Frame Delay Times.

Table 4.5: Type B – Timings

FDT _B	Minimum	Maximum
FDT _{B,PCD}	FDT _{B,PCD,MIN}	n.a.
FDT _{B,PICC}	TR0 _{MIN} + TR1 _{MIN}	<ul style="list-style-type: none"> • TR0_{MAX,ATQB} + TR1_{MAX} for ATQB • FWT for all other commands

4.9 EMD Handling

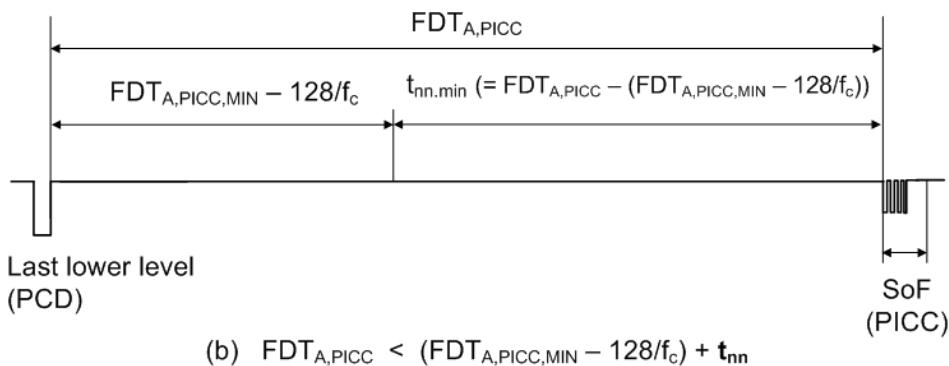
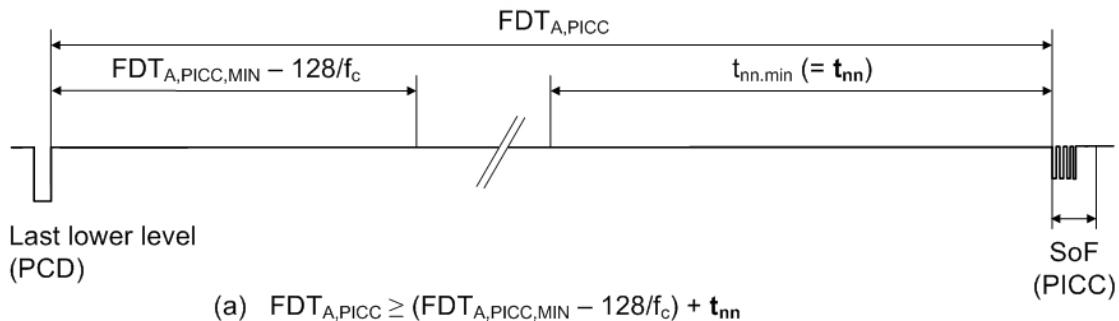
EMD handling enhances the robustness of the contactless communication between PCD and PICC against PICC generated electromagnetic disturbance (EMD).

4.9.1 $t_{nn,min}$

The time $t_{nn,min}$ is the minimum period during which the PICC is not allowed to produce any detectable disturbance before sending its response.

For Type A, $t_{nn,min}$ is defined as the minimum of $FDT_{A,PICC} - (FDT_{A,PICC,MIN} - 128/f_c)$ and t_{nn} . $t_{nn,min}$ is measured before the start of the SoF of the PICC response as shown in Figure 4.35.

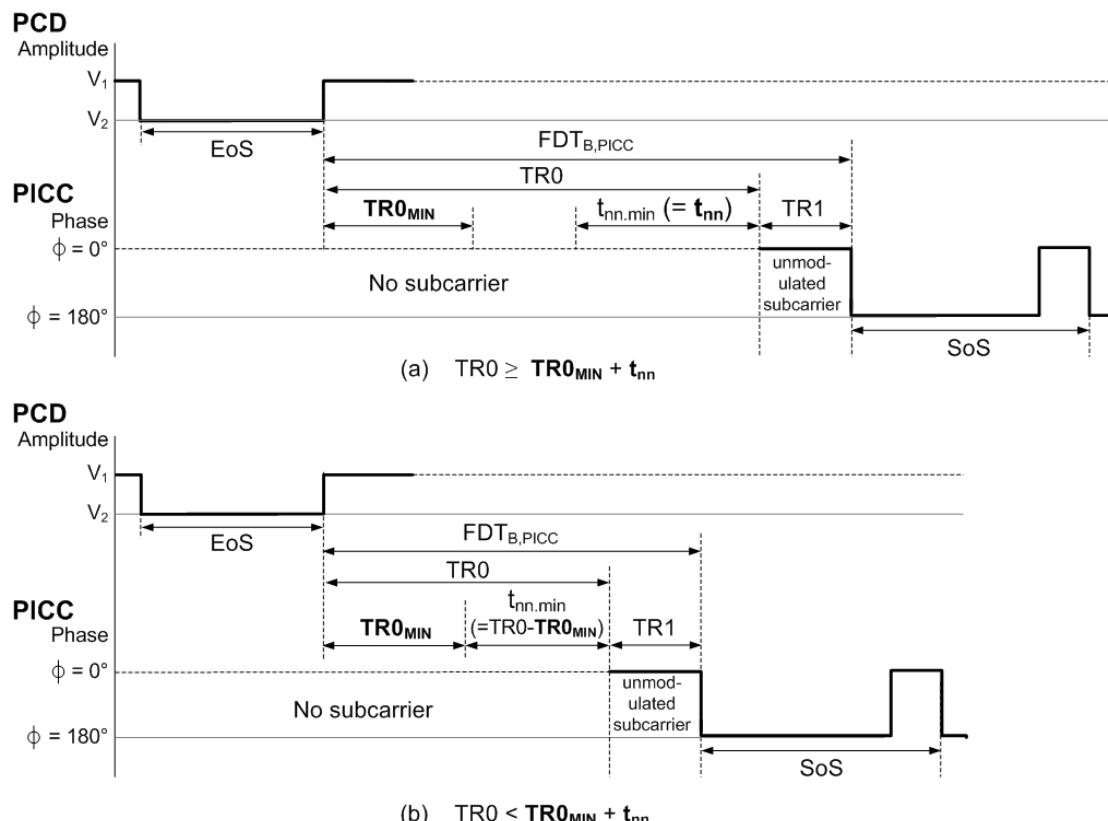
Figure 4.35: $t_{nn,min}$ for Type A



For Type B, $t_{nn,min}$ is defined as the minimum of $TR0 - TR0_{MIN}$ and t_{nn} .

For $TR0_{MIN}$ the PCD value is used. $t_{nn,min}$ is measured before the start of TR1 as shown in Figure 4.36.

Figure 4.36: $t_{nn,min}$ for Type B



Refer to Annex A.4 for the value of t_{nn} .

Requirements 4.29: $t_{nn,min}$

PICC

- 4.9.1.1 The PICC shall not produce any detectable disturbance during a period of at least $t_{nn,min}$ before sending its response. Where any modulation of the carrier envelope at J2 of the EMV - TEST PCD that can be distinguished from noise as having been produced by the PICC constitutes detectable disturbance.

Legacy PICCs may exhibit a single monotonic change in level of the envelope of the carrier provided it occurs at a rate not more than 1.2% of the envelope of the carrier per μs .

This was previously requirement number 4.8.1.16.

4.9.2 PCD EMD Handling

It is important for a PCD to distinguish between EMD and frame reception errors and therefore the following PCD EMD handling applies.

Requirements 4.30: PCD EMD Handling

PCD

- 4.9.2.1 When the PCD receives a PICC frame it shall check for transmission errors.

If transmission errors are detected in real time and the number of received bytes when a transmission error is detected is less than 4, then the PCD shall ignore the transmission and be ready to receive a PICC frame no later than $t_{RECOVERY}$ after the end of the modulation of the received bytes with the transmission error.

Alternatively, if transmission errors are not detected until the end of the frame containing an error and the number of received bytes is less than 4, then the PCD shall ignore the transmission and be ready to receive a PICC frame no later than $t_{RECOVERY}$ after the end of the modulation of the received bytes with the transmission error.

This does not apply to responses to the WUPA, REQA, SELECT, ANTICOLLISION, WUPB and REQB commands.

Refer to Annex A.5 for the value of $t_{RECOVERY}$.

The above defined EMD handling overrules the specified transmission error handling in cases where a transmission error is detected when less than 4 bytes have been received from the PICC.

It is recommended that the receiver detects transmission errors in real time and reacts as soon as the error is detected.

- 4.9.2.2 The PCD shall ignore any PICC generated EMD that occurs from the end of the EoS of a Type A PICC response until the start of the lower level within the SoF of the next command transmitted by the PCD.

5 Type A – Commands and Responses

This chapter specifies the Type A commands that are available to the PCD for the polling, collision detection, activation and removal procedures. Commands and responses are transmitted within frames as specified in section 4.7.

5.1 Type A – Command Set

Table 5.1 lists the commands that are available to the PCD for communication with a PICC of Type A. For every command, the corresponding response from the PICC is indicated.

Table 5.1: Type A – Command Set

PCD Command	PICC Response
WUPA	ATQA
REQA	ATQA
ANTICOLLISION CL1	UID CL1
ANTICOLLISION CL2	UID CL2
ANTICOLLISION CL3	UID CL3
SELECT CL1	SAK
SELECT CL2	SAK
SELECT CL3	SAK
HLTA	–
RATS	ATS
PPS	PPSR

This chapter details the format of these commands and their responses from the PICC.

Requirements 5.1: Protocol Error – Type A

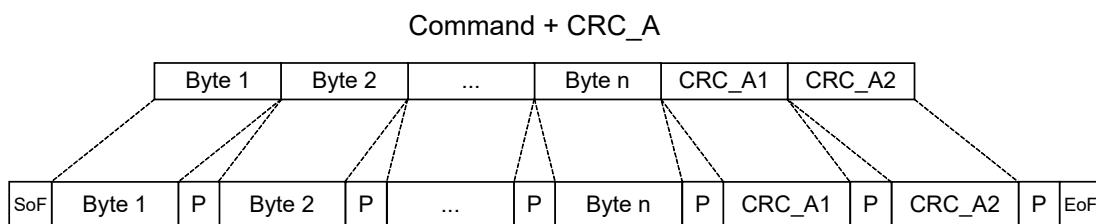
PCD	PICC
5.1.1.1 The PCD shall consider any PICC response transmitted in a valid frame (no transmission error) but having a coding not compliant with this specification, as a protocol error.	5.1.1.2 The PICC shall consider any PCD command transmitted in a valid frame (no transmission error) but having a coding not compliant with this specification, as a protocol error.

5.2 Type A – CRC_A

Some of the commands defined in Table 5.1 use a CRC for error checking. The CRC_A is defined as a function of k data bits, which consist of all the bits in the command. Since all commands using a CRC_A are encoded in bytes, the number of bits k is a multiple of 8.

Figure 5.1 shows how a command and the CRC_A are included within a standard frame. CRC_A1 is the least significant byte and CRC_A2 is the most significant byte.

Figure 5.1: Position of CRC_A within a Standard Frame



Requirements 5.2: CRC_A

PCD and PICC

- 5.2.1.1 If a CRC_A is included in a standard frame, then it shall be inserted in the frame after the last parity bit of the data bits.
Each CRC_A byte shall be followed by a parity bit.
A short frame shall not have a CRC_A.
- 5.2.1.2 The CRC_A is as defined in [ISO/IEC 13239], but the initial register content shall be '6363' and the register content shall not be inverted after calculation.

5.3 WUPA and REQA

The WUPA and REQA commands are sent by the PCD to probe the field for PICCs of Type A.

5.3.1 WUPA and REQA Command

The WUPA and REQA commands are transmitted within a short frame. The coding is specified in Table 5.2.

Table 5.2: Coding of WUPA and REQA within a Short Frame

b7	b6	b5	b4	b3	b2	b1	Meaning
1	0	1	0	0	1	0	WUPA
0	1	0	0	1	1	0	REQA

5.3.2 WUPA and REQA Response (ATQA)

In response to the WUPA and REQA commands, a PICC of Type A, depending on its state (see Chapter 7) will return an ATQA with a length of two bytes. The ATQA is transmitted within a standard frame without CRC_A and coded as specified in Table 5.3 and Table 5.4.

Table 5.3: Byte 1 of ATQA

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0	0							UID size: single (4 bytes)
0	1							UID size: double (7 bytes)
1	0							UID size: triple (10 bytes)
1	1							RFU
	0							RFU
		1	0	0	0	0		Bit frame anticollision ³
		0	1	0	0	0		Bit frame anticollision
		0	0	1	0	0		Bit frame anticollision
		0	0	0	1	0		Bit frame anticollision
		0	0	0	0	1		Bit frame anticollision
							All other values	RFU

³ If the PICC supports Bit frame anticollision then it should do so according to [ISO/IEC 14443-3] however this functionality is beyond the scope of this specification.

Table 5.4: Byte 2 of ATQA

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0								RFU
	0							RFU
		0						RFU
			0					RFU
				x	x	x	x	Any value

Requirements 5.3: PCD Handling of ATQA**PCD**

- 5.3.2.1 The PCD shall not examine or depend upon the values returned by the PICC in b8 to b7 and b5 to b1 of byte 1 and in b4 to b1 of byte 2 of the ATQA.⁴

Requirements 5.4: UID Length

PCD	PICC
5.3.2.2 The PCD shall be capable of successfully recovering a UID of 4, 7, or 10 bytes.	5.3.2.3 The PICC shall have a UID of 4, 7, or 10 bytes. The value of the UID shall be a fixed number or a random number which is dynamically generated by the PICC. <i>The value of the UID should conform to the UID contents requirements of [ISO/IEC 14443-3].</i>

⁴ A PCD supporting proprietary functionality may interpret any of the bits b4 to b1 of byte 2 of the ATQA and implement proprietary functionality which is out of scope of this specification.

Requirements 5.5: Dynamic UID

PICC

- 5.3.2.4 A dynamically generated UID shall change value only on state transition from **POWER-OFF** to **IDLE** state (see Chapter 7).
- 5.3.2.5 The length of a dynamically generated UID shall be 4 bytes.

5.4 ANTICOLLISION

The ANTICOLLISION command is used to obtain the complete UID of a Type A PICC and to detect whether more than one Type A PICC is in the Operating Field of the PCD (see section 9.3.2 for more details).

5.4.1 ANTICOLLISION Command

The ANTICOLLISION command is transmitted within a standard frame without CRC_A. Its coding is specified in Table 5.5.

Table 5.5: Coding of ANTICOLLISION Command

Byte 1	Byte 2
SEL	'20'

The SEL byte is coded as shown in Table 5.6.

Table 5.6: Coding of SEL

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
1	0	0	1	0	0	1	1	'93': ANTICOLLISION CL1
1	0	0	1	0	1	0	1	'95': ANTICOLLISION CL2
1	0	0	1	0	1	1	1	'97': ANTICOLLISION CL3
1	0	0	1	other values except those here above				Not allowed

With the SEL byte the Cascade Level (CL) of the UID requested by the ANTICOLLISION command is defined.

5.4.2 ANTICOLLISION Response (UID CLn)

In response to the ANTICOLLISION command all PICCs in the Operating Field transmit the requested cascade level of their UID (UID CLn, with n = 1, 2 or 3). The UID of a Type A PICC consists of 4, 7 or 10 bytes. The length of the response is always 5 bytes. The coding of the response is depending on the value of the SEL byte and the length of the UID. The ANTICOLLISION response is transmitted within a standard frame without CRC_A. Its coding is specified in Table 5.7.

Table 5.7: UID CLn

SEL	UID Size	Response (UID CLn)
'93'	4	UID CL1: uid ₀ uid ₁ uid ₂ uid ₃ BCC
'93'	> 4	UID CL1: CT uid ₀ uid ₁ uid ₂ BCC
'95'	7	UID CL2: uid ₃ uid ₄ uid ₅ uid ₆ BCC
'95'	> 7	UID CL2: CT uid ₃ uid ₄ uid ₅ BCC
'97'	10	UID CL3: uid ₆ uid ₇ uid ₈ uid ₉ BCC

Where:

- CT is the cascade tag with a value of '88'. The purpose of the cascade tag is to force a collision with PICCs that have a smaller UID size. Therefore, uid₀ of a single size UID and uid₃ of a double size UID must not have the value '88'.
- BCC is the UID CLn check byte. BCC is calculated as exclusive-or over the 4 previous bytes.
- uid_n is the nth byte of the complete UID with uid₀ the most significant byte.

Requirements 5.6: PCD Handling of BCC

PCD

5.4.2.1 The PCD shall verify the BCC included in the UID CLn. The PCD shall consider an incorrect BCC as a transmission error.

5.5 SELECT

The SELECT command is used to select the Type A PICC using its UID.

5.5.1 SELECT Command

The SELECT command is transmitted with CRC_A within a standard frame. Its coding is specified in Table 5.8.

Table 5.8: Coding of SELECT Command

Byte 1	Byte 2	Bytes 3 – 7
SEL	'70'	UID CLn

The SEL byte is coded as is shown in Table 5.9.

Table 5.9: Coding of SEL

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
1	0	0	1	0	0	1	1	'93': SELECT CL1
1	0	0	1	0	1	0	1	'95': SELECT CL2
1	0	0	1	0	1	1	1	'97': SELECT CL3
1	0	0	1	Other values except those here above				Not allowed

The coding of UID CLn is depending on the value of the SEL byte and the size of the UID. The coding is the same as for the ANTICOLLISION response and specified in Table 5.7.

5.5.2 Response – Select Acknowledge – SAK

The SAK is transmitted by the PICC in response to a SELECT command when all the data bits match with the UID CLn of the PICC. The length of the SAK is one byte and transmitted with CRC_A within a standard frame. The SAK is coded as specified in Table 5.10.

Table 5.10: Coding of SAK⁵

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x	x							Any value
		x						PICC compliant with [ISO/IEC 14443-4] if bit is set to (1)b
			x	x				Any value
					x			Cascade bit: UID not complete if bit is set to (1)b
						x	x	Any value

Requirements 5.7: Type A PICC Compliance with ISO/IEC 14443-4

PCD	PICC
5.5.2.1 The PCD shall support a PICC indicating conformity to [ISO/IEC 14443-4]. <i>The PCD may support a PICC not indicating conformity to ISO 14443-4.</i>	5.5.2.2 When the UID is complete (i.e. b3 = (0)b), the PICC shall indicate conformity to [ISO/IEC 14443-4] by setting b6 of the SAK to (1)b.
5.5.2.3 For b3 = (1)b, the PCD shall disregard any other bit of the SAK. For b3 = (0)b, the PCD shall interpret b6 and shall ignore any of the remaining bits of the SAK.	

⁵ A PCD supporting proprietary functionality may interpret any of the bits of the SAK and implement proprietary functionality which is out of scope of this specification.

5.6 HLTA

The HLTA command is used to put the PICC back in the **IDLE** state during the polling and removal procedures.

5.6.1 HLTA Command

The HLTA command consists of two bytes and is transmitted with CRC_A within a standard frame. Table 5.11 specifies the coding of the HLTA command.

Table 5.11: Coding of HLTA Command

Byte 1	Byte 2
'50'	'00'

5.6.2 HLTA Response

The PICC does not respond to a HLTA command. The PCD always assumes that the HLTA command has been ‘acknowledged’ by the PICC.

Requirements 5.8: HLTA Response

PCD	PICC
5.6.2.1 The PCD shall always consider the HLTA command as acknowledged.	5.6.2.2 The PICC shall not respond to a HLTA command.

5.7 Request for Answer to Select (RATS)

The RATS command is used by the PCD during the protocol activation to negotiate with the PICC maximum frame sizes (FSD and FSC), Frame Waiting Time (FWT) and Start-up Frame Guard Time (SFGT).

5.7.1 RATS Command

The RATS command is transmitted with CRC_A within a standard frame. Its coding is specified in Table 5.12.

Table 5.12: Coding of RATS Command

Byte 1	Byte 2
'E0'	PARAM

PARAM, the parameter byte, consists of two parts (see Table 5.13).

Table 5.13: Format of RATS Parameter Byte (PARAM)

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x	x	x	x					FSDI
				x	x	x	x	CID

The most significant nibble b8 to b5 is called FSDI (Frame Size for proximity coupling Device Integer) and codes FSD (Frame Size for proximity coupling Device). Refer to section 4.7.3 for the definition of FSD. The coding of FSD in terms of FSDI is given in Table 5.14.

Table 5.14: FSDI to FSD Conversion

FSDI	'0'	'1'	'2'	'3'	'4'	'5'	'6'	'7'	'8'	'9'	'A'	'B'	'C'	'D'–'F'
FSD (bytes)	16	24	32	40	48	64	96	128	256	512	1024	2048	4096	RFU

Requirements 5.9: FSDI_{MIN}

PCD

- 5.7.1.1 The PCD shall set FSDI greater than or equal to FSDI_{MIN} with a maximum value of 'C'.

Refer to Annex A.4 for the value of FSDI_{MIN}.

Requirements 5.10: PICC Handling of RFU values of FSDI

PICC

- 5.7.1.2 A received value of FSDI = 'D'–'F' shall be treated by the PICC as FSDI = 'C'.

The least significant nibble b4 to b1 is named Card Identifier (CID) and it defines the logical number of the addressed PICC in the range from 0 to 14 (CID = 15 is not allowed). The CID is set to zero as the PCD only addresses a single PICC at a time.

Requirements 5.11: Support of CID

PCD	PICC
5.7.1.3 The PCD shall not use CID, indicated by setting b4-b1 to (0000)b.	5.7.1.4 The PICC shall accept a RATS command with CID in the range from 0 to 14. <i>The PICC may ignore the value of the CID included in the RATS command and indicate in TC(1) that it does not support CID.</i>

5.7.2 RATS Response (Answer To Select)

The Answer To Select (ATS) is transmitted by the PICC in response to the RATS command. The ATS is transmitted with CRC_A within a standard frame. This section defines the ATS with all its available fields (see Table 5.15).

Table 5.15: Structure of the ATS

Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6 – 6+k-1
TL	T0	TA(1)	TB(1)	TC(1)	T1 ... Tk

The length byte TL is followed by a variable number of bytes in the following order:

- Format byte T0
- Interface bytes TA(1), TB(1), TC(1)
- Historical bytes T1 to Tk

Length byte

The length byte TL is mandatory and specifies the length of the transmitted ATS including itself. The two CRC_A bytes are not included in TL.

Requirements 5.12: Length Byte TL of the ATS

PCD	PICC
	5.7.2.1 The first byte of the ATS (TL) shall specify the length of the ATS including TL itself.
5.7.2.2 The PCD shall be capable of supporting a PICC returning an ATS with TL specifying a length less than or equal to 20 bytes.	5.7.2.3 TL shall not indicate a length greater than 20 bytes.
<i>The PCD may support a PICC returning an ATS with TL indicating a length greater than 20 bytes.</i>	

Format Byte T0

The format byte T0 is coded as specified in Table 5.16.

Table 5.16: Coding of Format Byte T0

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0								RFU
	x							TC(1) is transmitted, if bit is set to (1)b
		x						TB(1) is transmitted, if bit is set to (1)b
			x					TA(1) is transmitted, if bit is set to (1)b
				x	x	x	x	FSCI

The least significant nibble b4 to b1 is called FSCI (Frame Size for proximity Card Integer) and codes FSC (Frame Size for proximity Card). Refer to section 4.7.4 for the definition of FSC. The coding of FSC in terms of FSCI is specified in Table 5.17. The default value of FSCI is 2 and leads to an FSC of 32 bytes.

Table 5.17: FSCI to FSC Conversion

FSCI	'0'	'1'	'2'	'3'	'4'	'5'	'6'	'7'	'8'	'9'	'A'	'B'	'C'	'D'-'F'
FSC (bytes)	16	24	32	40	48	64	96	128	256	512	1024	2048	4096	RFU

Requirements 5.13: **FSCI_{MIN}**

PICC

5.7.2.4 The PICC shall set FSCI greater than or equal to **FSCI_{MIN}** with a maximum value of 'C'.

Refer to Annex A.4 for the value of **FSCI_{MIN}**.

Requirements 5.14: PCD Handling of RFU values of FSCI

PCD

5.7.2.5 A received value of FSCI = 'D'-'F' shall be treated by the PCD as FSCI = 'C'.

Requirements 5.15: Format Byte T0 of the ATS

PCD	PICC
5.7.2.6 The PCD shall be capable of supporting a PICC returning an ATS including T0, TA(1), TB(1), and TC(1). If one or more of the fields T0, TA(1), TB(1), and TC(1) are missing, then the PCD shall use the default values as specified in this section.	5.7.2.7 TA(1), TB(1), and TC(1) shall be present in the ATS and the presence shall be indicated in T0.

Interface Byte TA(1)

The interface byte TA(1) conveys information to define the bit rate capabilities of the PICC. The interface byte TA(1) is coded as specified in Table 5.18. Bits b7 to b5 code the bit rate capability of the PICC for the direction from PICC to PCD ($D_{PICC \rightarrow PCD}$). The default value for bits b7 to b5 is (000)b ($D_{PICC \rightarrow PCD} = 1$). Bits b3 to b1 code the bit rate capability of the PICC for the direction from PCD to PICC ($D_{PCD \rightarrow PICC}$). The default value for bits b3 to b1 is (000)b ($D_{PCD \rightarrow PICC} = 1$).

Table 5.18: Coding of Interface Byte TA(1)

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x								If b8 = (1)b, then only the same bit rate divisor for both directions is supported ($D_{PICC \rightarrow PCD} = D_{PCD \rightarrow PICC}$). If b8 = (0)b, then a different bit rate divisor for each direction is supported.
	x							$D_{PICC \rightarrow PCD} = 8$ supported, if bit is set to (1)b.
		x						$D_{PICC \rightarrow PCD} = 4$ supported, if bit is set to (1)b.
			x					$D_{PICC \rightarrow PCD} = 2$ supported, if bit is set to (1)b.
				0				RFU
					x			$D_{PCD \rightarrow PICC} = 8$ supported, if bit is set to (1)b.
						x		$D_{PCD \rightarrow PICC} = 4$ supported, if bit is set to (1)b.
							x	$D_{PCD \rightarrow PICC} = 2$ supported, if bit is set to (1)b.

Requirements 5.16: Format Byte TA(1) of the ATS

PCD	PICC
5.7.2.8 The PCD shall support a bit rate of 106 kbit/s in both directions. <i>The PCD may support higher bit rates.</i>	5.7.2.9 The PICC shall set the bits b7 to b5 and b3 to b1 of TA(1) equal to (0)b, indicating that it supports only a bit rate of 106 kbit/s in both directions.

Requirements 5.17: PCD Handling of RFU bit b4 in TA(1)

PCD
5.7.2.9a A received TA(1) with b4 set to (1)b shall be interpreted by the PCD as if b8 to b1 are set to (00000000)b.

Interface Byte TB(1)

The interface byte TB(1) conveys information to define the Frame Waiting Time (FWT) and the Start-up Frame Guard Time (SFGT). The interface byte TB(1) is coded as specified in Table 5.19.

Table 5.19: Coding of Interface Byte TB(1)

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x	x	x	x					FWI
				x	x	x	x	SFGI

- The most significant nibble b8 to b5 is called FWI (Frame Waiting time Integer) and codes FWT. Refer to section 4.8.1 for the definition of FWT. The default value of FWI is 4 and leads to an FWT of 4.8 ms.

Requirements 5.18: Interface Byte TB(1) of the ATS

PCD	PICC
5.7.2.10a The PCD shall accept FWI less than or equal to FWI_{MAX} . Refer to Annex A.4 for the value of FWI_{MAX} .	5.7.2.10 The PICC shall set FWI less than or equal to FWI_{MAX} . Refer to Annex A.4 for the value of FWI_{MAX} .
5.7.2.10b A received value of FWI = 15 shall be treated by the PCD as FWI = 4.	

- The least significant nibble b4 to b1 codes SFGI (Start-up Frame Guard time Integer) and is used by the PICC to code a multiplier value used to define the SFGT. Refer to section 4.8.2 for the definition of SFGT. The default value of SFGI is 0.

Requirements 5.19: Interface Byte TB(1) of the ATS

PCD	PICC
5.7.2.11 The PCD shall be capable of supporting a PICC returning an ATS with TB(1) indicating an SFGI less than or equal to SFGI_{MAX} .	5.7.2.12 The PICC shall set SFGI less than or equal to SFGI_{MAX} . Refer to Annex A.4 for the value of SFGI_{MAX} .
5.7.2.11a A received value of SFGI = 15 shall be treated by the PCD as SFGI = 0.	

Interface Byte TC(1)

The interface byte TC(1) indicates whether Node ADdress (NAD) and Card Identifier (CID) are supported by the PICC. The interface byte TC(1) is coded as specified in Table 5.20.

Table 5.20: Coding of Interface Byte TC(1)

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0								RFU
	0							RFU
		0						RFU
			0					RFU
				0				RFU
					x			CID supported, if bit is set to (1)b
						x		NAD supported, if bit is set to (1)b

Bits b2 and b1 are used by the PICC to define which optional fields in the prologue field it supports. Bit b1 set to (1)b indicates that NAD is supported; b2 set to (1)b indicates that CID is supported. Refer to section 10.1 for the specification of the prologue field.

Requirements 5.20: Interface Byte TC(1) of the ATS

PCD	PICC
5.7.2.13 The PCD shall not use CID or NAD and shall disregard any value returned by the PICC in b1-b2 of TC(1).	<i>The PICC may support CID and NAD. In this case it should do so according to ISO/IEC 14443.</i>

Historical Bytes

The historical bytes T1 to Tk are optional and are used by the PICC to designate general information.

Requirements 5.21: Historical Bytes of the ATS

PCD	PICC
5.7.2.14 The PCD shall allow the PICC to send up to 15 historical bytes. <i>A PCD may support an ATS with more than 15 historical bytes.</i>	5.7.2.15 The PICC shall send no more than 15 historical bytes.

5.8 Protocol Parameter Selection (PPS)

The PPS command contains the start byte that is followed by two parameter bytes (see Table 5.21). The PPS response acknowledges the received PPS command and it contains only the start byte. A PCD compliant with this specification does not use the PPS command. A PICC compliant with this specification which supports PPS is required to respond correctly to a valid PPS command when it is received as the first block after the PICC has sent the RATS response.

5.8.1 PPS Command

The PPS command is transmitted with CRC_A within a standard frame. The format of the PPS command is defined in Table 5.21.

Table 5.21: Coding of PPS Command

Byte 1	Byte 2	Byte 3
PPSS	PPS0	PPS1

Requirements 5.22: PPS Command

PCD	PICC
5.8.1.1 If the PICC indicates in TA(1) of the ATS that it supports only a bit rate of 106 kbits/s in both directions, then the PCD shall not send a PPS command. <i>If the PICC indicates in TA(1) of the ATS that it supports higher bit rates, then the PCD may send a PPS command.</i>	5.8.1.2 If the PPS command is not the first block received after the PICC has sent the RATS response, the PICC shall ignore the PPS command.

The components of this command are defined as follows:

Coding of PPSS

PPSS consists of two parts. b8 to b5 identify the PPS and b4 to b1 include the CID.

Table 5.22: Coding of PPSS of the PPS Command

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
1	1	0	1					
				x	x	x	x	CID

Coding of PPS0

PPS0 indicates the presence of the optional byte PPS1.

Table 5.23: Coding of PPS0

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0	0	0						Other values are RFU
			x					PPS1 is transmitted if set to (1)b
				0	0	0	1	Other values are RFU

Coding of PPS1

PPS1 conveys information to define the bit rate selection of the PCD compliant with the bit rate capabilities of the PICC indicated in the interface byte TA(1) of the RATS response.

Table 5.24: Coding of PPS1

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0								RFU
	0							RFU
		0						RFU
			0					RFU
				x	x			DSI (selected divisor PICC to PCD)
						x	x	DRI (selected divisor PCD to PICC)

The coding of the selected divisor integer D in terms of DSI and DRI is given in Table 5.25.

Table 5.25: Coding of Selected Divisor Integer

DSI, DRI	(00)b	(01)b	(10)b	(11)b
D	1	2	4	8

Requirements 5.23: PPS1

PICC

- 5.8.1.3 The PICC shall implement the bit rates requested by the PCD in the PPS command after sending the PPS response provided they comply with those proposed by the PICC in TA(1) of the RATS response.
-

5.8.2 PPS Response

The length of the PPS response is one byte and transmitted with CRC_A within a standard frame. The format of the PPS response is defined in Table 5.26.

Table 5.26: Coding of PPS Response

Byte 1
PPSS

Requirements 5.24: PPS Response

PICC

- 5.8.2.1 If the bit rates requested by the PCD in the PPS command do not comply with those proposed by the PICC in TA(1) of the RATS response, the PICC shall not send a PPS response (i.e. ignore the PPS command).
-

PICC

- 5.8.2.2 If the bit rates requested by the PCD in the PPS command comply with those proposed by the PICC in TA(1) of the RATS response the PICC shall send a PPS response with PPSS set to the same value as the PPSS byte of the PPS command.
-

6 Type B – Commands and Responses

This chapter specifies the Type B commands that are available to the PCD for the polling, collision detection, activation and removal procedures. Commands and responses are transmitted within the frames as specified in section 4.7.

6.1 Type B – Command Set

Table 6.1 lists the commands that are available to the PCD for communication with a Type B PICC. All commands and responses use the frame format defined in section 4.7.2 including CRC_B.

Table 6.1: Type B – Command Set

PCD Command	PICC Response
WUPB	ATQB
REQB	ATQB
ATTRIB	Answer to ATTRIB
HLTB	'00'

Requirements 6.1: Protocol Error – Type B

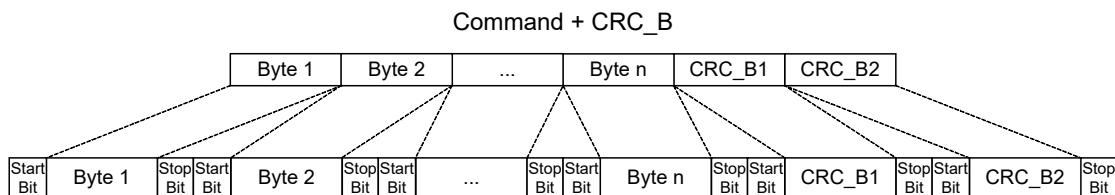
PCD	PICC
6.1.1.1 The PCD shall consider any PICC response transmitted in a valid frame (no transmission error) but having a coding not compliant with this specification, as a protocol error.	6.1.1.2 The PICC shall consider any PCD command transmitted in a valid frame (no transmission error) but having a coding not compliant with this specification, as a protocol error.

6.2 Type B – CRC_B

All of the commands defined in Table 6.1 use a CRC for error checking. The CRC_B is a function of k data bits which consist of all the data bits in the command. Since the commands are encoded in bytes, the number of bits k is a multiple of 8.

Figure 6.1 shows how a command and its CRC_B are included within a frame. CRC_B1 is the least significant byte and CRC_B2 is the most significant byte.

Figure 6.1: Position of a CRC_B within a Frame



Requirements 6.2: CRC_B

PCD and PICC

- 6.2.1.1 The two CRC_B bytes shall be included in the frame after the data bytes.
- 6.2.1.2 The CRC_B shall be as defined in [ISO/IEC 13239]. The initial register content shall be all ones ('FFFF').

6.3 WUPB and REQB

The WUPB and REQB commands are used by the PCD to probe the Operating Field for Type B PICCs.

6.3.1 WUPB and REQB Command

The format of the WUPB and REQB command is defined in Table 6.2.

Table 6.2: WUPB and REQB Command Format

Byte 1	Byte 2	Byte 3
'05'	AFI	PARAM

The components of these commands are defined as follows:

AFI coding

The AFI indicates the application family being selected.

Requirements 6.3: Application Family Indicator (AFI)

PCD	PICC
6.3.1.1 The AFI shall be set to '00'. This selects all application families.	<i>The PICC may support a WUPB command with AFI different from '00'. In this case it should do so according to ISO/IEC 14443.</i>

PARAM Coding

Table 6.3 specifies the coding of PARAM.

Table 6.3: Coding of PARAM Byte Included in WUPB and REQB Command

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0								RFU
	0							RFU
		0						RFU
			x					(0)b: Extended ATQB not supported by PCD (1)b: Extended ATQB supported by PCD
				x				(0)b: REQB (1)b: WUPB
					x	x	x	Number of slots (N)

The Number of slots (N) is used by the anticollision scheme defined in [ISO/IEC 14443-3]. The anticollision scheme is based on the definition of time slots in which PICCs are invited to respond with minimum identification data.

Requirements 6.4: Number of Slots (N)

PCD	PICC
6.3.1.2 The Number of slots (N) shall always be set to (000)b to force all PICCs to respond with ATQB in the first time slot.	<i>The PICC may support a WUPB and REQB command with Number of slots different from (000)b. In this case it should do so according to ISO/IEC 14443 including supporting the Slot-MARKER command and anticollision sequence defined in [ISO/IEC 14443-3] however this functionality is beyond the scope of this specification.</i>

Bit b5 indicates if the PCD supports the Extended ATQB byte. The Extended ATQB byte is an optional byte included in the ATQB response coding the SFGT used by the PICC.

Requirements 6.5: Support for Extended ATQB

PCD	PICC
6.3.1.3 The PCD shall set b5 equal to (0)b (Extended ATQB not supported).	6.3.1.4 When answering a WUPB or REQB command with b5 set to (0)b (Extended ATQB not supported), the PICC shall not include the Extended ATQB byte in its ATQB response. The PICC shall accept a WUPB or REQB command with b5 set to (1)b (Extended ATQB supported). <i>When answering a WUPB command with bit b5 set to (1)b (Extended ATQB supported), the PICC may include an Extended ATQB byte in its ATQB response.</i>

6.3.2 WUPB and REQB Response (ATQB)

The ATQB format is defined in Table 6.4.

Table 6.4: ATQB Format

Byte 1	Byte 2 – 5	Byte 6 – 9	Byte 10 – 12 or 13
'50'	PUPI	Application Data	Protocol Info

Byte 13 of the ATQB is optional. If it is not used, then the ATQB consists of 12 bytes only.

PUPI (Pseudo-Unique PICC Identifier)

A Pseudo-Unique PICC Identifier (PUPI) is used to differentiate between PICCs during collision detection.

Requirements 6.6: PUPI in ATQB

PICC

- 6.3.2.1 The PUPI shall have a length of 4 bytes. The value of the PUPI shall be a fixed number or a random number which is dynamically generated by the PICC.
 - 6.3.2.2 The random PUPI shall only be generated by a state transition from the **POWER-OFF** to the **IDLE** state (see Chapter 8).
-

Application Data

The Application Data field is used to inform the PCD which applications are installed on the PICC.

Requirements 6.7: Application Data Field

PCD

- 6.3.2.3 The PCD shall disregard any value returned by the PICC in the Application Data field.
-

Protocol Info

The Protocol Info indicates the parameters supported by the PICC as detailed in Table 6.5.

Table 6.5: Protocol Info Format

Byte 1	Byte 2		Byte 3			Byte 4 (optional)	
Bit_Rate_Capability (8 bits)	Max_Frame_Size (4 bits)	Protocol_Type (4 bits)	FWI (4 bits)	ADC (2 bits)	FO (2 bits)	SFGI (4 bits)	RFU (4 bits)

- Bit_Rate_Capability**

Bit rates supported by the PICC are specified in Table 6.6. Bits b7 to b5 code the bit rate capability of the PICC for the direction from PICC to PCD ($D_{PICC \rightarrow PCD}$). The value (000)b corresponds with $D_{PICC \rightarrow PCD} = 1$. Bits b3 to b1 code the bit rate capability of the PICC for the direction from PCD to PICC ($D_{PCD \rightarrow PICC}$). The value (000)b corresponds with $D_{PCD \rightarrow PICC} = 1$.

Table 6.6: Bit Rates Supported by the PICC

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x								If b8 = (1)b, then only the same bit rate divisor for both directions is supported ($D_{PICC \rightarrow PCD} = D_{PCD \rightarrow PICC}$). If b8 = (0)b, then a different bit rate divisor for each direction is supported.
	x							$D_{PICC \rightarrow PCD} = 8$ supported, if bit is set to (1)b.
		x						$D_{PICC \rightarrow PCD} = 4$ supported, if bit is set to (1)b.
			x					$D_{PICC \rightarrow PCD} = 2$ supported, if bit is set to (1)b.
				0				RFU
					x			$D_{PCD \rightarrow PICC} = 8$ supported, if bit is set to (1)b.
						x		$D_{PCD \rightarrow PICC} = 4$ supported, if bit is set to (1)b.
							x	$D_{PCD \rightarrow PICC} = 2$ supported, if bit is set to (1)b.

Requirements 6.8: Bit Rates Supported by the PICC

PCD	PICC
<p>6.3.2.4 The PCD shall support a bit rate of 106 kbit/s in both directions. <i>The PCD may support higher bit rates.</i></p>	<p>6.3.2.5 The PICC shall set the bits b7 to b5 and b3 to b1 of the Bit_Rate_Capability equal to (0)b, indicating that it supports only a bit rate of 106 kbit/s in both directions.</p>

Requirements 6.9: PCD Handling of RFU bit b4 in Bit_Rate_Capability

PCD
<p>6.3.2.5a A received Bit_Rate_Capability with b4 set to (1)b shall be interpreted by the PCD as if b8 to b1 are set to (00000000)b.</p>

- **Max_Frame_Size**

Max_Frame_Size codes the maximum frame size (FSC) as specified in section 4.7.4. The maximum frame size in terms of Max_Frame_Size is indicated in Table 6.7.

Table 6.7: FSC in Terms of Max_Frame_Size

Max_Frame_Size	'0'	'1'	'2'	'3'	'4'	'5'	'6'	'7'	'8'	'9'	'A'	'B'	'C'	'D'-'F'
FSC (bytes)	16	24	32	40	48	64	96	128	256	512	1024	2048	4096	RFU

Requirements 6.10: FSCI_{MIN}

PICC
<p>6.3.2.6 The PICC shall set Max_Frame_Size greater than or equal to FSCI_{MIN} with a maximum value of 'C'. Refer to Annex A.4 for the value of FSCI_{MIN}.</p>

Requirements 6.11: PCD Handling of RFU Values of Max_Frame_Size**PCD**

6.3.2.7 A received value of Max_Frame_Size = 'D'–'F' shall be treated by the PCD as Max_Frame_Size = 'C'.

- **Protocol_Type**

The Protocol_Type indicates the protocol type and the minimum TR2 (see Figure 4.31) supported by the PICC as indicated in Table 6.8.

Table 6.8: Protocol_Type

b4	b3	b2	b1	Meaning
0				Must be set to (0)b
	x	x		Minimum TR2
			x	PICC compliance with [ISO/IEC 14443-4] (see Table 6.9)

Table 6.9: Protocol Types Supported by the PICC

b1	Meaning
1	PICC compliant with [ISO/IEC 14443-4]
0	PICC not compliant with [ISO/IEC 14443-4]

Requirements 6.12: Type B Protocol Type supported by the PICC

PCD	PICC
6.3.2.8 The PCD shall be capable of supporting a PICC indicating conformity to [ISO/IEC 14443-4].	6.3.2.9 The PICC shall announce that it supports [ISO/IEC 14443-4]. This means that the PICC shall set b1 to (1)b.
<p><i>The PCD may support a PICC not indicating conformity to [ISO/IEC 14443-4].</i></p> <p>6.3.2.8a The PCD shall resort to exception processing (protocol error) on reception of an ATQB with b4 of Protocol_Type set to (1)b.</p> <p><i>Alternatively, legacy PCDs may optionally ignore bit b4 of Protocol Type. Future versions of this specification may not support this option.</i></p> <p><i>As described in Chapter 9 the ATQB coding is only considered during Collision Detection. The ATQB coding is ignored during Polling and Removal.</i></p>	

Requirements 6.13: Minimum TR2

PCD	PICC
<p>6.3.2.10 The PCD shall disregard any value returned by the PICC in b3 and b2.</p> <p><i>The PCD uses FDT_{B,PCD,MIN} as minimum TR2 as defined in section 4.8.2.</i></p>	<p>6.3.2.11 The PICC shall set bits b3, b2 equal to (00)b.</p> <p><i>The minimum TR2 supported by the PICC is defined by FDT_{B,PCD,MIN} as defined in section 4.8.2 and is independent of the value of b3 and b2.</i></p>

- **FWI – Frame Waiting time Integer (4 bits)**

The FWI codes an integer value used to define the Frame Waiting Time (FWT). Refer to section 4.8.1 for the definition of FWT.

Requirements 6.14: Maximum Value of FWI for Type B

PCD	PICC
<p>6.3.2.12a The PCD shall accept FWI less than or equal to FWI_{MAX}. Refer to Annex A.4 for the value of FWI_{MAX}.</p>	<p>6.3.2.12 The PICC shall set FWI less than or equal to FWI_{MAX}. Refer to Annex A.4 for the value of FWI_{MAX}.</p>
<p>6.3.2.12b A received value of FWI = 15 shall be treated by the PCD as FWI = 4.</p>	

- **ADC**

The ADC represents the Application Data Coding supported by the PICC as indicated in Table 6.10.

Table 6.10: Application Data Coding Supported by the PICC

b4	b3	Meaning
0		RFU
	x	(0)b: proprietary (1)b: as defined in [ISO/IEC 14443-3]

Requirements 6.15: Application Data Coding (ADC)

PCD

6.3.2.13 The PCD shall disregard the value of b3 returned by the PICC in the ADC field.

- **FO**

The Frame Options supported by the PICC are indicated in Table 6.11.

Table 6.11: Frame Options Supported by the PICC

b2	b1	Meaning
x		Node ADdress (NAD) supported, if bit is set to (1)b.
	x	Card Identifier (CID) supported, if bit is set to (1)b.

Requirements 6.16: Frame Options (FO)

PCD	PICC
6.3.2.14 The PCD shall not use CID or NAD and shall disregard any value returned by the PICC in the FO field.	<i>The PICC may support CID and NAD. In this case it should do so according to [ISO/IEC 14443-3].</i>

- **SFGI – Start-up Frame Guard Time Integer (4 bits)**

The most significant nibble b8 to b5 of the optional Extended ATQB byte codes SFGI and is used by the PICC to define the SFGT. Refer to section 4.8.2 for the definition of SFGT. The default value of SFGI is 0.

Requirements 6.17: SFGI

PICC

6.3.2.15 The PICC shall set SFGI less than or equal to **SFGI_{MAX}**.

Refer to Annex A.4 for the value of **SFGI_{MAX}**.

6.4 ATTRIB

The ATTRIB command sent by the PCD includes information required to select the PICC. After receiving a valid ATTRIB command and sending the ATTRIB response, the PICC only responds to commands defined in Chapter 10.

6.4.1 ATTRIB Command

The format of the ATTRIB command is defined in Table 6.12.

Table 6.12: ATTRIB Command Format

Byte 1	Byte 2 – 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10 – 10+k-1
'1D'	PUPI	Param 1	Param 2	Param 3	Param 4	Higher layer – INF

PUPI

Byte 2 through byte 5 include the PUPI sent by the PICC in the ATQB.

Requirements 6.18: PUPI in ATTRIB Command

PCD	PICC
6.4.1.1 The PCD shall send the ATTRIB command using the PUPI received in the valid ATQB from the PICC.	6.4.1.2 The PICC shall recognize its own PUPI and respond only to a valid ATTRIB command in which its PUPI is included.

Coding of Param 1

The PCD codes Param 1 with the values of minimum TR0 and TR1, and whether SoS and EoS are to be used. The coding of Param 1 is specified in Table 6.13.

Table 6.13: Coding of Param 1 of the ATTRIB Command

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x	x							Minimum TR0
		x	x					Minimum TR1
				x	x			Suppression of SoS/EoS
						0		RFU
							0	RFU

Requirements 6.19: Coding of Param 1 of the ATTRIB Command

PCD	PICC
6.4.1.3 The PCD shall set b8 and b7 equal to (00)b indicating that the default minimum value of TR0 (TR0_{MIN}) has to be used (see Annex A.4).	<i>The PICC may support values different from (00)b for b8 and b7. In this case it should do so according to ISO/IEC 14443.</i>
6.4.1.4 The PCD shall set b6 and b5 equal to (00)b indicating that the default minimum value of TR1 (TR1_{MIN}) has to be used (see Annex A.4).	<i>The PICC may support values different from (00)b for b6 and b5. In this case it should do so according to ISO/IEC 14443.</i>
6.4.1.5 The PCD shall set b4 and b3 equal to (00)b indicating that it does not support suppression of SoS/EoS.	<i>The PICC may support suppression of SoS/EoS. In this case it should do so according to ISO/IEC 14443.</i>

Coding of Param 2

The PCD codes Param 2 as specified in Table 6.14.

Table 6.14: Coding of Param 2 of the ATTRIB Command

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x	x							Bit rate PICC → PCD
		x	x					Bit rate PCD → PICC
				x	x	x	x	Max_Frame_Size

The least significant nibble (b4 to b1) of Param 2 is used by the PCD to code the maximum frame size (FSD) that it can receive. Refer to section 4.7.3 for the definition of FSD. The FSD in terms of Max_Frame_Size is indicated in Table 6.15.

Table 6.15: FSD in Terms of Max_Frame_Size

Max_Frame_Size	'0'	'1'	'2'	'3'	'4'	'5'	'6'	'7'	'8'	'9'	'A'	'B'	'C'	'D'–'F'
FSD (bytes)	16	24	32	40	48	64	96	128	256	512	1024	2048	4096	RFU

Requirements 6.20: **FSDI_{MIN}**

PCD

6.4.1.6 The PCD shall set Max_Frame_Size greater than or equal to **FSDI_{MIN}** with a maximum value of 'C'.

Refer to Annex A.4 for the value of **FSDI_{MIN}**.

Requirements 6.21: PICC Handling of RFU values of Max_Frame_Size

PICC

6.4.1.7 A received value of Max_Frame_Size = 'D'–'F' shall be treated by the PICC as Max_Frame_Size = 'C'.

The most significant nibble (b8 to b5) is used by the PCD for bit rate selection, as shown in Table 6.16 and Table 6.17.

Table 6.16: Coding of b8 and b7 of Param 2

b8	b7	Meaning
0	0	$D_{\text{PICC} \rightarrow \text{PCD}} = 1$
0	1	$D_{\text{PICC} \rightarrow \text{PCD}} = 2$
1	0	$D_{\text{PICC} \rightarrow \text{PCD}} = 4$
1	1	$D_{\text{PICC} \rightarrow \text{PCD}} = 8$

Table 6.17: Coding of b6 and b5 of Param 2

b6	b5	Meaning
0	0	$D_{\text{PCD} \rightarrow \text{PICC}} = 1$
0	1	$D_{\text{PCD} \rightarrow \text{PICC}} = 2$
1	0	$D_{\text{PCD} \rightarrow \text{PICC}} = 4$
1	1	$D_{\text{PCD} \rightarrow \text{PICC}} = 8$

Requirements 6.22: Setting the Bit Rate for Type B

PCD	PICC
<i>The PCD may establish bit rates higher than 106 kbit/s, provided they comply with those proposed by the PICC in its ATQB response.</i>	6.4.1.8 The PICC shall implement the bit rates requested by the PCD in the ATTRIB command provided they comply with those proposed by the PICC in its ATQB response.

Coding of Param 3

Param 3 is used for confirmation of the protocol type and is coded as specified in Table 6.18.

Table 6.18: Coding of Param 3 of the ATTRIB Command

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0	0	0	0					All other values are RFU
				0				RFU
					x	x		Minimum TR2
							x	PICC compliance with [ISO/IEC 14443-4] (see Table 6.9)

Requirements 6.23: Coding and Handling of Param 3 of the ATTRIB Command

PCD	PICC
6.4.1.9 The PCD shall set: <ul style="list-style-type: none"> • b3-b2 to (00)b • b1 to (1)b 	6.4.1.9a In the case that b8 to b5 is different from (0000)b, the PICC shall treat it as a protocol error. <i>Some legacy PICCs may ignore bits b8 to b5. Future versions of this specification may not support this option.</i>
	6.4.1.9b The PICC shall ignore the value contained in b3 to b2. <i>In the case that b1 is set to (0)b, the PICC behaviour is proprietary and outside the scope of this specification.</i>

Coding of Param 4

The Param 4 byte is coded as shown in Table 6.19.

Table 6.19: Coding of Param 4 of the ATTRIB Command

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0								RFU
	0							RFU
		0						RFU
			0					RFU
				x	x	x	x	CID

The least significant nibble b4 to b1 is named Card Identifier (CID) and it defines the logical number of the addressed PICC in the range from 0 to 14 (CID = 15 is not allowed). The CID is set to zero as the PCD only addresses a single PICC at a time.

Requirements 6.24: Coding of Param 4 of the ATTRIB Command

PCD	PICC
6.4.1.10 The PCD shall not use CID, indicated by setting b4-b1 of Param 4 to (0000)b.	6.4.1.11 The PICC shall accept an ATTRIB command with CID set to 0.

PCD	PICC
	<p>6.4.1.11a A PICC that indicates support for CID in the ATQB (b1 of byte 3 of Protocol Info set to (1)b) shall accept an ATTRIB command with CID in the range from 1 to 14. A PICC that does not indicate support for CID in the ATQB (b1 of byte 3 of Protocol Info set to (0)b) shall treat an ATTRIB command with CID in the range from 1 to 14 as a protocol error.</p>
	<p>6.4.1.11b The PICC shall treat an ATTRIB command with CID set to 15 as a protocol error.</p>

Higher layer – INF

The ‘Higher layer – INF’ field may include any higher layer command transferable as INF field in the Half-Duplex Block Transmission protocol defined in Chapter 10.

Requirements 6.25: Higher layer – INF

PCD	PICC
6.4.1.12 The PCD shall not include a higher layer command in the Higher layer – INF field. <i>This requirement is not applicable during the personalisation. A PCD used during personalisation may include a higher layer command in the Higher layer – INF field.</i>	6.4.1.13 The PICC shall accept an ATTRIB command with or without Higher layer – INF field.

6.4.2 ATTRIB Response

A PICC is required to answer to any valid ATTRIB command with the format described in Table 6.20. A valid answer to an ATTRIB command is the means for a PCD to verify that PICC selection has been successful.

Table 6.20: ATTRIB Response Format

Byte 1		Byte 2 – 2+n-1
MBLI	CID	Higher layer – Response

- The least significant nibble (b4 to b1) of Byte 1 contains the returned CID.

Requirements 6.26: CID in ATTRIB Response

PCD	PICC
6.4.2.1a The PCD shall resort to exception processing (protocol error) on reception of an ATTRIB response with CID different from the value of the CID in the ATTRIB command.	6.4.2.1 The value of the CID in the ATTRIB response shall be equal to the value of the CID in the ATTRIB command.
<ul style="list-style-type: none">The most significant nibble (b8 to b5) of Byte 1 codes the Maximum Buffer Length Index (MBLI). It is used by the PICC to inform the PCD about its Maximum Buffer Length (MBL) to receive chained frames. MBL is calculated with the following formula:	

$$\text{MBL} = \text{FSC} \times 2^{\text{MBLI}-1}$$

where MBLI is an integer greater than zero. If the PICC returns MBLI = 0, then the PICC provides no information on its internal input buffer size.

Requirements 6.27: MBLI in ATTRIB Response

PCD	PICC
6.4.2.2 The PCD shall disregard any value returned in the MBLI field.	6.4.2.3 The returned MBLI in the ATTRIB response shall always have the value (0000)b.

- The ‘Higher layer – Response’ field includes the answer to the higher layer command included in the ‘Higher layer – INF’ field of the ATTRIB command.

Requirements 6.28: Higher layer – Response

PCD	PICC
6.4.2.4 The PCD shall accept an ATTRIB response with an empty Higher – layer INF field.	6.4.2.5 The PICC shall respond with an empty Higher layer – Response to an ATTRIB command without Higher layer – INF field. <i>The PICC may respond with a Higher layer – Response to an ATTRIB command with Higher layer – INF field.</i> <i>The PICC may also respond with an empty Higher layer – Response to an ATTRIB command with Higher layer – INF field, indicating that the higher layer command is not supported by the PICC.</i>

6.5 HLTB

The HLTB command is used to put a PICC of Type B in the **HALT** state. (Refer to Chapter 8 for the definition of the **HALT** state.)

6.5.1 HLTB Command

The format of the HLTB command is defined in Table 6.21.

Table 6.21: HLTB Command Format

Byte 1	Byte 2 – 5
'50'	PUPI

Byte 2 through byte 5 include the PUPI sent by the PICC in the ATQB.

6.5.2 HLTB Response

The format of the answer to the HLTB command is defined in Table 6.22.

Table 6.22: HLTB Response Format

Byte 1
'00'

7 Type A – PICC State Machine

This chapter specifies the behaviour of a PICC of Type A as a state machine.

7.1 State Diagram

Figure 7.1 shows the state diagram for a PICC of Type A. The state diagram takes all possible state transitions caused by commands specified in Chapter 5 into account.

The following general requirements apply for the Type A state machine.

Requirements 7.1: PICC Type A – State Machine

PICC

- 7.1.1.1 For any state different from the **PROTOCOL** state, the default communication parameters shall be used.
 - 7.1.1.2 The PICC shall send no response when a transmission error is detected.⁶
 - 7.1.1.3 The PICC shall only respond to commands consistent with this specification. The PICC shall send no response when a protocol error is detected.
 - 7.1.1.4 Once the PICC has responded to a Type A command, it shall continue with this technology and respond only to Type A commands until it has been reset and has transitioned from the **POWER-OFF** state to the **IDLE** state, when it may respond to any technology.⁷
-

⁶ Except for the **ACTIVE** state, in which the PICC may return (0001)b or (0101)b when a transmission error is detected. (Refer to requirement 7.2.6.2.)

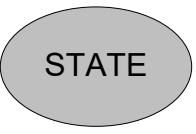
⁷ In the case that the PICC supports a technology other than Type A and Type B, then it may also respond to this technology after the PICC has been placed in the **HALT** state.

PICC

- 7.1.1.5 The PICC shall either go to the **IDLE** or **HALT**⁸ state or be able to continue a transaction in progress⁹ after receiving any Type B command. The PICC shall be able to respond again to a Type A command no later than t_P of unmodulated carrier after receiving the Type B command.

Unless explicitly specified otherwise, once a PICC has responded to a Type A command, it is assumed that it is not expecting a command of another technology and that if one is received, then the resulting state of the PICC is undefined. Similarly it is assumed that the Operating Field is stable enough and provides enough energy to maintain state (e.g. the reduction in field strength associated with the transmission of an unexpected command may result in insufficient energy for the PICC to maintain state).

The following symbols apply for the state diagram:

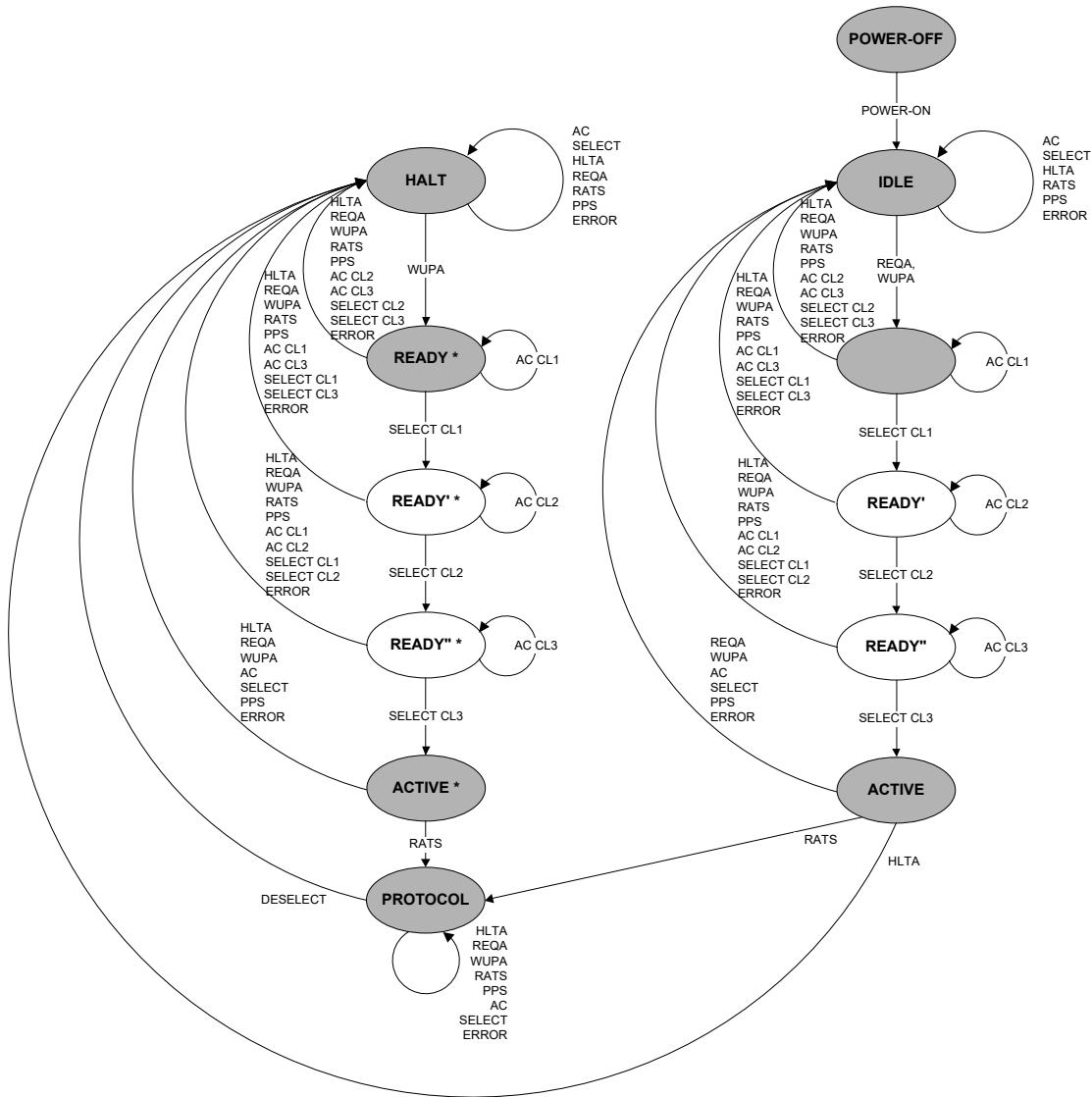
AC	Any ANTCOLLISION command as specified in section 5.4.
AC CLn	ANTICOLLISION command for cascade level n of the UID.
SELECT	Any SELECT command as specified in section 5.5.
SELECT CLn	SELECT command selecting cascade level n of the UID. The UID CLn passed in the SELECT command matches the UID CLn of the PICC.
ERROR	A transmission or protocol error detected. ¹⁰
DESELECT	S(DESELECT) request block as defined in Chapter 10.
	Box representing a state of the PICC that is always present, regardless of the length of the UID.
	Box representing a state of the PICC that may not be present depending on the length of the UID.

⁸ This option is only applicable when either in **READY***, **READY'***, **READY"*** or **ACTIVE*** state.

⁹ The PICC is able to continue a transaction in progress if it remains in the same state and continues to respond as required by that state.

¹⁰ This does not include Type B commands.

Figure 7.1: PICC Type A State Diagram



7.2 Type A PICC States

This section specifies the different states and their transit conditions.

7.2.1 POWER-OFF State

In the **POWER-OFF** state, the PICC is not powered because of a lack of carrier energy.

If the PICC is exposed to an unmodulated carrier, it enters its **IDLE** state no later than t_P as defined by requirement 3.2.8.1.

The PICC moves back to the **POWER-OFF** state no later than t_{RESET} after the Operating Field is switched off as defined by requirement 3.2.7.1. This transition is not shown in Figure 7.1 for clarity.

7.2.2 IDLE State

In the **IDLE** state, the PICC is powered and ready to receive a WUPA or REQA command.

Requirements 7.2: Type A – IDLE State

PICC

- 7.2.2.1 The PICC shall enter the **READY** state after it has received a valid WUPA or REQA command and transmitted its ATQA.
 - 7.2.2.3 The PICC shall ignore all other commands and errors and remain in the **IDLE** state.
-

7.2.3 READY and READY* States

In the **READY** and **READY*** states, the ANTICOLLISION command can be applied to retrieve the complete UID of the PICC.

Requirements 7.3: Type A – READY and READY* States

PICC

- 7.2.3.1 When in the **READY (READY*)** state, a PICC shall remain in the **READY (READY*)** state after it has received a valid ANTICOLLISION CL1 command and transmitted its UID CL1.
- 7.2.3.2 When in the **READY (READY*)** state, a PICC with a single size UID shall enter the **ACTIVE (ACTIVE*)** state after it has received a valid SELECT CL1 command with a matching UID CL1 and transmitted its SAK. The PICC shall indicate in its SAK response that the UID is complete.
- 7.2.3.3 When in the **READY (READY*)** state, a PICC with a double or triple size UID shall enter the **READY' (READY'*)** state after it has received a valid SELECT CL1 command with a matching UID CL1 and transmitted its SAK.
- 7.2.3.4 In all other cases, when in the **READY (READY*)** state, a PICC shall return to the **IDLE (HALT)** state and no response shall be sent to the PCD.

As described in section 7.1, if a command of another technology is received, the resulting state of the PICC is undefined.

7.2.4 READY' and READY'* States

The **READY'** and **READY'*** states are intermediate states that only exist for PICCs with double and triple size UID. In these states, the cascade level 1 of the UID has been selected.

Requirements 7.4: Type A – READY' and READY'* States

PICC

- 7.2.4.1 When in the **READY'** (**READY'***) state, a PICC shall remain in the **READY'** (**READY'***) state after it has received a valid ANTICOLLISION CL2 command and transmitted its UID CL2.
- 7.2.4.2 When in the **READY'** (**READY'***) state, a PICC with a double size UID shall enter the **ACTIVE** (**ACTIVE***) state after it has received a valid SELECT CL2 command with a matching UID CL2 and transmitted its SAK. The PICC shall indicate in its SAK response that the UID is complete.
- 7.2.4.3 When in the **READY'** (**READY'***) state, a PICC with a triple size UID shall enter the **READY"** (**READY"***) state after it has received a valid SELECT CL2 command with a matching UID CL2 and transmitted its SAK.
- 7.2.4.4 In all other cases, when in the **READY'** (**READY'***) state, a PICC shall return to the **IDLE** (**HALT**) state and no response shall be sent to the PCD.

As described in section 7.1, if a command of another technology is received, the resulting state of the PICC is undefined.

7.2.5 READY" and READY"** States

The **READY"** and **READY"**** states are intermediate states that only exist for PICCs with triple size UID. In these states, the cascade level 1 and 2 of the UID have been selected.

Requirements 7.5: Type A – READY" and READY"** States

PICC

- 7.2.5.1 When in the **READY"** (**READY"***) state, a PICC shall stay in the **READY"** (**READY"***) state after it has received a valid ANTICOLLISION CL3 command and transmitted its UID CL3.
- 7.2.5.2 When in the **READY"** (**READY"***) state, a PICC with a triple size UID shall enter the **ACTIVE (ACTIVE*)** state after it has received a valid SELECT CL3 command with a matching UID CL3 and transmitted its SAK.
The PICC shall indicate in its SAK response that the UID is complete.
- 7.2.5.3 In all other cases, when in the **READY"** (**READY"***) state, a PICC shall return to the **IDLE (HALT)** state and no response shall be sent to the PCD.

As described in section 7.1, if a command of another technology is received, the resulting state of the PICC is undefined.

7.2.6 ACTIVE and ACTIVE* States

In the **ACTIVE** and **ACTIVE*** states, the PICC listens to the RATS command for the protocol activation.

Requirements 7.6: Type A – ACTIVE and ACTIVE* States

PICC

- 7.2.6.1 The PICC shall enter the **PROTOCOL** state after it has received a valid RATS command and transmitted its ATS.
- 7.2.6.2 The PICC shall enter the **IDLE** state when a transmission error is detected and either:
 - send no response to the PCD, or
 - send four bits with value (0001)b or (0101)b to the PCD (preceded by a SoF).
- 7.2.6.3 The PICC shall enter the **HALT** state after it has received a valid HLTA command.
- 7.2.6.4 In all other cases, when in the **ACTIVE (ACTIVE*)** state, the PICC shall return to the **IDLE (HALT)** state and no response shall be sent to the PCD.

As described in section 7.1, if a command of another technology is received, the resulting state of the PICC is undefined.

7.2.7 PROTOCOL State

In the **PROTOCOL** state, the PICC listens to any higher layer message.

Requirements 7.7: Type A – PROTOCOL State

PICC

- 7.2.7.1 The PICC shall only reply to valid blocks as defined in Chapter 10 and optionally to the PPS command as defined in Chapter 5. All other Type A commands (i.e. WUPA, REQA, HLTA, AC, SELECT, and RATS) and errors shall be ignored.

As described in section 7.1, if a command of another technology is received, the resulting state of the PICC is undefined.

- 7.2.7.2 The PICC shall enter the **HALT** state when a valid S(DESELECT) request block (as defined in section 10.1) is received.
-

- 7.2.7.3 The PICC shall remain in the **PROTOCOL** state when a PPS command is received and either:
- respond to the PPS command if allowed by the requirements specified in Chapter 5
 - ignore the PPS command
-

7.2.8 HALT State

In the **HALT** state, the PICC only reacts to a WUPA command.

Requirements 7.8: Type A – HALT State

PICC

- 7.2.8.1 When in the **HALT** state, the PICC shall only reply to a valid WUPA command. All other commands and errors shall be ignored.
 - 7.2.8.2 The PICC shall enter the **READY*** state after it has received a valid WUPA command and transmitted its ATQA.
 - 7.2.8.3 A PICC with random UID shall remain in the **HALT** state after it has received a WUPB command.
-

8 Type B – PICC State Machine

This chapter specifies the behaviour of a PICC of Type B as a state machine.

8.1 State Diagram

Figure 8.1 shows the state diagram for a PICC of Type B. The state diagram takes all possible state transitions caused by commands specified in Chapter 6 into account.

The following general requirements apply for the state machine:

Requirements 8.1: PICC Type B – State Machine

PICC

- 8.1.1.1 For any state different from the **ACTIVE** state, the default communication parameters shall be used.
 - 8.1.1.2 The PICC shall send no response when a transmission error is detected.
 - 8.1.1.3 The PICC shall only respond to commands consistent with this specification. The PICC shall send no response when a protocol error is detected.
 - 8.1.1.4 Once the PICC has responded to a Type B command, it shall continue with this technology and respond only to Type B commands until it has been reset and has transitioned from the **POWER-OFF** state to the **IDLE** state, when it may respond to any technology.¹¹
-

¹¹ In the case that the PICC supports a technology other than Type A and Type B, then it may also respond to this technology after the PICC has been placed in the **HALT** state.

-
- 8.1.1.5 The PICC shall either go to the **IDLE** state or be able to continue a transaction in progress¹² after receiving any Type A command. The PICC shall be able to respond again to a Type B command no later than t_P of unmodulated carrier after receiving the Type A command.
-

Unless explicitly specified otherwise, once a PICC has responded to a Type B command, it is assumed that it is not expecting a command of another technology and that if one is received, then the resulting state of the PICC is undefined. Similarly it is assumed that the Operating Field is stable enough and provides enough energy to maintain state (e.g. the reduction in field strength associated with the transmission of an unexpected command may result in insufficient energy for the PICC to maintain state).

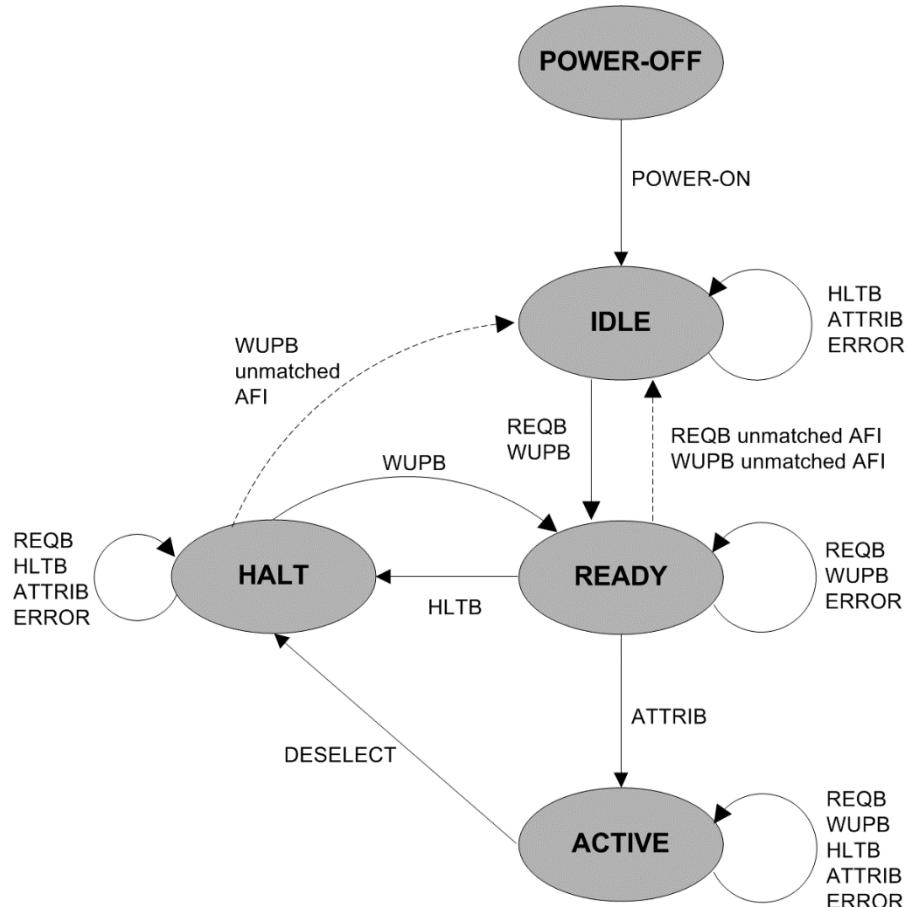
¹² The PICC is able to continue a transaction in progress if it remains in the same state and continues to respond as required by that state.

The following symbols apply for the state diagram:

ERROR Transmission or protocol error detected¹³.

DESELECT S(DESELECT) request block as defined in Chapter 10.

Figure 8.1: PICC Type B State Diagram



¹³ This does not include Type A commands.

8.2 Type B PICC States

This section specifies the different states and their transit conditions.

8.2.1 POWER-OFF State

In the **POWER-OFF** state, the PICC is not powered because of a lack of carrier energy.

If the PICC is exposed to an unmodulated carrier, it enters its **IDLE** state no later than t_P as defined by requirement 3.2.8.1.

The PICC moves back to the **POWER-OFF** state no later than t_{RESET} after the Operating Field is switched off as defined by requirement 3.2.7.1. This transition is not shown in Figure 8.1 for clarity.

8.2.2 IDLE State

In the **IDLE** state, the PICC is powered and ready to receive a WUPB or REQB command.

Requirements 8.2: Type B – IDLE State

PICC

- 8.2.2.1 The PICC shall enter the **READY** state after it has received a valid WUPB or REQB command and transmitted its ATQB.
 - 8.2.2.3 The PICC shall ignore all other commands and errors and remain in the **IDLE** state.
-

8.2.3 READY State

In the **READY** state, the PICC recognizes the ATTRIB command. On receipt of the ATTRIB command the PICC goes to the **ACTIVE** state.

Requirements 8.3: Type B – READY State

PICC

- 8.2.3.1 The PICC shall enter the **ACTIVE** state after it has received a valid ATTRIB command with a PUPI that matches the PUPI of the PICC and transmitted its ATTRIB response.
- 8.2.3.2 The PICC shall remain in the **READY** state and transmit no response after it has received an ATTRIB command with a PUPI that does not match the PUPI of the PICC.
- 8.2.3.3 The PICC shall remain in the **READY** state after it has received a valid WUPB or REQB command and transmitted its ATQB.
- 8.2.3.3a The PICC may enter the **IDLE** state and transmit no response after it has received a WUPB or REQB command containing an AFI different from '00' that does not match the PICC's AFI value.
- 8.2.3.4 The PICC shall enter the **HALT** state after it has received a valid HLTB command and transmitted its HLTB response.
- 8.2.3.5 The PICC shall remain in the **READY** state or return to the **IDLE** state after it has received any Type A command. The PICC shall be able to respond to a WUPB or REQB command no later than t_P of unmodulated carrier after receiving the Type A command.
- 8.2.3.6 The PICC shall ignore all other commands and errors and remain in the **READY** state.

8.2.4 ACTIVE State

In the **ACTIVE** state, the PICC has entered a higher layer mode.

Requirements 8.4: Type B – ACTIVE State

PICC

- 8.2.4.1 The PICC shall enter the **HALT** state when a valid S(DESELECT) request block (as defined in section 10.1) is received.
- 8.2.4.2 The PICC shall only reply to valid blocks as defined in Chapter 10. All Type B commands (i.e. WUPB, REQB, HLTB and ATTRIB) and errors shall be ignored.

As described in section 8.1, if a command of another technology is received, the resulting state of the PICC is undefined.

8.2.5 HALT State

In the **HALT** state, the PICC only responds to a WUPB command.

Requirements 8.5: Type B – HALT State

PICC

- 8.2.5.1 The PICC shall enter the **READY** state after it has received a valid WUPB command and transmitted its ATQB.
- 8.2.5.1a The PICC may enter the **IDLE** state and transmit no response after it has received a WUPB command containing an AFI different from ‘00’ that does not match the PICC’s AFI value.
- 8.2.5.2 The PICC shall ignore all other Type B commands and errors and remain in the **HALT** state.
- 8.2.5.4 A PICC with random PUPI shall remain in the **HALT** state after it has received a WUPA command.

9 PCD Processing

This chapter specifies the functionality implemented in the PCD. This includes the polling, collision detection, activation and removal procedures. The transmission protocol used to process the transaction is specified in Chapter 10. The actual transaction processing is at the application layer and outside the scope of this specification.

This chapter considers the PCD to be a peripheral device of the terminal. The terminal contains the main loop and the different applications.

9.1 Main Loop

This section describes the overall main loop of the terminal. The main loop is implemented by the terminal and makes use of the functionality located in the PCD. This section has two sub-sections. Section 9.1.1 is informative and is used as illustration for the use of the different procedures implemented in the PCD. Section 9.1.2 is normative and contains the requirements on the main loop.

9.1.1 Main Loop – Informative

The terminal and PCD proceed as follows (see also Figure 9.1):

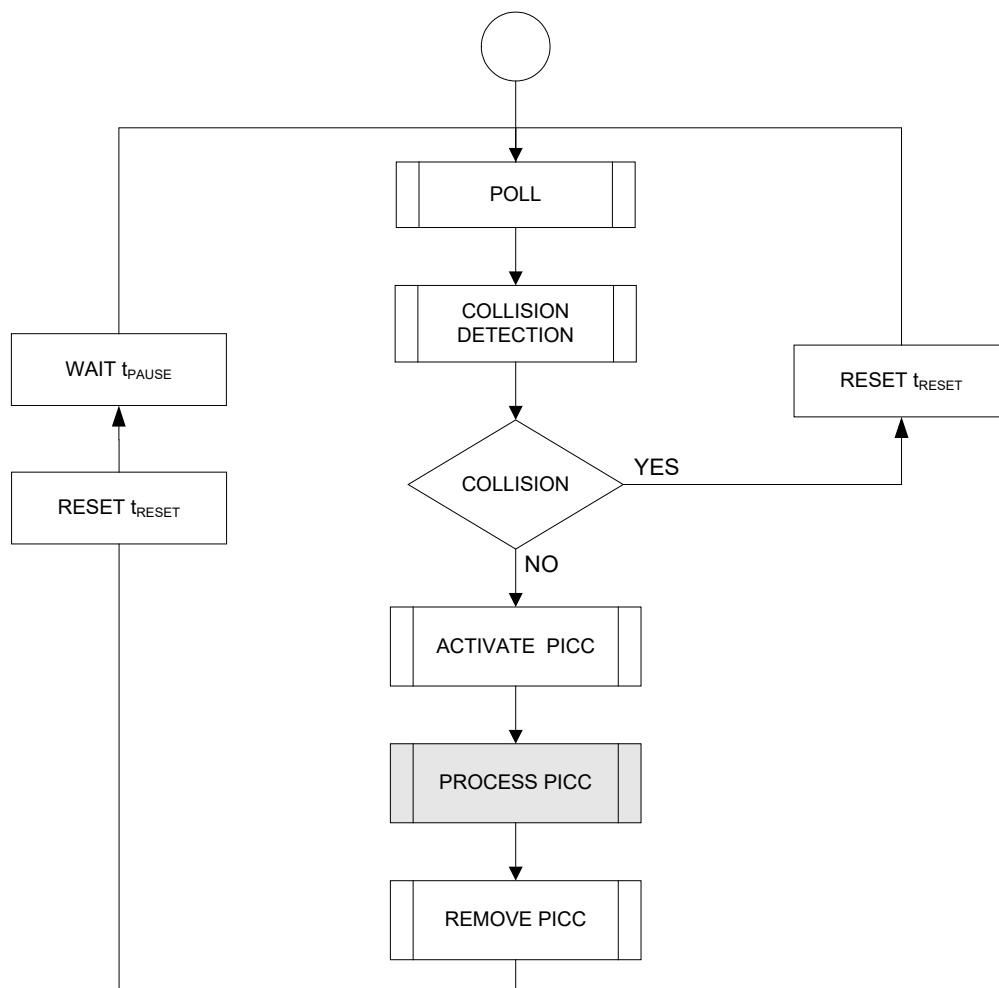
1. To detect PICCs that are in the Operating Field, the PCD performs a power-on of the Operating Field if not already active and polls for the different communication signal interfaces (further on referenced as technologies) supported by the PCD (Type A and Type B are mandatory, other technologies are optional). The polling procedure is specified in section 9.2.
2. During the collision detection procedure, the PCD ensures that there is only a single PICC in the Operating Field. If the PCD receives a response from more than one PICC, then the PCD reports a collision to the terminal, resets the Operating Field (as defined in section 3.2.6) and resumes with the polling.

The collision detection procedure is specified in section 9.3.

3. If there is only one PICC in the Operating Field, then the PCD activates the PICC. The activation procedure is specified in section 9.4.
4. After the PICC has been activated, the PCD installs the half-duplex transmission protocol as specified in Chapter 10 and the terminal application performs the transaction. The transaction processing is situated at the application layer and outside the scope of this specification.

5. In some environments it is necessary to ensure that the PICC has left the field by employing a removal procedure. The removal procedure is specified in section 9.5. When the PICC is removed from the Operating Field, the PCD resets the Operating Field (as defined in section 3.2.6), waits during a time t_{PAUSE} with unmodulated carrier (optional) and resumes with the polling and collision detection (optional). The value of t_{PAUSE} is implementation specific. In other environments where the physical configuration and the way the transaction completes may be sufficient to ensure no overlapping transactions, the removal procedure may be skipped.
6. Finally the terminal may request the PCD to perform a power-off of the Operating Field as described in section 3.2.9.

Figure 9.1: Terminal Main Loop



9.1.2 Main Loop – Normative

The following are PCD requirements related to the main loop:

Requirements 9.1: PCD Requirements Related to the Main Loop

PCD

- 9.1.2.1 The PCD shall only have one technology active during a communication session, i.e. the PCD can communicate either Type A or Type B (or optionally other technologies). The PCD shall not mingle different technologies except under the conditions as described in requirement 9.1.2.2.
- 9.1.2.2 The PCD shall only change from one technology to another during the polling, as described in section 9.2.
- 9.1.2.3 The PCD shall alternate between technologies as specified in section 9.2.
- 9.1.2.4 The PCD shall perform collision detection as specified in section 9.3.
- 9.1.2.5 Only if a single PICC is detected during the collision detection procedure, the PCD shall activate the PICC as specified in section 9.4 to initiate the transaction process.
- 9.1.2.6 During the transaction process the PCD shall use the half-duplex block protocol as specified in Chapter 10 and shall not initiate any communication with another PICC.
- 9.1.2.7 The PCD shall perform the removal procedure as specified in section 9.5, when requested to do so by the terminal.
- 9.1.2.8 The PCD shall perform a power-off of the Operating Field as defined in section 3.2.9, when requested to do so by the terminal.

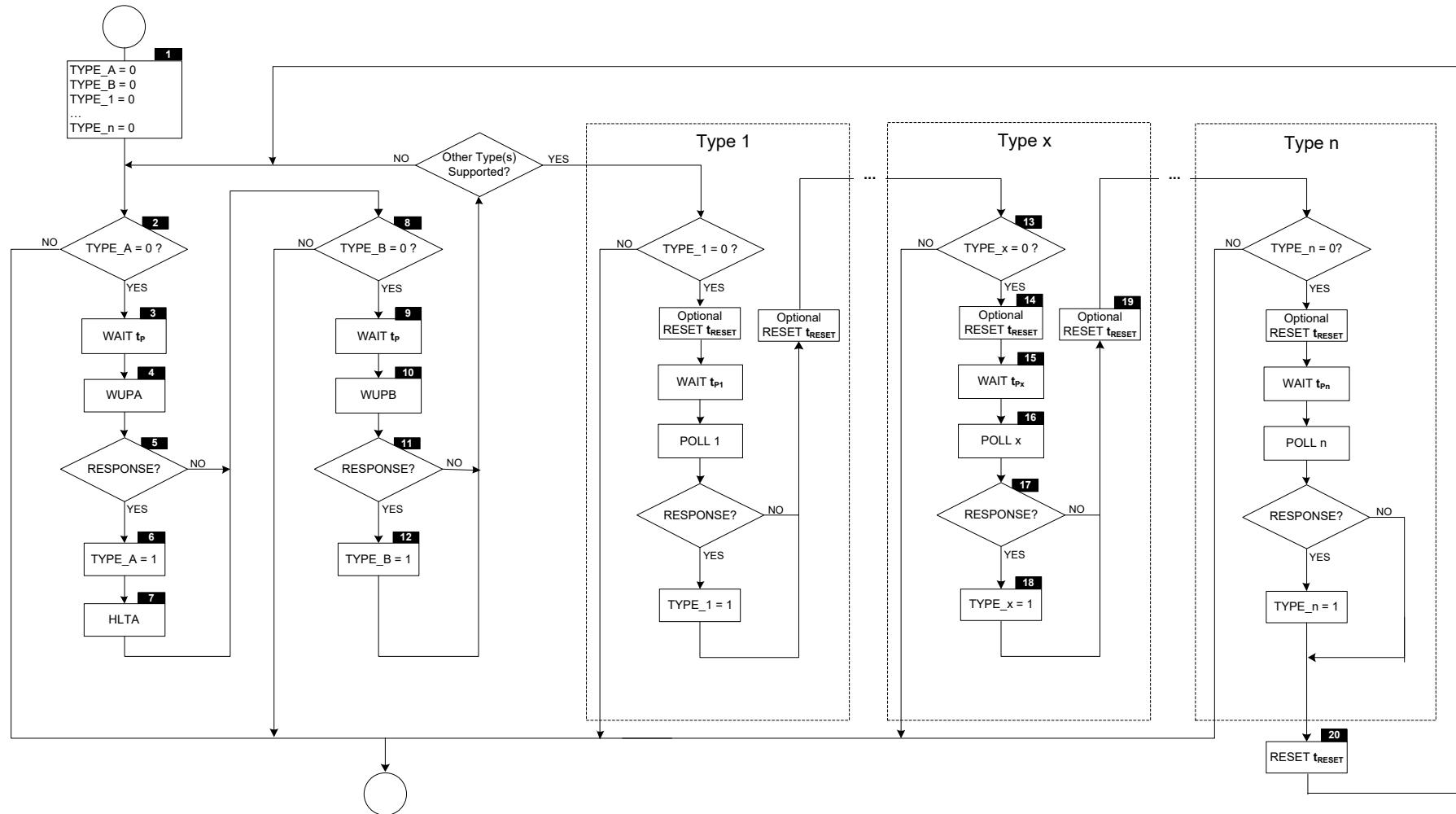
9.2 Polling

This section specifies how the PCD polls for PICCs of different technologies. During the polling, the PCD sends poll commands until a response is received. In one polling cycle, all supported technology poll commands are sent. The PCD completes at least one polling cycle after a technology is detected.

The PCD always polls for Type A and Type B, but may also poll for other technologies. The PCD polls for Type A and Type B by sending WUPA and WUPB commands. The poll commands for other technologies are not defined by this specification. The PCD terminates the polling procedure if at least one technology is detected.

The polling procedure is shown in Figure 9.2.

Figure 9.2: Polling



Requirements 9.2: Polling

PCD

9.2.1.1 The PCD shall poll for Type A and Type B.

The PCD may poll for other technologies.

9.2.1.2 The PCD shall allocate for each supported technology a polling flag and initialize it to zero: TYPE_A = 0, TYPE_B = 0, TYPE_1 = 0, ..., TYPE_n = 0 (symbol 1).

The PCD shall make the polling flags available to the collision detection procedure.

9.2.1.3 The PCD shall check the value of TYPE_A (symbol 2).

If TYPE_A is different from zero,
then the PCD shall conclude the polling procedure and continue with the collision detection procedure.

If TYPE_A is equal to zero, then:

- The PCD shall wait a time t_P with unmodulated carrier (symbol 3) before sending a WUPA command (symbol 4).
- If the PCD receives any response (correct or not) to the WUPA command, then:
 - The PCD shall set TYPE_A equal to 1 (symbol 6) and shall send a HLTA command (symbol 7) to put the PICC(s) back in the **IDLE** state.
 - The PCD shall continue with 9.2.1.4.

PCD

9.2.1.4 The PCD shall check the value of TYPE_B (symbol 8).

If TYPE_B is different from zero,
then the PCD shall conclude the polling procedure and continue
with the collision detection procedure.

If TYPE_B is equal to zero, then:

- The PCD shall wait a time t_P with unmodulated carrier (symbol 9) before sending a WUPB command (symbol 10).
 - If the PCD receives any response (correct or not) to the WUPB command, then:
 - The PCD shall set TYPE_B equal to 1 (symbol 12).
 - The PCD shall continue with 9.2.1.5.
-

9.2.1.5 If the PCD supports only Type A and Type B,
then the PCD shall continue with 9.2.1.3.

Otherwise, the PCD shall continue with 9.2.1.6.

PCD

9.2.1.6 If the PCD supports other technologies, then for each supported technology x , the PCD shall proceed as follows:

- The PCD shall check the value of TYPE_x (symbol 13).
- If TYPE_x is different from zero, then the PCD shall conclude the polling procedure and continue with the collision detection procedure.
- Else if TYPE_x is equal to zero, then:
 - If specifically required by the technology, the PCD shall reset the Operating Field (symbol 14).¹⁴
 - If required by the technology, the PCD shall wait t_{Px} (symbol 15). The value of t_{Px} is proprietary for technology x and may be zero. It is not defined by this specification.
 - The PCD shall send a proprietary polling command for technology x (symbol 16).
 - If the PCD detects a PICC of technology x , the PCD shall set TYPE_x equal to 1 (symbol 18).
 - If specifically required by the technology, the PCD shall reset the Operating Field before moving to the next technology (symbol 19).

Proprietary polling commands shall be different from WUPA/REQA and WUPB/REQB as defined by this specification.

Other technologies (if any) that do not require a reset of the Operating Field (before and/or after) the proprietary polling command, shall be polled before other technologies (if any) that require a reset(s) of the Operating Field.

The PCD shall continue with 9.2.1.7.

PCDs that implement other technologies that require a reset before/after the polling command are responsible for implementing a proprietary process to handle any resulting collisions. For example from PICCs that support the proprietary technology alongside another supported technology.

¹⁴ Resets are not to be applied if not specifically required by the other technology.

PCD

- 9.2.1.7 If the PCD supports other technologies, then the PCD shall reset the Operating Field (as defined in section 3.2.6) before continuing with 9.2.1.3 (symbol 20).

PCDs that implement other technologies are responsible for suppressing any unintentional collision indications. These would occur when PICCs support more than one technology and are due to the same PICC responding both before and after the RESET (symbol 20).

9.3 Collision Detection

This section specifies how the PCD ensures that there is only one PICC in the Operating Field. The terminal will not initiate a transaction when there is more than one PICC.

The PCD first checks if different technologies were detected during the polling procedure. If this is the case, then a collision is reported to the terminal. If only one technology was detected during the polling procedure, the PCD performs collision detection specific to that technology. This specification includes only the technology specific collision detection procedures for Type A and Type B.

9.3.1 General Collision Detection

Requirements 9.3: Collision Detection

PCD

9.3.1.1 The PCD shall check the polling flags.

If more than one polling flag is set to 1, then the PCD shall report a collision to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure. The PCD shall start the reset of the PICC no later than $t_{RESETDELAY}$ measured from the start of the response of the last polling command (i.e. the start of SoF for a Type A polling command and the start of SoS for a Type B polling command as defined in section 4.8).

If only one polling flag is set to 1, then the PCD shall continue with 9.3.1.2.

9.3.1.2 If TYPE_A is set to 1, then the PCD shall continue with the Type A collision detection procedure (see section 9.3.2).

If TYPE_B is set to 1, then the PCD shall continue with the Type B collision detection procedure (see section 9.3.3).

If TYPE_x is set to 1, then the PCD may continue with the collision detection procedure for other technology x.

9.3.2 Type A Collision Detection

This section specifies how the PCD verifies that there is only one Type A PICC in the Operating Field.

The use of Manchester coding and the fact that the Type A PICC answers synchronously to a WUPA command, allows the PCD to detect a collision at bit level for Type A PICCs (i.e. at least two Type A PICCs simultaneously transmit bit patterns with complementary values for one or more bit positions). In this case the bit patterns merge and the carrier is modulated with the subcarrier for the whole (100%) bit duration.

To verify if there is only one Type A PICC in the Operating Field and to retrieve the UID from the PICC, the PCD proceeds as follows (see also Figure 9.3).

Requirements 9.4: Type A Collision Detection

PCD

- 9.3.2.1 The PCD shall wait a time t_P with unmodulated carrier (symbol 0) before sending a WUPA command (symbol 1).
- If the PCD detects a transmission error in the response to the WUPA command,
then the PCD shall report a collision to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).
- Otherwise, the PCD shall continue with 9.3.2.2.
-
- 9.3.2.2 The PCD shall send an ANTICOLLISION command with SEL = '93' (symbol 3).
- If the PCD detects a transmission error in the response to the ANTICOLLISION command,
then the PCD shall report a collision to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).
- Otherwise the PCD shall continue with 9.3.2.3.
-

PCD

9.3.2.3 If the ATQA indicates a single size UID, then:

- The complete UID (= UID CL1: uid₀ uid₁ uid₂ uid₃ BCC) has been retrieved from the PICC. The PCD shall put the PICC in the **ACTIVE** state by sending a SELECT command with SEL = '93' and UID CL1 (symbol 8).
- If the PCD detects a transmission error in the response to the SELECT command, then the PCD shall report a transmission error to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than t_{RESETDELAY} measured from the start of the response (i.e. the start of SoF as defined in section 4.8).

Otherwise the PCD shall conclude the Type A collision detection procedure with one Type A PICC in the Operating Field and proceed with the Type A activation procedure.

PCD

9.3.2.4 If the ATQA indicates a double or triple size UID, then:

- The PCD shall first select cascade level 1 by sending a SELECT command with SEL = '93' and UID CL1 (symbol 6) before continuing with cascade level 2.
- If the PCD detects a transmission error in the response to the SELECT command, then the PCD shall report a transmission error to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).

Otherwise:

- The PCD shall continue with cascade level 2 by sending an ANTICOLLISION command with SEL = '95' (symbol 7).
- If the PCD detects a transmission error in the response to the ANTICOLLISION command, then the PCD shall report a collision to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).

Otherwise the PCD shall continue with 9.3.2.5.

PCD

9.3.2.5 If the ATQA indicates a double size UID, then:

- The complete UID (= UID CL1: CT uid₀ uid₁ uid₂ BCC; UID CL2: uid₃ uid₄ uid₅ uid₆ BCC) has been retrieved from the PICC. The PCD shall put the PICC in the **ACTIVE** state by sending a SELECT command with SEL = '95' and UID CL2 (symbol 13).
- If the PCD detects a transmission error in the response to the SELECT command, then the PCD shall report a transmission error to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).

Otherwise the PCD shall conclude the Type A collision detection procedure with one Type A PICC in the Operating Field and proceed with the Type A activation procedure.

PCD

9.3.2.6 If the ATQA indicates a triple size UID, then:

- The PCD shall first select cascade level 2 by sending a SELECT command with SEL = '95' and UID CL2 (symbol 11) before continuing with cascade level 3.
- If the PCD detects a transmission error in the response to the SELECT command, then the PCD shall report a transmission error to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).

Otherwise:

- The PCD shall continue with cascade level 3 by sending an ANTICOLLISION command with SEL = '97' (symbol 12).
- If the PCD detects a transmission error in the response to this ANTICOLLISION command, then the PCD shall report a collision to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).

Otherwise the PCD shall continue with 9.3.2.7.

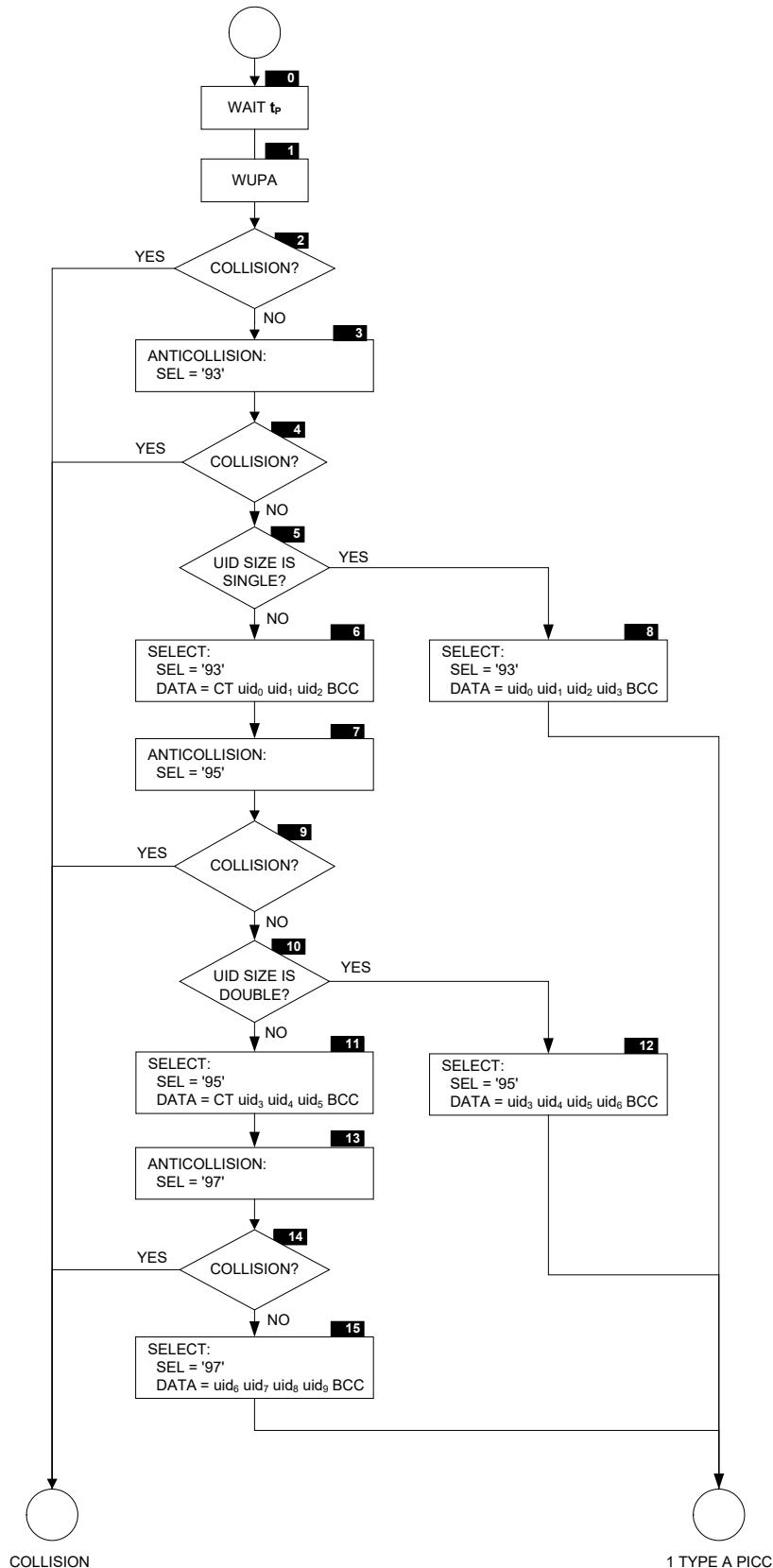
PCD

9.3.2.7 The complete UID (= UID CL1: CT uid₀ uid₁ uid₂ BCC; UID CL2: CT uid₃ uid₄ uid₅ BCC; UID CL3: uid₆ uid₇ uid₈ uid₉ BCC) has been retrieved from the PICC. The PCD shall put the PICC in the **ACTIVE** state by sending a SELECT command with SEL = '97' and UID CL3 (symbol 15).

If the PCD detects a transmission error in the response to the SELECT command, then the PCD shall report a transmission error to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoF as defined in section 4.8).

Otherwise the PCD shall conclude the Type A collision detection procedure with one Type A PICC in the Operating Field and proceed with the Type A activation procedure.

Figure 9.3: Type A Collision Detection



9.3.3 Type B Collision Detection

This section specifies how the PCD verifies that there is only one Type B PICC in the Operating Field.

Type B PICCs do not respond synchronously to a WUPB command. To detect whether more than one Type B PICC is in the Operating Field, the PCD will perform a WUPB command with $N = 1$. This forces all Type B PICCs to respond in the first time slot. If there is more than one Type B PICC in the Operating Field, then the asynchronous responses will cause a transmission error.

To verify if there is only one Type B PICC in the Operating Field, the PCD proceeds as follows (see also Figure 9.4).

Requirements 9.5: Type B Collision Detection

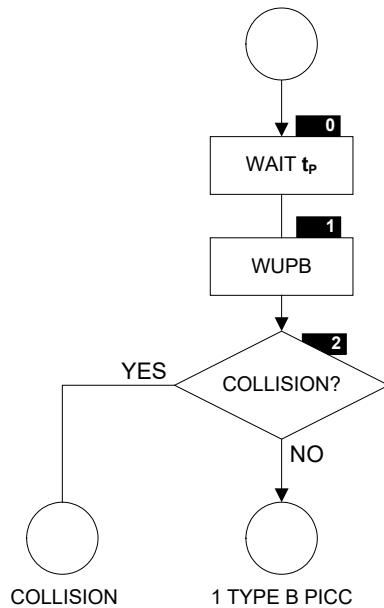
PCD

- 9.3.3.1 The PCD shall wait a time t_P with unmodulated carrier (symbol 0) before sending a WUPB command (symbol 1).

If the PCD detects a transmission error in the response to the WUPB command, then the PCD shall report a collision to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure. It shall reset the Operating Field no later than $t_{RESETDELAY}$ measured from the start of the response (i.e. the start of SoS as defined in section 4.8).

Otherwise, the PCD shall proceed with the Type B activation procedure.

Figure 9.4: Type B Collision Detection



9.4 Activation

This section specifies how the PCD activates a PICC of Type A and Type B.

9.4.1 Type A Activation

This section specifies how the PCD activates a Type A PICC after the PCD concluded that there is only one Type A PICC in the Operating Field.

Requirements 9.6: Type A Activation

PCD

- 9.4.1.1 The PCD shall send a RATS command to move the PICC from the **ACTIVE** state into the **PROTOCOL** state.
- 9.4.1.2 After the PCD has sent the RATS and received a valid ATS, the PCD shall continue with the transaction process (i.e. half-duplex block protocol as specified in Chapter 10).

9.4.2 Type B Activation

This section specifies how the PCD activates a Type B PICC after the PCD has concluded that there is only one Type B PICC in the Operating Field.

Requirements 9.7: Type B Activation

PCD

- 9.4.2.1 The PCD shall send an ATTRIB command to move the PICC from the **READY** state into the **ACTIVE** state.
- 9.4.2.2 After the PCD has sent the ATTRIB command and received a valid ATTRIB response, the PCD shall continue with the transaction process (i.e. half-duplex block protocol as specified in Chapter 10).

9.5 Removal

This section specifies how the PCD proceeds when the removal procedure is requested by the terminal. Figure 9.5 shows that the PCD continues polling until the PICC is removed. The implementation of the removal procedure is mandatory for the PCD, but the removal procedure is only executed upon request from the terminal.

Requirements 9.8: Removal Procedure for Type A

PCD

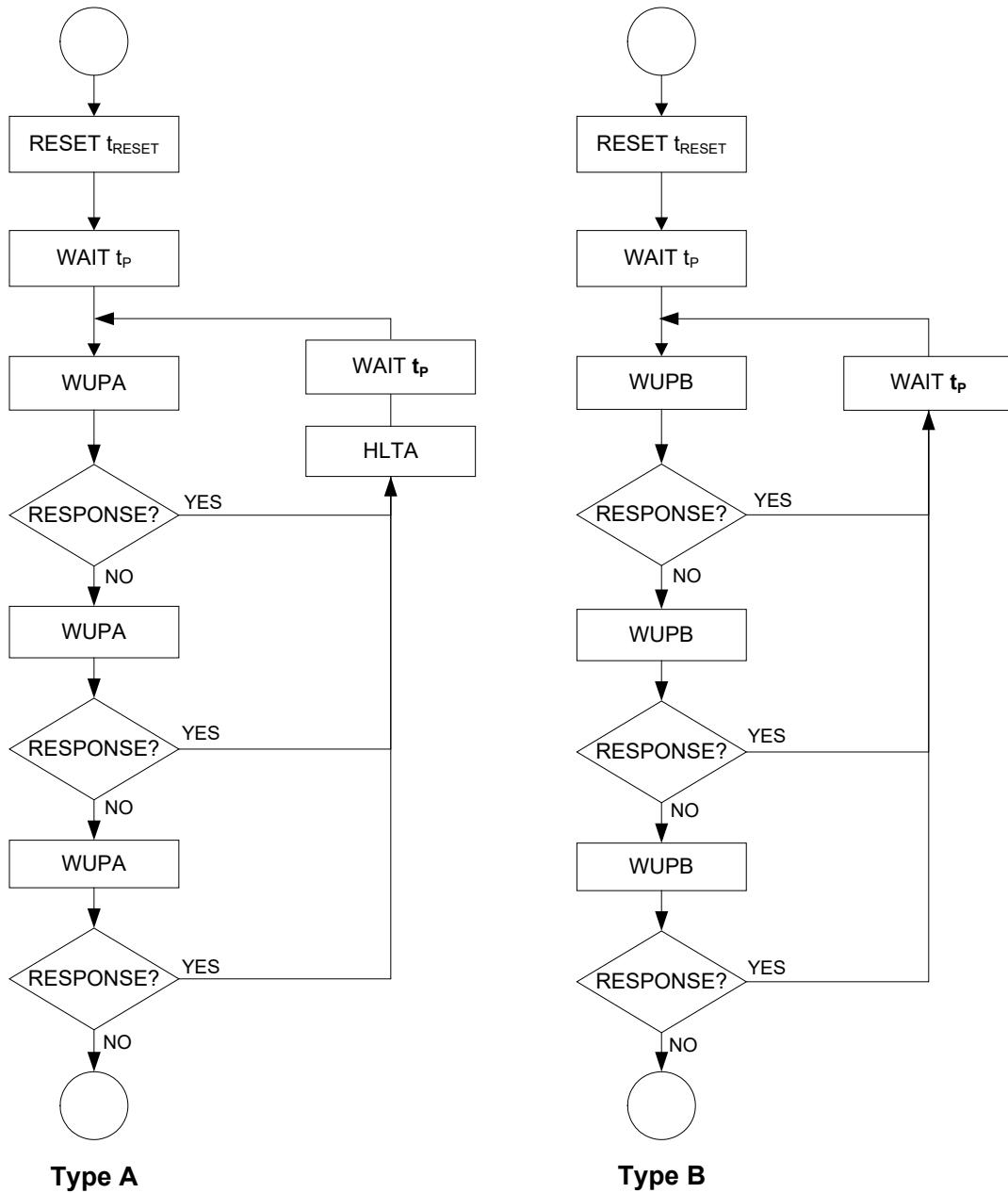
- 9.5.1.1 The PCD shall reset the Operating Field (as defined in section 3.2.6) and wait for a time t_P with unmodulated carrier.
- 9.5.1.2 The PCD shall poll for a PICC of Type A by sending a WUPA command.
 - If the PCD receives any response (correct or not), then the PCD shall continue with 9.5.1.3.
 - If the PCD receives no response to the WUPA command, then the PCD shall continue with 9.5.1.4.
- 9.5.1.3 The PCD shall send a HTLA command to put the PICC back in the **IDLE** state. After sending the HTLA command, the PCD shall wait for a time t_P with unmodulated carrier before continuing with 9.5.1.2.
- 9.5.1.4 The PCD shall send up to two more WUPA commands. The PCD shall retransmit the WUPA commands no later than **tRETRANSMISSION** after the maximum allowed response time (refer to section 4.8).
 - If the PCD receives any response (correct or not), then the PCD shall continue with 9.5.1.3.
 - If no response is received to the third WUPA command, then the PCD shall report a time-out error to the terminal and terminate the removal procedure.

Requirements 9.9: Removal Procedure for Type B

PCD

- 9.5.1.5 The PCD shall reset the Operating Field (as defined in section 3.2.6) and wait for a time t_P with unmodulated carrier.
- 9.5.1.6 The PCD shall poll for a PICC of Type B by sending a WUPB command.
If the PCD receives any response (correct or not), then the PCD shall continue with 9.5.1.7.
If the PCD receives no response to the WUPB command, then the PCD shall continue with 9.5.1.8.
- 9.5.1.7 The PCD shall wait for a time t_P with unmodulated carrier before continuing with 9.5.1.6.
- 9.5.1.8 The PCD shall send a second WUPB command within $\text{FWT}_{\text{ATQB}} + \Delta T_{\text{PCD}} + t_{\text{RETRANSMISSION}}$ after the first WUPB command. If no response is received, then the PCD shall send a third WUPB command within $\text{FWT}_{\text{ATQB}} + \Delta T_{\text{PCD}} + t_{\text{RETRANSMISSION}}$ after the second WUPB command.
If the PCD receives any response (correct or not) to the second or third WUPB command, then the PCD shall continue with 9.5.1.7.
If no response is received to the third WUPB command, then the PCD shall report a time-out error to the terminal and terminate the removal procedure.

Figure 9.5: Removal of PICC of Type A and PICC of Type B



9.6 Exception Processing

This section specifies how the PCD proceeds in case an exception occurs for a PICC that is not in the **PROTOCOL** (for Type A) or **ACTIVE** (for Type B) state. Refer to Chapter 10 for the PCD error handling in the case an exception occurs for a PICC that is in the **PROTOCOL** (for Type A) or **ACTIVE** state (for Type B).

Requirements 9.10: Exception Processing

PCD

- 9.6.1.1 During the activation procedure, on detection of a response with a transmission error, the PCD shall report the transmission error to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure.

The PCD shall start the reset of the PICC no later than $t_{RESETDELAY}$ measured from the start of the invalid response (i.e. the start of SoF for Type A response and the start of SoS for a Type B response as defined in section 4.8).

Note that the transmission error is suppressed by the EMD handling defined in section 4.9.2 if the transmission error is detected when less than 4 bytes have been received from the PICC.

- 9.6.1.2 On detection of a protocol error (except during the polling and removal procedures):
- The PCD shall report the protocol error to the terminal, reset the Operating Field (as defined in section 3.2.6), and return to the polling procedure.
 - The PCD shall start the reset of the PICC no later than $t_{RESETDELAY}$ measured from the start of the response frame containing the protocol error (i.e. the start of SoF for Type A response and the start of SoS for a Type B response as defined in section 4.8).

PCD

9.6.1.3 On detection of a time-out error (except during the polling and removal procedures):

- The PCD shall retransmit the command a maximum of two times.
 - For the SELECT and ANTICOLLISION commands, the PCD shall retransmit the command after $FDT_{PICC,MAX} + t_{MIN,RETRANSMISSION}$ and before $FDT_{PICC,MAX} + t_{RETRANSMISSION}$.
 - For the RATS and ATTRIB commands, the PCD shall retransmit the command after $FDT_{PICC,MAX} + t_{MIN,RETRANSMISSION}$ and before $FDT_{PICC,MAX} + \Delta T_{PCD} + t_{RETRANSMISSION}$.

Refer to Annex A.5 for the value of $t_{MIN,RETRANSMISSION}$.

- If on the second retransmission (third transmission), no valid response has been received:
 - The PCD shall report a time-out error to the terminal, reset the Operating Field (as defined in section 3.2.6) and return to the polling procedure.
 - The PCD shall start the reset of the PICC no later than $t_{RESETDELAY}$ after the maximum allowed response time applicable for the command.

10 Half-Duplex Block Transmission Protocol

This chapter defines the high-level data transmission protocol. The half-duplex block transmission protocol defined in this chapter is common for Type A and Type B. Blocks defined in this chapter are transferred as data bytes in frames as defined in section 4.7.

10.1 Block Format

The block format as shown in Figure 10.1 consists of a prologue field (mandatory), an information field (optional) and an epilogue field (mandatory).

Figure 10.1: Block Format

Prologue field	Information Field	Epilogue field
PCB (1 byte)	[INF]	EDC (2 bytes)

10.1.1 Block Length

The PCD and PICC requirements related to the total length of a block are included in section 4.7.

10.1.2 Prologue Field

The prologue field is mandatory and contains the Protocol Control Byte (the CID and NAD defined in [ISO/IEC 14443-4] are not used). The Protocol Control Byte (PCB) is used to convey the information required to control the data transmission. The protocol defines three fundamental types of blocks:

- I-block used to convey information for use by the application layer.
- R-block used to convey positive or negative acknowledgements. An R-block never contains an INF field. The acknowledgement relates to the last received block.
- S-block used to exchange control information between the PCD and the PICC. Two different types of S-blocks are defined:
 - 1) Waiting Time eXtension (WTX) containing a 1 byte long INF field
 - 2) DESELECT containing no INF field

The coding of the PCB depends on its type as shown in Table 10.1.

Table 10.1: Coding of b8-b7 of PCB

b8	b7	Meaning
0	0	I-block
0	1	Not allowed
1	0	R-block
1	1	S-block

The coding of I-blocks, R-blocks and S-blocks are shown in Table 10.2, Table 10.3 and Table 10.4.

Table 10.2: Coding of I-block PCB

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0	0							I-block
		0						Must be set to (0)b ⁽¹⁾
			x					Chaining, if bit is set to (1)b
				0				CID following, if bit is set to (1)b
					0			NAD following, if bit is set to (1)b
						1		Must be set to (1)b
							x	Block number

⁽¹⁾ Requirement 10.1.5.1 applies when an I-block is received with b6 set to (1)b. Alternatively, legacy PCDs and PICCs may optionally ignore bit b6. Future versions of this specification may not support this option.

Table 10.3: Coding of R-block PCB

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
1	0							R-block
		1						Must be set to (1)b
			x					ACK if bit is set to (0)b, NAK if bit is set to (1)b
				0				CID following, if bit is set to (1)b
					0			Must be set to (0)b
						1		Must be set to (1)b ⁽¹⁾
							x	Block number

⁽¹⁾ Requirement 10.1.5.1 applies when an R-block is received with b2 set to (0)b. Alternatively, legacy PCDs and PICCs may optionally ignore bit b2. Future versions of this specification may not support this option.

Table 10.4: Coding of S-block PCB

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
1	1							S-block
		x	x					If b2 = (0)b, then must be set to (11)b If b2 = (1)b, then (00)b: DESELECT (01)b: Not allowed (10)b: Not allowed (11)b: WTX
				0				CID following, if bit is set to (1)b
				0				Must be set to (0)b
					x			PARAMETERS if set to (0)b DESELECT or WTX if set to (1)b
						0		Must be set to (0)b ⁽¹⁾

- ⁽¹⁾ Requirement 10.1.5.1 applies when an S-block is received with b1 set to (1)b.
 Alternatively, legacy PCDs and PICCs may optionally ignore bit b1. Future versions of this specification may not support this option.

Requirements 10.1: Coding of S-block PCB

PCD	PICC
10.1.2.1 b2 of the S-block PCB shall be set to (1)b.	10.1.2.2 b2 of the S-block PCB shall be set to (1)b.
10.1.2.3 A PCD receiving an S-block PCB with b2 set to (0)b, shall handle this setting as a protocol error.	10.1.2.4 A PICC receiving an S-block PCB with b2 set to (0)b, shall handle this setting as a: <ul style="list-style-type: none"> - protocol error, or - S(PARAMETERS) block (out of scope of this specification)

10.1.3 Information Field

The INF field is optional. When present, the INF field conveys either application data in I-blocks or non-application data and status information in S-blocks. The length of the information field is calculated by counting the number of bytes of the whole block minus the length of the prologue and epilogue fields.

10.1.4 Epilogue field

The epilogue field contains the Error Detection Code (EDC) of the transmitted block, which is the CRC as defined in section 5.2 for a Type A PICC and in section 6.2 for a Type B PICC.

10.1.5 Protocol Error

Requirements 10.2: Protocol Error

PCD and PICC

- 10.1.5.1 A block received within a valid frame but with a coding not compliant with this specification (e.g. PCB not compliant with this specification), shall be considered as a protocol error.
-

10.2 Frame Waiting Time Extension

When the PICC needs more time than the defined FWT to process the received block it uses an S(WTX) request for a waiting time extension. An S(WTX) request contains a 1 byte long INF field as specified in Table 10.5.

Table 10.5: Coding of INF Field of an S(WTX) Request

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
x	x							Power level indication
		x	x	x	x	x	x	WTXM

10.2.1 Power Level Indicator

The two most significant bits b8 and b7 code the power level indication.

Requirements 10.3: Power Level Indication

PCD	PICC
<i>The PCD may support a Power level indication different from (00)b.</i>	10.2.1.1 The Power level indication is not used and the bits shall be set to (00)b.

10.2.2 WTXM

The least significant bits b6 to b1 code WTXM. WTXM is coded in the range from 1 to 59.

The PCD acknowledges by sending an S(WTX) response containing also a 1 byte INF field that consists of two parts containing the same WTXM as received in the request (see Table 10.6).

Table 10.6: Coding of INF Field of an S(WTX) Response

b8	b7	b6	b5	b4	b3	b2	b1	Meaning
0	0							Must be set to (00)b ⁽¹⁾
		x	x	x	x	x	x	WTXM

⁽¹⁾ Requirement 10.1.5.1 applies when an S(WTX) response is received with b8-b7 set to (00)b. Alternatively, legacy PICCs may optionally ignore bits b8-b7. Future versions of this specification may not support this option.

Requirements 10.4: RFU Handling of S(WTX) Response

PICC

10.2.1.1a The PICC shall treat b8 to b7 different from (00)b as a protocol error.

Alternatively, legacy PICCs may optionally ignore bits b8 to b7. Future versions of this specification may not support this option.

The corresponding temporary value of FWT is calculated by the following formula:

$$FWT_{TEMP} = FWT \times WTXM.$$

The time FWT_{TEMP} requested by the PICC starts after the PCD has sent the S(WTX) response.

Requirements 10.5: Frame Waiting Time Extension

PCD	PICC
<p>10.2.2.1 The PCD shall accept an S(WTX) having a WTXM with a value in the range from 1 to 59.</p> <p>The PCD shall resort to exception processing (protocol error) on reception of an S(WTX) having a WTXM set to 0 or a value in the range from 60 to 63.</p> <p><i>Alternatively, legacy PCDs may optionally treat a WTXM in the range from 60 to 63 as value 59. Future versions of this specification may not support this option.</i></p>	<p>10.2.2.2 The PICC shall code WTXM in the range from 1 to 59.</p>
<p>10.2.2.3 The PCD shall support a frame waiting time extension less than or equal to FWT_{MAX} (i.e. $FWT_{TEMP} \leq FWT_{MAX}$).</p>	<p>10.2.2.4 The PICC shall code WTXM such that FWT_{TEMP} is less than or equal to FWT_{MAX}.</p> <p><i>This requirement is applicable after personalisation of the PICC. The PICC may code WTXM such that FWT_{TEMP} is greater than FWT_{MAX} during the initialization and personalisation phase.</i></p>
<p>10.2.2.5 The PCD shall code WTXM in the S(WTX) response with the same value as the value of WTXM in the S(WTX) request.</p>	<p>10.2.2.6 The PICC shall consider a WTXM in the S(WTX) response with a value different from the value of WTXM in the S(WTX) request as a protocol error.</p>

PCD	PICC
<p>10.2.2.7 After sending the S(WTX) response block in response to an S(WTX) request block from the PICC, the PCD shall wait for at least $FWT_{TEMP} + \Delta FWT$ for a block of the PICC.</p> <p>If the PCD does not receive a block from the PICC within $FWT_{TEMP} + \Delta FWT + \Delta T_{PCD}$, then the PCD shall resort to exception processing (time-out error).</p> <p>Refer to Annex A.4 for the values of ΔT_{PCD}.</p> <p><i>Between $FWT_{TEMP} + \Delta FWT$ and $FWT_{TEMP} + \Delta FWT + \Delta T_{PCD}$, the PCD may accept the response of the PICC or may generate a time-out error.</i></p>	<p>10.2.2.8 After receiving the S(WTX) response block of the PCD, the PICC shall start sending the next block within FWT_{TEMP}.</p>
<p>10.2.2.9 The PCD shall apply $FWT_{TEMP} + \Delta FWT$ only until the next block has been received from the PICC or until the PCD resorts to exception processing.</p>	<p>10.2.2.10 The PICC shall apply FWT_{TEMP} only until the next block has been sent by the PICC.</p>

10.3 Protocol Operation

10.3.1 General Rules

This section specifies the rules for the half-duplex transmission protocol.

Requirements 10.6: General Rules for Half-Duplex Transmission Protocol

PCD	PICC
10.3.1.1 After sending a block, the PCD shall switch to receive mode and wait for a block before switching back to transmit mode.	10.3.1.2 After the activation of the PICC, the PICC shall wait for a block as only the PCD has the right to send.
10.3.1.3 The PCD shall not initiate a new command/response pair until the current command/response pair has been completed or until the frame waiting time has been exceeded with no response.	10.3.1.4 The PICC shall send a block only when it has received a valid block from the PCD. After responding, the PICC shall return to the receive mode.

10.3.2 Chaining

The chaining feature allows the PCD or PICC to transmit information that does not fit in a single block as defined by FSC or FSD respectively, by dividing the information into several blocks.

Requirements 10.7: General Chaining Rule

PCD and PICC
10.3.2.1 The chaining bit in the PCB of an I-block controls the chaining of blocks. When an I-block indicating chaining is received, the block shall be acknowledged by an R(ACK) block. <i>This requirement applies even if the INF field of the received I-block has zero length.</i>

Requirements 10.8: Chaining Invocation

PCD	PICC
<p>10.3.2.1a The PCD shall invoke chaining when the number of data bytes in the frame to be sent exceeds the minimum of:</p> <ul style="list-style-type: none">• FSC indicated by the PICC, and• Maximum FSC supported by the PCD which shall be at least 256 bytes. Refer to Table 5.17 (for Type A) and Table 6.7 (for Type B) for possible values of FSC greater than 256 bytes.	<p>10.3.2.1b The PICC shall invoke chaining when the number of data bytes in the frame to be sent exceeds the minimum of:</p> <ul style="list-style-type: none">• FSD indicated by the PCD, and• Maximum FSD supported by the PICC. Refer to Table 5.14 (for Type A) and Table 6.15 (for Type B) for all possible FSD values.

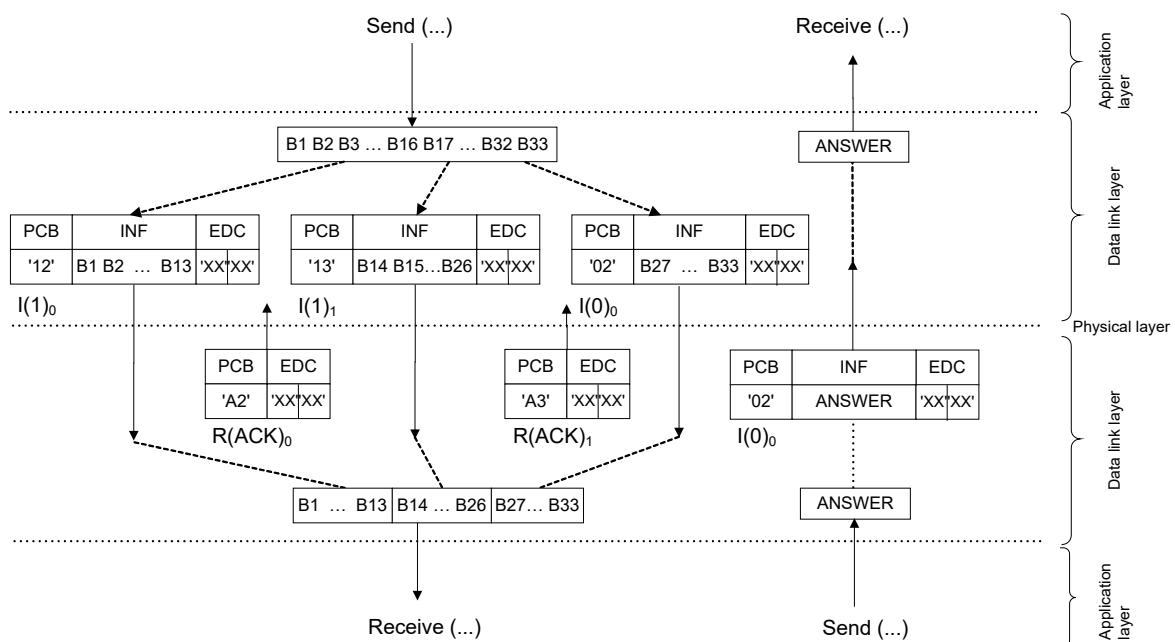
Requirements 10.9: Block Sizes during Chaining

PCD	PICC
<p>10.3.2.2 When the PCD sends a chain of I-blocks, each block indicating chaining (i.e. all blocks of the chain except the last one) shall have a length equal to the minimum of:</p> <ul style="list-style-type: none">• FSC indicated by the PICC, and• Maximum FSC supported by the PCD which shall be at least 256 bytes. Refer to Table 5.17 (for Type A) and Table 6.7 (for Type B) for possible values of FSC greater than 256 bytes.	
<p><i>When the PCD sends a chain of I-blocks, the INF field of the last block may have a length equal to zero.</i></p>	<p>10.3.2.3 The PICC shall accept a chain of I-blocks of which the INF field of the last block has a length equal to zero.</p>
	<p>10.3.2.4 When the PICC sends a chain of I-blocks, each block indicating chaining (i.e. all blocks of the chain except the last one) shall have an INF field with a length different from zero.</p>

An example of the chaining feature is shown in Figure 10.2. The example shows a 33 byte long string transmitted in three blocks (FSC = 16). It uses the following notation:

- I(1)x I-block with chaining bit set and block number x
- I(0)x I-block with chaining bit not set (last block of chain) and block number x
- R(ACK)x R-block that indicates a positive acknowledgement

Figure 10.2: Chaining



10.3.3 Block Numbering Rules

This section specifies the rules for the block numbering in the PCD block.

Requirements 10.10: Block Numbering Rules

PCD	PICC
10.3.3.1 The PCD block number shall be initialized to 0 for the current activated PICC.	10.3.3.2 The PICC block number shall be initialized to 1 at activation.
10.3.3.3 When a correct I-block or a correct R(ACK) block with a block number equal to the current block number is received, the PCD shall toggle the current block number for the current PICC before optionally sending a block.	10.3.3.4 When an I-block is received, the PICC shall toggle its block number immediately after receiving the I-block. <i>The PICC may check if the received block number is not in compliance with the PCD rules to decide not to toggle its internal block number nor send a response block.</i>
	10.3.3.5 When an R(ACK) block with a block number not equal to the current PICC's block number is received, the PICC shall toggle its block number immediately after receiving the R(ACK) block. <i>The PICC may check if the received block number is not in compliance with the PCD rules to decide not to toggle its internal block number nor send a response block.</i>

10.3.4 Block Handling Rules

This section specifies the block handling rules for the PCD and the PICC.

Requirements 10.11: Block Handling Rules for both PCD and PICC

PCD and PICC

- 10.3.4.1 The first block shall be sent by the PCD.
 - 10.3.4.2 S(WTX) blocks are only used in pairs. An S(WTX) request block shall always be followed by an S(WTX) response block.
-

Requirements 10.12: Block Handling Rules for the PCD

PCD

- 10.3.4.3 When an R(ACK) block is received with a block number not equal to the PCD's current block number, then the PCD shall re-transmit the last I-block if this R(ACK) block is received in response to an R(NAK) block sent by the PCD to notify a time-out.
In all other cases, when an R(ACK) block with a block number not equal to the PCD's current block number is received, then the PCD may directly report a protocol error to the terminal or the PCD may re-transmit the last I-block.
 - 10.3.4.4 When the PCD has re-transmitted an I-block two times (i.e. same I-block sent 3 times),
if an R(ACK) block with a block number not equal to the PCD's current block number is received,
it shall be considered as a protocol error.
 - 10.3.4.5 When an R(ACK) block is received, if its block number is equal to the PCD's current block number and the last I-block sent by the PCD indicated chaining, then chaining shall be continued.
If the last I-block sent by the PCD did not indicate chaining, then the PCD shall consider the R(ACK) block as a protocol error.
 - 10.3.4.6 When an R(NAK) block is received by the PCD, it shall be considered as a protocol error.
-

Requirements 10.13: Block Handling Rules for the PICC

PICC

10.3.4.7 The PICC is permitted to send an S(WTX) block instead of an I-block or an R(ACK) block (except in the case of a retransmitted I-block or a retransmitted R(ACK) block).

10.3.4.8 When an I-block not indicating chaining is received, the block shall be acknowledged by an I-block.

If the I-block received has a zero length INF field then the mandatory I-block sent may either have a zero length INF field or may contain any applicative information.

If the I-block with zero length INF field that is received by the PICC is the last I-block of a chain, then the I-block sent by the PICC may only have a zero length INF field if all I-blocks of the chain that is received by the PICC have a zero length INF field.

10.3.4.9 When an R(ACK) or an R(NAK) block is received with a block number equal to the PICC's current block number, then the last block shall be retransmitted.

If an R(ACK) is received with a block number equal to the PICC's current block number and the PICC is not chaining (i.e. the last I-block sent by the PICC was not the start, middle nor end of a chain), then the PICC may consider the R(ACK) block as a protocol error.

10.3.4.10 When an R(NAK) block is received, if its block number is not equal to the PICC's current block number, an R(ACK) block shall be sent.

10.3.4.11 When an R(ACK) block is received, if its block number is not equal to the PICC's current block number, and the last I-block sent by the PICC indicated chaining, chaining shall be continued.

If the last I-block sent by the PICC did not indicate chaining, then the PICC may consider the R(ACK) block as a protocol error.

10.3.5 Exception Processing

This section describes the error handling to be attempted when errors are detected.

Requirements 10.14: Exception Processing – PICC

PICC

- 10.3.5.1 The PICC shall detect transmission errors (frame error or EDC error) and protocol errors (infringement of the protocol rules) unless explicitly specified otherwise.
- 10.3.5.2 The PICC shall attempt no error recovery. The PICC shall always stay in receive mode when a transmission error or a protocol error occurs.

Note that an R(NAK) block is never sent by the PICC.

Requirements 10.15: Exception Processing – PCD

PCD

- 10.3.5.3 If a block with a transmission error is received after receipt of a block not indicating chaining, then the PCD shall send an R(NAK) block.

The PCD shall send the R(NAK) block no later than $t_{RETRANSMISSION}$ after the end of the modulation of the block with the transmission error.

The PCD shall send up to two consecutive R(NAK) blocks to ask for retransmission.

If a block with a transmission error in response to the second R(NAK) block is received,
then the PCD shall report a transmission error to the terminal and continue as specified in 10.3.5.9 no later than $t_{RESETDELAY}$ after the end of the modulation of the last block with the transmission error.

Note that the transmission error is suppressed by the EMD handling defined in section 4.9.2 if the transmission error is detected when less than 4 bytes have been received from the PICC.

- 10.3.5.4 If a block with a protocol error is received after receipt of a block not indicating chaining, then the PCD shall report a protocol error to the terminal and continue as specified in 10.3.5.9 no later than $t_{RESETDELAY}$ after the end of the modulation of the block containing the protocol error.

PCD

10.3.5.5 If a time-out error occurs after receipt of a block not indicating chaining, then:

- Up to two R(NAK) blocks shall be sent to ask for retransmission.
- The PCD shall send the R(NAK) block after $t_{TIMEOUT}$ and before $t_{TIMEOUT} + \Delta T_{PCD} + t_{RETRANSMISSION}$.

If a time-out error occurs after the second R(NAK) block, or if the PCD has detected a time-out after having re-transmitted an S(WTX) response block two times (i.e. the PCD twice consecutively repeats the sequence of detecting a time-out error following an S(WTX) response block, sending R(NAK) block(s), receiving an S(WTX) request, and sending the S(WTX) response), then the PCD shall report a time-out error to the terminal and continue as specified in requirement 10.3.5.9 within $t_{TIMEOUT}$ and $t_{TIMEOUT} + t_{RESETDELAY}$.

If no frame waiting time extension is requested by the PICC, then $t_{TIMEOUT}$ is equal to $FWT + \Delta FWT$.

Otherwise, $t_{TIMEOUT}$ is equal to $(FWT \times WTXM) + \Delta FWT$.

10.3.5.6 If a block with a transmission error is received after receipt of a block indicating chaining, then the last R(ACK) block sent by the PCD shall be retransmitted.

The PCD shall send the R(ACK) block no later than $t_{RETRANSMISSION}$ after the end of the modulation of the block with the transmission error.

The PCD shall retransmit the R(ACK) block up to two consecutive times to ask for retransmission.

If a block with a transmission error in response to the second R(ACK) block is received, then the PCD shall report a transmission error to the terminal and continue as specified in 10.3.5.9 no later than $t_{RESETDELAY}$ after the end of the modulation of the last block with the transmission error.

Note that the transmission error is suppressed by the EMD handling defined in section 4.9.2 if the transmission error is detected when less than 4 bytes have been received from the PICC.

PCD

10.3.5.7 If a block with a protocol error is received after receipt of a block indicating chaining, then the PCD shall report a protocol error to the terminal and continue as specified in 10.3.5.9 no later than $t_{RESETDELAY}$ after the end of the modulation of the block containing the protocol error.

10.3.5.8 If a time-out error occurs after receipt of a block indicating chaining:

- The last R(ACK) block sent by the PCD shall be retransmitted up to two times to ask for retransmission.
- The PCD shall send the R(ACK) block after $t_{TIMEOUT}$ and before $t_{TIMEOUT} + \Delta T_{PCD} + t_{RETRANSMISSION}$.

If a time-out error occurs after the second R(ACK) block, then the PCD shall report a time-out error to the terminal and continue as specified in 10.3.5.9 within $t_{TIMEOUT}$ and $t_{TIMEOUT} + t_{RESETDELAY}$.

If no frame waiting time extension is requested by the PICC, then $t_{TIMEOUT}$ is equal to $FWT + \Delta FWT$.

Otherwise, $t_{TIMEOUT}$ is equal to $(FWT \times WTXM) + \Delta FWT$.

10.3.5.9 If no error recovery is possible, then the PCD shall reset the Operating Field (as defined in section 3.2.6).

At this stage it is up to the implementation to define how terminal and PCD continue processing. Options include (but are not limited to):

- *Wait with unmodulated carrier for a time t_{PAUSE} and resume with the polling procedure as specified in section 9.2.*
- *Continue with the removal procedure as specified in section 9.5. Note that in this case the reset of the Operating Field in requirement 9.5.1.1 should be skipped.*
- *Power-off of the Operating Field as specified in section 3.2.9.*

10.3.6 DESELECT Processing

The DESELECT command is coded as an S-block and consists of an S(DESELECT) request block sent by the PCD and an S(DESELECT) response sent as acknowledgement by the PICC. The coding of the S(DESELECT) block is as shown in Table 10.4. A PCD compliant with this specification does not use the S(DESELECT) request block. A PICC compliant with this specification is required to respond correctly to an S(DESELECT) request block.

Requirements 10.16: S(DESELECT) Response

PICC

- 10.3.6.1 The PICC shall acknowledge the S(DESELECT) request block by sending an S(DESELECT) response block. The S(DESELECT) response block shall be coded as an S - block as specified in Table 10.4.
 - 10.3.6.2 The PICC shall send an S(DESELECT) response block in response to an S(DESELECT) request block within **FWT_{DESELECT}** (refer to Annex A.6 for the value of **FWT_{DESELECT}**)
-

Annex A Values

Throughout the specification, symbols are used to identify the values of parameters. The actual values of the parameters are listed in this annex.

A.1 Operating Volume

Table A.1 lists the values of the parameters to define the Operating Volume.

Table A.1: Operating Volume

Topic	Parameter	Value	Units
Operating Volume	D_1	3	cm
	D_2	5	cm
	S_1	1	cm
	S_2	2	cm

A.2 RF Power and Signal Interface

Table A.2 lists the values of the parameters to define the RF power and signal interface requirements. For each of the parameters a minimum and maximum value is defined.

Table A.2: RF Power and Signal Interface

Topic	Parameter	EMV – TEST PICC	Value		Units
			Min	Max	
Power Transfer PCD→PICC	V_{ov} ($0 \leq z \leq 2$)	1	4.30 – 0.05 z	7.35	V
		2	4.60	6.95	V
		3	4.11 – 0.20 z	8.75	V
	V_{ov} ($2 < z \leq 4$)	1	4.56 – 0.18 z	7.35	V
		2	4.60	6.95	V
		3	4.19 – 0.24 z	8.75	V
	$\Delta V_{SENSE R}$	2	0	1	–
	f_c		13.553	13.567	MHz
Modulation PCD→PICC (Type A)	t_1		2.06	2.99	μs
	t_2		0.52	t_1	μs
	t_3		0	1.18	μs
	t_4		0	min(0.44, $t_3/1.5$)	μs
	t_5		0	0.50	μs
	$V_{OU,A}$	1 (LLZ)	0	$(1 - t_3/2.36) \times 0.1$	–
		2 (LLZ)	0	$(1 - t_3/2.36) \times 0.1$	–
		3 (LLZ)	0	$(1 - t_3/2.36) \times 0.1$	–
		1 (HLZ)	0	$t_3 < 0.44 \mu s: (1 - t_3/0.742) \times 0.2$ $t_3 \geq 0.44 \mu s: (1 - t_3/2.36) \times 0.1$	–
		2 (HLZ)	0	$t_3 < 0.44 \mu s: (1 - t_3/0.742) \times 0.2$ $t_3 \geq 0.44 \mu s: (1 - t_3/2.36) \times 0.1$	–
		3 (HLZ)	0	$t_3 < 0.44 \mu s: (1 - t_3/0.742) \times 0.2$ $t_3 \geq 0.44 \mu s: (1 - t_3/2.36) \times 0.1$	–

Topic	Parameter	EMV – TEST PICC	Value		Units
			Min	Max	
Modulation PCD→PICC (Type B)	mod_i		9.0	$15.0 - 0.25 z$	%
	t_f		0	1.18	μs
	t_r		0	1.18	μs
	$V_{ou,B}^{(1)}$	1 (LLZ)	0	$(1 - t_f/2.36) \times 0.1$	—
		2 (LLZ)	0	$(1 - t_f/2.36) \times 0.1$	—
		3 (LLZ)	0	$(1 - t_f/2.36) \times 0.1$	—
		1 (HLZ)	0	$t_f < 0.44 \mu\text{s}: (1 - t_f/0.742) \times 0.2$ $t_f \geq 0.44 \mu\text{s}: (1 - t_f/2.36) \times 0.1$	—
		2 (HLZ)	0	$t_f < 0.44 \mu\text{s}: (1 - t_f/0.742) \times 0.2$ $t_f \geq 0.44 \mu\text{s}: (1 - t_f/2.36) \times 0.1$	—
		3 (HLZ)	0	$t_f < 0.44 \mu\text{s}: (1 - t_f/0.742) \times 0.2$ $t_f \geq 0.44 \mu\text{s}: (1 - t_f/2.36) \times 0.1$	—
Load Modulation	V_{pp}		See Table A.3	80	mV

- ⁽¹⁾ The values for $V_{ou,B}$ included in Table A.2 are for the falling edge. For the rising edge, t_f has to be replaced with t_r .

Table A.3: Minimum Value of V_{pp}

$z \backslash r$	0	1.5	2.5
0	8.8	4.9	–
1	7.2	4.1	2.5
2	5.6	3.3	2.1
3	4.0	2.5	1.7
4	2.4	1.7	–

Minimum values of V_{pp} for (z,r) not included in the table are derived through linear interpolation. For example:

$$V_{pp} (z=2.5, r=1) :$$

$$V_{pp} (z=2.5, r=0) = 5.6 - (5.6 - 4.0) \times 0.5 = 4.8 \text{ mV}$$

$$V_{pp} (z=2.5, r=1.5) = 3.3 - (3.3 - 2.5) \times 0.5 = 2.9 \text{ mV}$$

$$V_{pp} (z=2.5, r=1) = 4.8 - (4.8 - 2.9) / 1.5 = 3.5 \text{ mV}$$

A.3 Set-up Values for Test Equipment

Table A.4 lists the set-up parameters for the EMV Contactless Level 1 Test Equipment. For each of the parameters a minimum and maximum value is defined. When applicable, also a nominal value is defined.

Table A.4: Set-up Values for EMV Contactless Level 1 Test Equipment

Topic	Parameter	EMV – TEST PICC	Min	Max	Unit
PCD Power	$V_{S,OV}$	1	5.11	5.95	V
	$V_{S,OV,RESET}$		0	5.3	mV
	$V_{S,OV,LM}$	1		5.74	V
Carrier Frequency	$f_{S,C}$	1	13.55	13.57	MHz
Modulation PCD→PICC (Type A)	$t_{S,1}$	1	2.03	3.02	μs
	$t_{S,2}$	1	0.44	$t_{S,1}$	μs
	$t_{S,3}$	1	0	1.25	μs
	$t_{S,4}$	1	0	min(0.52, $t_{S,3}/1.45$)	μs
Modulation PCD→PICC (Type B)	$m_{S1,i}$	1	7.5	19	%
	$m_{S2,i}$	1	7.5	18	%
	$m_{S3,i}$	1	8	17	%
	$t_{S,f}$	1	0	1.25	μs
	$t_{S,r}$	1	0	1.25	μs
Load Modulation	$V_{S1,pp}$	1	5.5	85.0	mV
		2	5.5	85.0	mV
		3	6.0	85.0	mV
	$V_{S2,pp}$	1	3.5	40.0	mV
		2	3.5	40.0	mV
		3	4.5	33.0	mV
	$V_{S2,pp,IQ}$	IQ		4.0	mV

A.4 Sequences and Frames

Table A.5 lists the values of the parameters to define the requirements regarding sequences and frames. For some of the parameters a minimum and maximum value is defined. Other parameters are defined by a single value.

Parameters listed in Table A.5 have a value for the PCD and for the PICC. Unless otherwise specified, the PCD value is used when the parameter is referenced in a PCD requirement. The PICC value is used when referenced in a PICC requirement.

Table A.5: Sequences and Frames

Topic	Parameter	PCD Value Min	PCD Value Max	PICC Value Min	PICC Value Max	Units
Type A	FWT_{ACTIVATION}	71680		65536		1/f _c
	FDT_{A,PCD,MIN}	6780		1172		1/f _c
Type B	t_{PCD,S,1}	1280	1416	1272	1424	1/f _c
	t_{PCD,S,2}	248	392	240	400	1/f _c
	t_{PCD,E}	1280	1416	1272	1424	1/f _c
	t_{PICC,S,1}	1264	1424	1272	1416	1/f _c
	t_{PICC,S,2}	240	400	248	392	1/f _c
	t_{PICC,E}	1264	1424	1272	1416	1/f _c
	TR0_{MIN}	1008		1024		1/f _c
	TR1_{MIN}	1264		1280		1/f _c
	TR1_{MAX}	3216		3200		1/f _c
	t_{FSOFF}	0	272	0	256	1/f _c
	EGT_{PCD}	0	752	0	768	1/f _c
	EGT_{PICC}	0	272	0	256	1/f _c
Common	FWT_{ATQB}	7680				1/f _c
	TR0_{MAX,ATQB}	6416		4096		1/f _c
	FDT_{B,PCD,MIN}	6780		1792		1/f _c
	FWT_{MAX}	4096 x 2 ^{FWIMAX}		4096 x 2 ^{FWIMAX}		1/f _c
	ΔFWT	49152				1/f _c
	ΔT_{PCD}	16.4				ms
	FSD_{MIN}	256		256		bytes
	FSC_{MIN}	16		32		bytes
	SFGI_{MAX}	14		8		-
	ΔSFGT	384 x 2 ^{SFGI}				1/f _c
	FWI_{MAX}	14		7		-
	FSDI_{MIN}	8		8		-
	FSCI_{MIN}	0		2		-
	t_{nn}			1408		1/f _c

A.5 PCD Processing

Table A.6 lists the values of the parameters to define the requirements regarding PCD processing. Some parameters listed in Table A.6 have a value for the PCD and for the PICC. Unless otherwise specified, the value for the PCD is used when the parameter is referenced in a PCD requirement. The value for the PICC is used when referenced in a PICC requirement.

Table A.6: PCD Processing

Parameter	PCD Value		PICC Value	Units
	Min	Max		
t_{RESET}	5.1	10	5	ms
t_P	5.1	10	5	ms
$t_{RETRANSMISSION}$		10		ms
$t_{MIN,RETRANSMISSION}$		3		ms
$t_{RESETDELAY}$		33		ms
$t_{RECOVERY}$		1280		1/f _c
$t_{POWEROFF}$		15		ms

A.6 Protocol Operation

Table A.7: Protocol Operation

Parameter	PICC Value	Units
$FWT_{DESELECT}$	512	etu

Annex B Position Conventions

This annex specifies the convention used to define the position of a PICC within the Operating Volume. The position of the PICC is represented by the quadruplet (r, φ, z, θ) , where r and φ represents the coordinates of the centre of the PICC horizontal to the landing plane. The values $(r, \varphi) = (0,0)$ locate the centre of the landing plane. All observations involving a PICC are performed with the PICC perpendicular to the Z-axis. The value of z represents the distance above the landing plane and θ represents the orientation of the PICC as shown in Figure B.1. The values r and z are always expressed in cm. Figure B.1 and Figure B.2 illustrate the convention used for indicating different positions in the Operating Volume.

Figure B.1: Position of r , φ , and Z Axis within Operating Volume

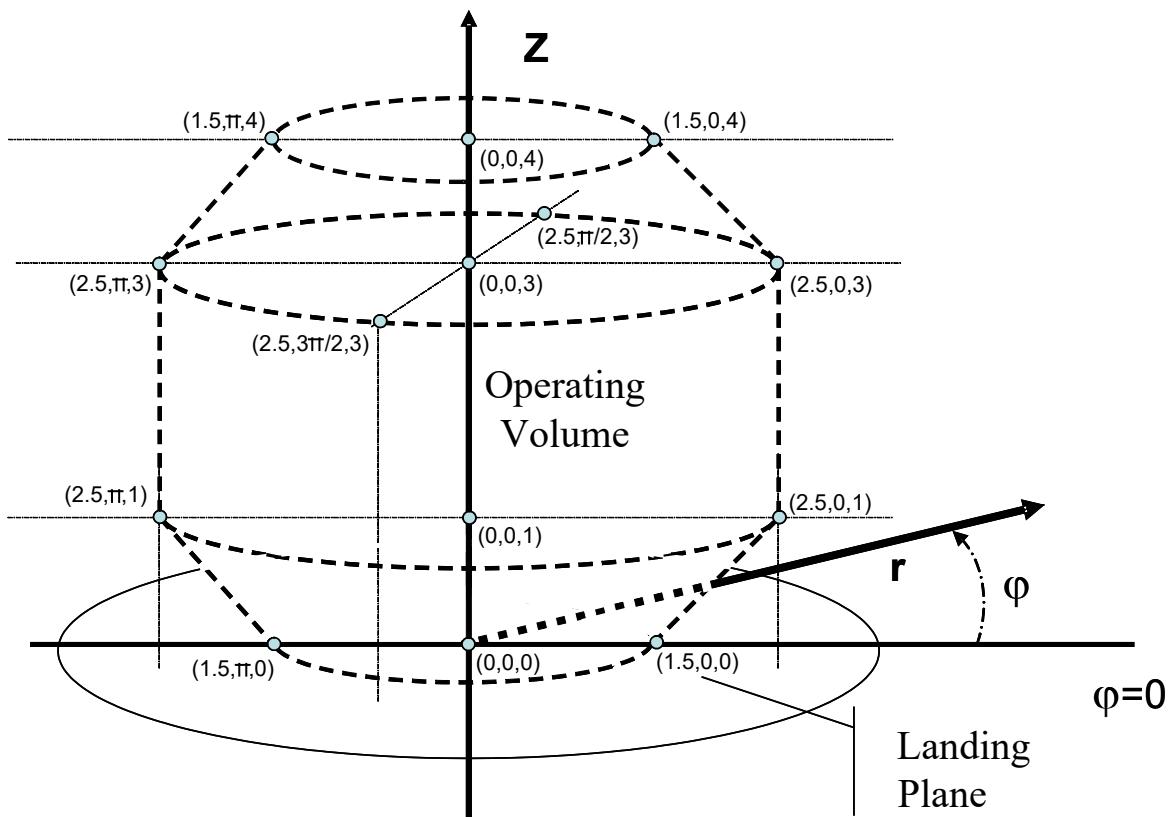
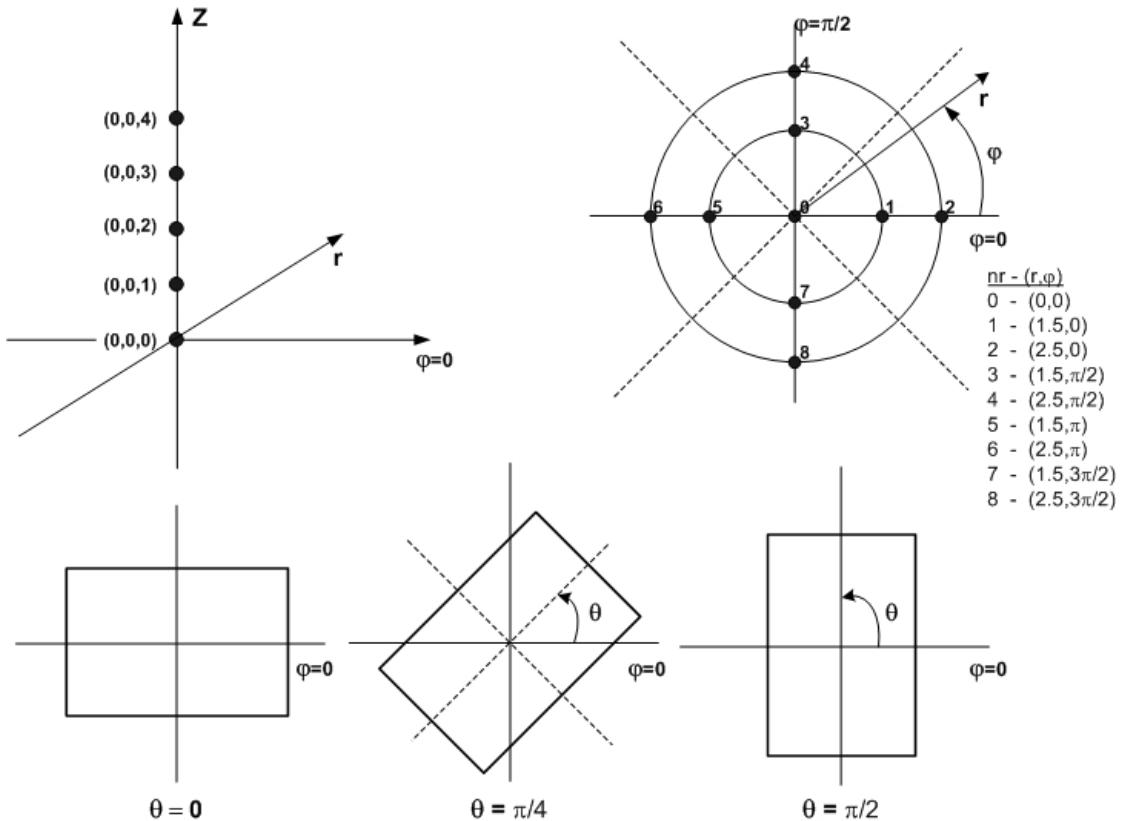


Figure B.2: Positions within the Operating Volume

***** END OF DOCUMENT *****