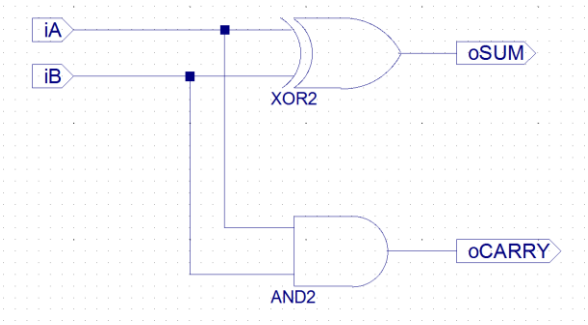
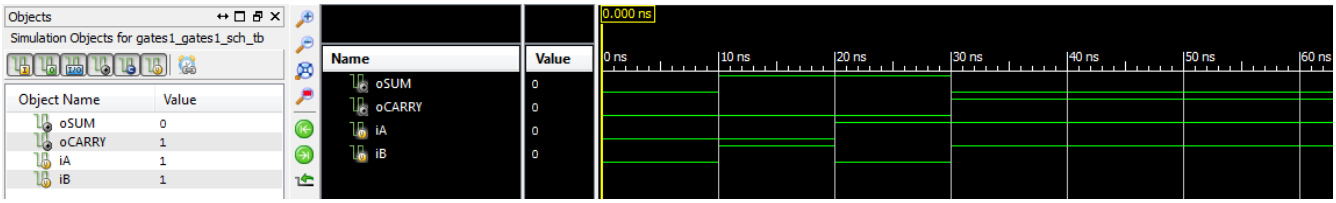
Design Assignment 1 – Introduction to Xilinx

1 PROCEDURE

1) Team sizes of 1 or 2 students, 1 report per student
2) Open the application Xilinx Design Tools → ISE Design Suite 14.2 → ISE Design Tools → 64-bit Project Navigator
3) Dismiss "Tip of the Day" if it comes up
4) Click New Project …
5) Set the location to an appropriate path (like your H: drive)
6) Name: eng312_proj1
7) Set the top level source for "Schematic"
8) Right click on eng312_proj1, and select "New Source …"→ Schematic. Give your schematic the name "gates_1".
    a. Enter the following schematic, and save it.



9) Right click on eng312_proj1, and select "New Source …"→ Verilog Test Fixture. Give your file the name "tb_eng312_proj1", which suggests that this will be the Testbench for your first project.
    a. Write Verilog testbench code to apply stimulus to gates_1, to produce the following scenario:



    b. You can use an initial .. begin .. end construct.
10) Click the radio button for "Simulation" under View: at the top of the project pane.
11) Right click on ISim Simulator → Behavioral Check Syntax → Run to check syntax.
12) Right click on Simulate Behavioral Model → Run to run your simulation
    a. If all goes well ISim will bring up a waveform window.

13) Add one more source file, to model the gates behaviorally – this will be Verilog, named "behav_1". Use Boolean expressions to compute oSUM and oCARRY. Modify your testbench to instantiate behav_1, rather than gates_1. Rerun the simulation, and compare waveforms.

2 REPORT

- 1 report per team, please submit via Canvas
- Include your code, schematic and waveforms
- All code should be properly formatted:
    - Tabs used as appropriate
    - Columns lined up
    - Comments
    - Whitespace for readability

3 RESOURCES

- Dr. Hernandez' Xilinx tutorial video at: http://www.tcnj.edu/~hernande/movies/xilinx1_media/xilinx1.wmv
- Xilinx ISE Tutorial document at: http://www.tcnj.edu/~hernande/Eng312/ise7tut.pdf