Design Assignment 3 – Traffic Light Controller

1 PROJECT OVERVIEW

The aim of this project is to design a digital controller to control traffic at an intersection of a busy main street (North-South) and an occasionally used side street (East-West).

The design relies on the theoretical concepts such as combinational logic design, sequential logic design, counters and state machines that are covered in the ENG 312 lectures.

2 DESIGN SPECIFICATIONS

The North-South (NS) street is to have a green light for a minimum of 25 Seconds or as long as there is no vehicle on the side street. The East-West (EW) street is to have a green light until there is no vehicle on the side street or for a maximum of 25 Seconds. There is to be 4-Second caution light (Yellow) between changes from green to red on both the main street and the side street. Note that the signal should not allow traffic on EW until there is a vehicle present on that street. For this design the lights do not have to be simultaneously red.

INPUTS:

NS_VEHICLE_DETECT, 1: a vehicle is present in NS lanes, 0: no vehicle is present

EW_VEHICLE_DETECT, 1: a vehicle is present in EW lanes, 0: no vehicle is present

OUTPUTS:

NS_RED

NS_YELLOW

NS_GREEN

EW_RED

EW_YELLOW

EW_GREEN

3 PROCEDURE

Team sizes of 1 or 2 students, 1 report per team.

1) Draw a bubble state-diagram for the traffic controller using appropriate variable definitions. How many states does the system go through? What controls the state transitions? Note that you will likely use a separate time counter, which is an additional state machine.
2) Assign binary values to the states.
3) Develop a truth table for the outputs, as a function of the states.
4) Draw a gate level representation of your design, showing flip-flops and gates
5) Create a new ISE Project, called eng312_proj3
    a. Implement your design in Verilog.
6) Create a testbench with test stimulus that models corner cases:
    a. No traffic on either NS or EW
    b. Steady traffic on both NS and EW
    c. Steady traffic on NS, not EW
    d. Steady traffic on EW, not NS
    e. Intermittent traffic on NS, none on EW
    f. Intermittent traffic on EW, none on NS
    g. Intermittent traffic on both NS and EW, e.g. 1 car every 20 or 30 seconds.
    h. NOTE: it is up to you to convince us that you have verified your design to properly handle all cases.
7) Report, include:
    a. All Verilog source code, nicely formatted and commented, in a monospaced (e.g. Courier New) font.
    b. All testbench code, similarly formatted and commented.
    c. Waveform snapshots, covering each test case and highlighting expected and observed behavior
8) Present your project in class.