Neha Sinha

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Education

National University of Singapore

M.S. IN ELECTRICAL AND COMPUTER ENGINEERING   *Jan 2022 - Present*

Vellore Institute of Technology   *9.22*

B.TECH. IN ELECTRICAL AND ELECTRONICS ENGINEERING   *July 2015 - Apr 2019*

Projects

Design of Systolic Array Architecture   *NUS*

MENTOR: PROF. MASSIMO ALIOTO AND PROF. XUANYAO FONG   *Jan 2022 - Apr 2022*

- Worked on the design and verification of a Systolic Array Architecture using RTL for neural network inference, a popular hardware accelerator architecture used in myriad of accelerators such as the Google TPU
- Also did the post synthesis analysis for area and timing analysis along with suggesting improvements in the design of the architecture for higher area efficiency

16-bit RISC Processor Design   *NUS*

MENTOR: PROF. MASSIMO ALIOTO AND PROF. XUANYAO FONG   *Jan 2022 - Apr 2022*

- Worked on the design and verification of a 16-bit pipelined processor based on the RISC ISA

MRAM Cell Design   *NUS*

MENTOR: PROF. HYUNSOO YANG   *Jan 2022 - Mar 2022*

- Designed an MRAM-based memory cell using OOMMF design software

Face Detection using Neural Networks   *VIT*

MENTOR: PROF. MONICA SUBHASHINI   *Jan 2017 - May 2017*

- Designed an MLP model in order to perform real time face detection

Detection of Breast Tumor using Image Processing   *VIT*

MENTOR: PROF. SUDHA PRABHAKARAN   *Aug 2018 - Dec 2018*

- Worked on the Breast Tumor Detection using K-means clustering post pre-processing of X-ray images

Professional Experience

Marvell Technology Limited   *Singapore*

PRODUCT ENGINEERING INTERN   *May 2022 - July 2022*

- Worked on the testing flow and analysis of memory controllers and ASIC chips

ALSTOM   *Bangalore, India*

TRAINLAB ENGINEER   *Jul 2019 - Dec 2021*

- Analyzed train schematics and obtained inputs from suppliers to develop logical working models of different subsystems like Doors, Brakes, Traction, ATC, etc which will emulate their overall functioning
- Developed user cases to test and verify the working of modelized subsystems with respect to original hardware present in the train
- Collaborated with Design, Control, and Testing teams to test, verify and provide inputs for the software used in train for different system
- Integrated all models representing various subsystems of the train together in order to finally attain the functionality of the train
- Developed, tested, and commissioned test benches (hardware, software, and communication between train devices) for activities related to testing and validation of train software
- Worked on planning, development, and Integration of virtual driver desk for the metros to be used for driving and controlling the operation of the train in numerous scenarios
- Worked for various metros/high-speed train projects like Mumbai Metro, TGV, Barcelona Metro, Shanghai Line 15, Perth Metro at Alstom Bengaluru R&D Centre (Laboratory)

Indian Institute of Science   *Bangalore, India*
Research Intern   *May 2018 - Aug 2018*
- Worked on the software and hardware implementation of the identification of Fault location in a DC Ring bus Microgrid.

Publications

- *Breast Cancer Detection Using Image Processing Techniques*, Siddhartha Gupta, Neha Sinha, R Sudha, Challa Babu 2020, IEEE, page number 1-6

- *A Review on Present Trends of Renewable Energy Resources in India*, Siddhartha Gupta, Neha Sinha and Balaji S 2018, International Journal of Recent Advances in Multidisciplinary Research, page number 1-6

Relevant Courses

M.S. Courses: Integrated Digital Design (EE4415), Magnetic Data Storage for Big Data (EE5440), Microelectronic Process Integration (EE5434), Semiconductor Fundamentals (EE5508)
B.E. Courses: Neural Networks and Fuzzy Control , Microprocessors and Microcontrollers, Digital Signal Processing, Analog and Digital Circuits, VLSI Design

Technical Strengths

Programming Languages: Verilog, Matlab, Python, TCL, C++
Tools & Simulators: Synopsys Design Compiler, Labview, Vivado, OOMMF

Honors & Awards

Spot Award: Received Spot Awards for consistently performing well in all the projects taken up	*ALSTOM Bangalore*
Summer Research Fellowship: Scholarship awarded by the Indian Academy of Science under the Summer Research Fellowship Program	*IAS*
Merit Award and Scholarship: Received Merit Award and scholarship for academic excellence during undergraduate studies	*VIT*

Responsibilities

2016 - 18	**Assistant General Secretary, ISOI (Instrument Society of India)**: Enhancing the knowledge, helping out and creating awareness among undergraduate students by working on different projects and organizing sessions on Internet-of-Things, working of different micro-controllers and sensors	*VIT*
2016 - 18	**Student Tutor**: Worked as a student tutor in an initiative called "Each One Teach One" by Juvenile Care (A society for teaching orphaned children)	*VIT*
2019 - 21	**Editor, Alstom Book Club**: Organized weekly discussions on various genres of books by inviting the authors to cultivate a reading habit among the employees at ALSTOM, Bangalore	*ALSTOM*