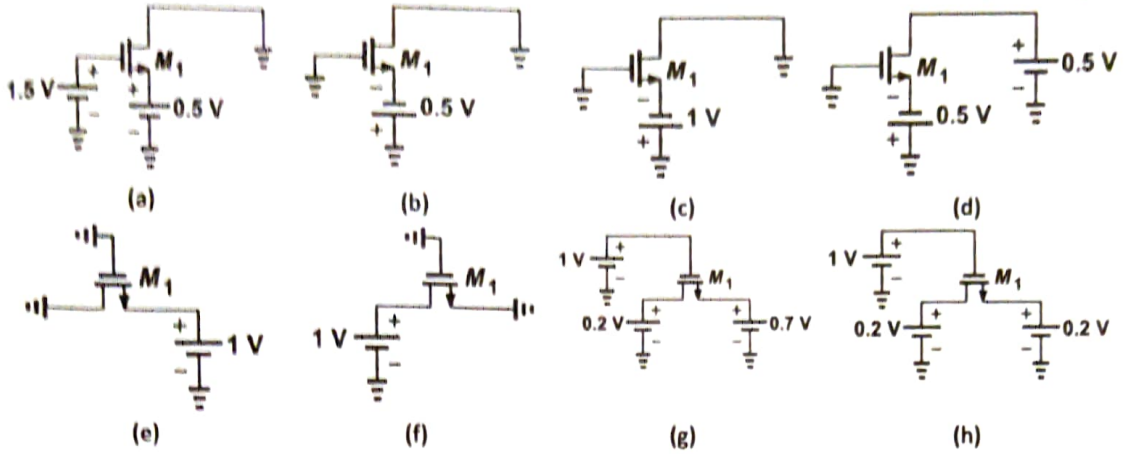
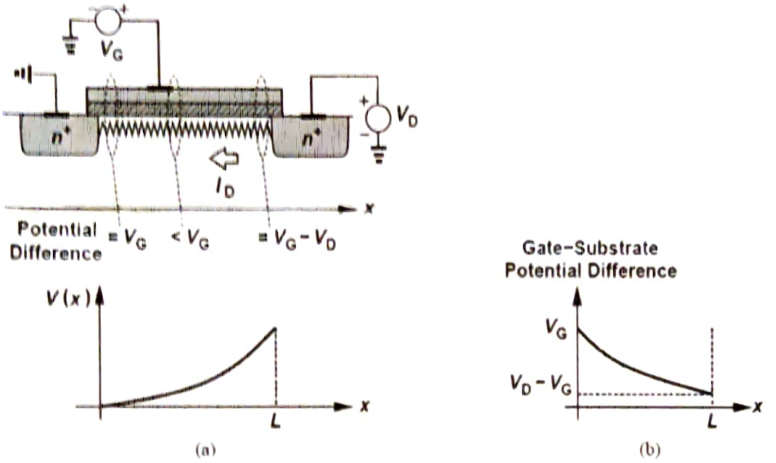
# Quiz-2: Analog Electronic Circuits (S25.EC2.103)

**NOTE: No query allowed during the exam. Write your assumptions (if any) for each question.**

**Q1.** Determine the region of operation of MOSFET (M1) in each of the circuits shown in Fig. below. [(a)-(h)]. Consider $V_{TH}$=0.4V **[8 Marks]**




**Q2.** Referring to Fig. Q2 below and assume $V_D$ >0, **[5 Marks]**




(a) Channel potential variation. (b) gate-substrate voltage difference along the channel. **Fig. Q2**

(a) Sketch the electron density in the channel as a function of x.

(b) Sketch the local resistance of the channel (per unit length) as function of x.

**Q3 (a).** What is the effect of temperature on MOSFET. Discuss through the basic MOS equation, e.g. how your $I_D$ get effected with rise in temperature when the MOSFET is in Saturation? **[2 Marks]**

**(b).** Pick the right option [(I)-(IV)] **[4 Marks]**

**(I).** The capacitances in MOSFET occurs due to _____

i. Interconnects
ii. Difference in Doping concentration
iii. Difference in dopant materials
iv. All of the mentioned

**(II).** The parasitic capacitances found in MOSFET are _____

i. Oxide related capacitances
ii. Inter electrode capacitance

iii. Electrolytic capacitance

iv. All of the mentioned

**(III).** In Cut-off region (assume MOS is in accumulation), the capacitance Cgs will be equal to

i. $2C_{GD0}$

ii. $C_{GS0}.W$

iii. $C_{GB}$

iv. All of the mentioned

**(IV).** In saturation mode operation, gate to drain capacitance (channel) is considered zero due to_____

i. Gate and drain are interconnected

ii. Channel length is reduced

iii. Inversion layer doesn't exist

iv. Drain is connected to ground

**Q4.** In the Fig.Q4, what is the minimum allowable value of $V_{DD}$ if M1 must not enter the triode region?

Assume $\lambda=0$, $V_{TH}= 0.4V$, $\mu_n C_{ox}= 200\ \mu A/V^2$

**[5 Marks]**

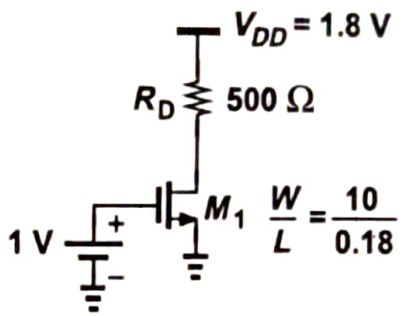



Fig. Q4

**Q5.** Sketch $I_x$ as a function of $V_x$ for the circuits shown in Fig. Q5. Assume $V_x$ goes from 0 to VDD=1.8V. Determine at what value of Vx the device changes its region of operation. Consider $\lambda=0$, $V_{TH}= 0.4V$.
**[6 Marks]**

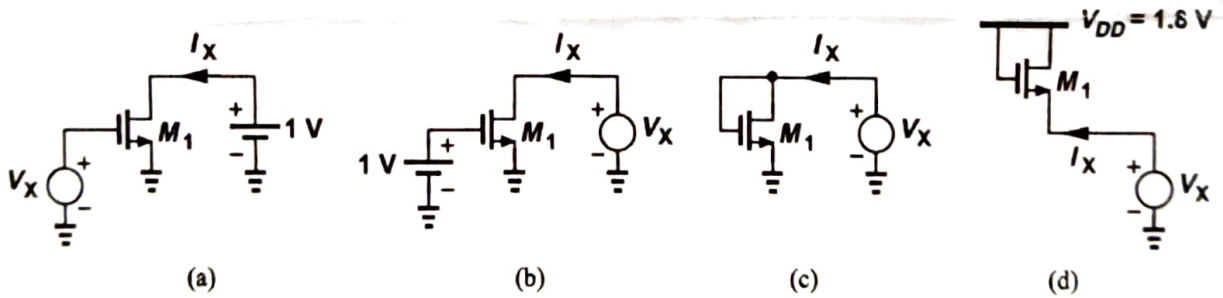



Fig. Q5