

## Mid-Sem: Analog Electronic Circuits (S25.EC2.103)

**NOTE: No query allowed during the exam. Write your assumptions (if any) for each question.**

**Q1 (a).** What is Base-width modulation? Discuss how it impacts the collector current in BJT? [2 Marks]

**(b).** Discuss the internal capacitances in BJT. What we call them? Who put them there? Can we eliminate them fully? Do these capacitance impacts the amplifier performances? If yes, how? Which capacitance you think is larger? [5 Marks]

**(c).** Draw a high-frequency hybrid-pi model. [2 Marks]

**(d).** What do you understand by Unity-gain frequency in an amplifier? [1 Mark]

**Q2.** What issues do you find in the biasing of Fig.1 below? Discuss the solutions. [5 Marks]

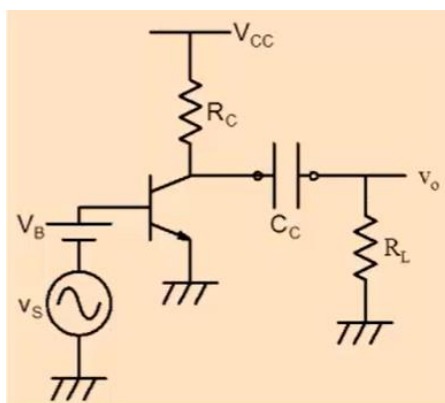


Fig. 1

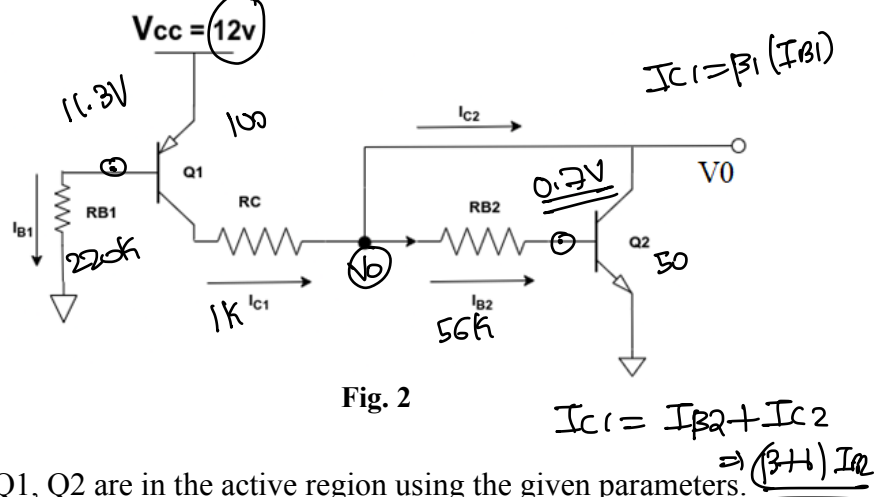


Fig. 2

**Q3.** Find  $V_O$  (in Fig. 2) assuming  $Q_1, Q_2$  are in the active region using the given parameters. [10 Marks]

$R_C = 1k\Omega, R_{B1} = 220k\Omega, R_{B2} = 56k\Omega, \beta_1 = 100, \beta_2 = 50$  and  $|V_{BE}| = 0.7V$

**Q4.** Discrete transistors  $T_1$  and  $T_2$  having maximum collector current rating of 0.75 Amps are connected in parallel as shown in Fig. 3. This combination is treated as a single transistor to carry a total current of 1 Amp, when biased with self-bias circuit. When the circuit is switched on,  $T_1$  draws 0.55 Amps and  $T_2$  draws 0.45 Amps. If the supply is kept on continuously, ultimately it is very likely that

- (a) Both  $T_1$  and  $T_2$  get damaged
- (b) Both  $T_1$  and  $T_2$  will be safe
- (c)  $T_1$  will get damaged and  $T_2$  will be safe
- (d)  $T_2$  will get damaged and  $T_1$  will be safe

**Justify your answer properly. [5 Marks]**

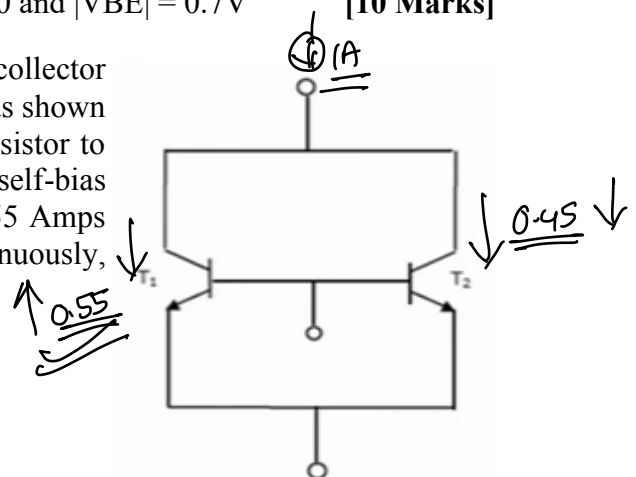
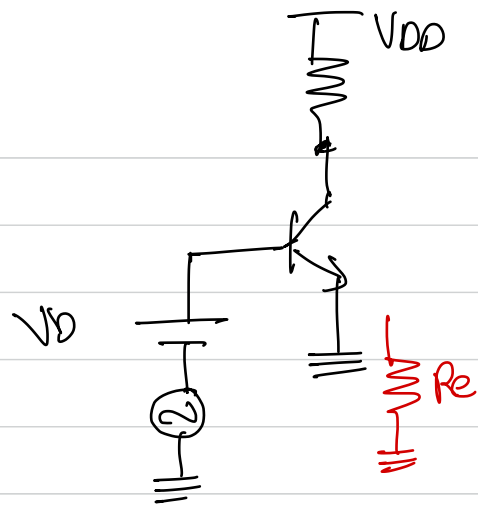


Fig. 3

②



$$\underline{V_b = 0.7V}$$

difficult to achieve

solution: place  $R_e$  b/w emitter node and gnd

③

**Q5 (a).** For the circuit shown in Fig. 4, assume that the  $\beta$  of the transistor is very large and  $V_{BE}$  is 0.7V. Estimate the mode of the operation of the BJT through proper calculations. [8+2 = 10 Marks]

Hint:  $I_B$  may be considered zero if  $\beta$  is very large.

**(b).** Consider the following statements **S1** and **S2**.

**S1:** the  $\beta$  of a transistor reduces if the base width is increased.

**S2:** the  $\beta$  of a transistor increases if the doping concentration in the base is increased.

Which one of the following is correct?

(a). S1 is FALSE AND S2 is TRUE (b). Both S1 and S2 are TRUE (c). Both S1 and S2 are FALSE (d). S1 is TRUE AND S2 is FALSE

**Attempt Q6 or Q7. [10 Marks]**

**Q6.** Consider the topology in Fig. 5 containing both pnp and npn transistors.

- Find the value of output ( $V_{out}$ ) when input ( $V_{in}$ ) is 0 and input ( $V_{in}$ ) is  $V_{CC}$ .
- For what input range would the output be close to 0?
- For what input range would the output be close to  $V_{CC}$ ?
- Draw the small signal model for the given topology (mention intrinsic output impedance  $r_o$  and input impedance  $r_\pi$  for both npn and pnp as well in the small-signal model)

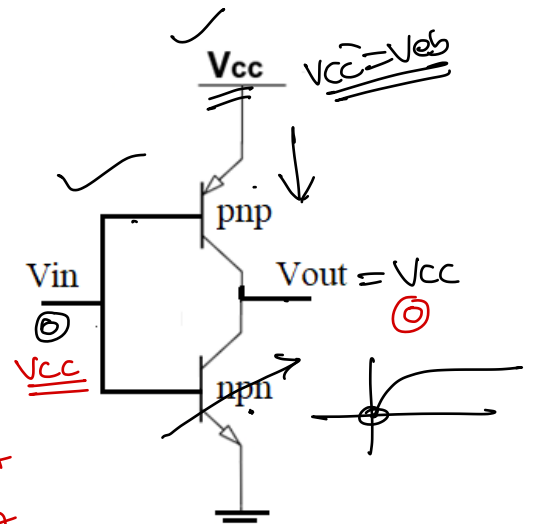


Fig. 5

**Q7.** For the BJT (Q1) in the circuit shown in Fig. 6,  $\beta = \infty$ ,  $V_{BEon} = 0.7V$ ,  $V_{CEsat} = 0.7V$ . The switch is initially closed. At time  $t=0$ , the switch is opened. Estimate the time  $t$  at which Q1 leaves the active region?

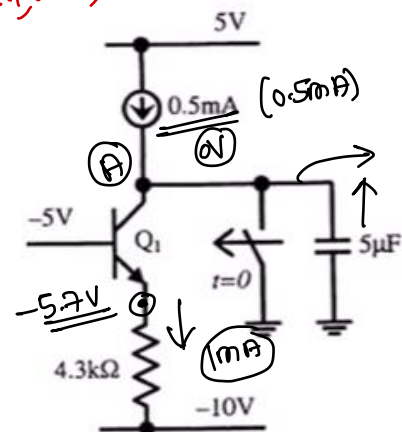


Fig. 6

$$V_A = -5V(A \rightarrow S)$$

$$-0.5mA = \frac{(5\mu)(-5)}{dt}$$

$$dt = \frac{25\mu}{0.5mA}$$

$$50ms$$

$$I_E = \frac{4.3V}{4.3k}$$

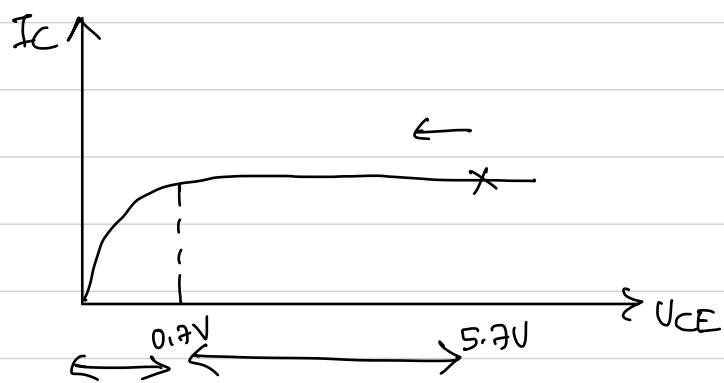
$$I_E = 1mA$$

Attach the question paper with your exam sheet"

[27/02/2025]

$$i = C \frac{dV}{dt}$$

$$-0.5mA = (5\mu F) \frac{dV}{dt}$$



$$V_{CE}(t=0) = \underline{\underline{5.7V}}$$