Pipelined

To simulate pipelining by adding pipeline register between each stage named IF/ID, ID/EX, EX/MEM, MEM/WB register. Below are the steps:

a. Define IFID_Reg, IDEX_Reg, EXMEM_Reg,MEMWB_Reg module for pipeline register.
b. Combine register pipeline register module with the modules define in previous lab to simulate piplelining.

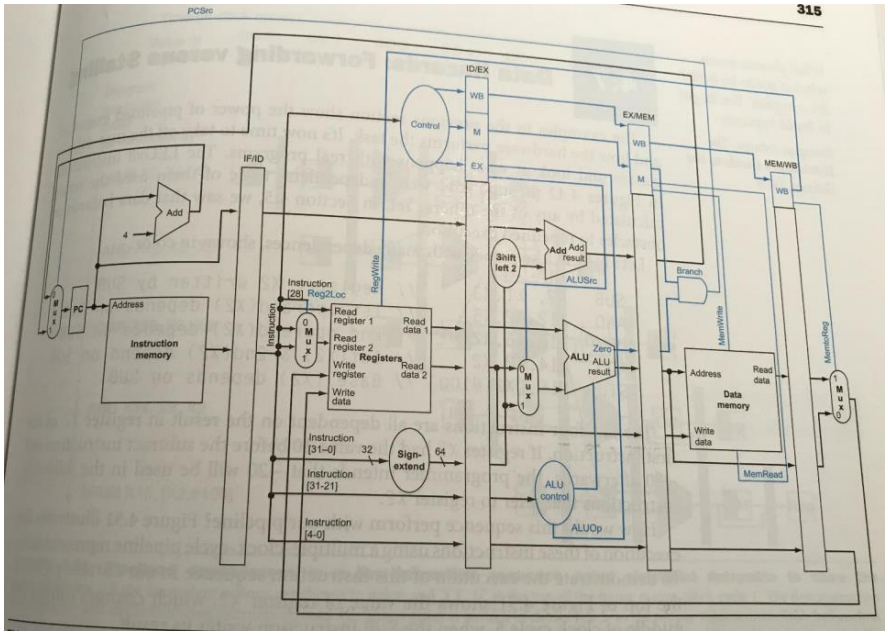


Figure shows the pipelining register used in pipelining.

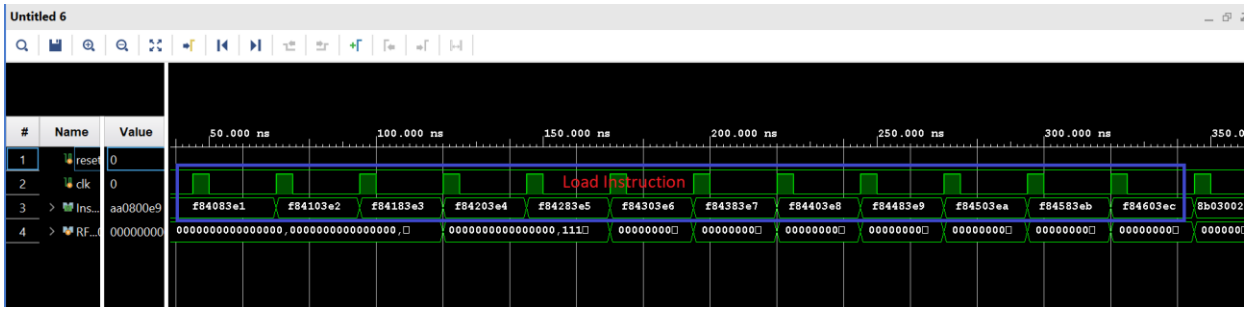
Operation parameters:

- Input clk 1 bit
- Input reset 1 bit

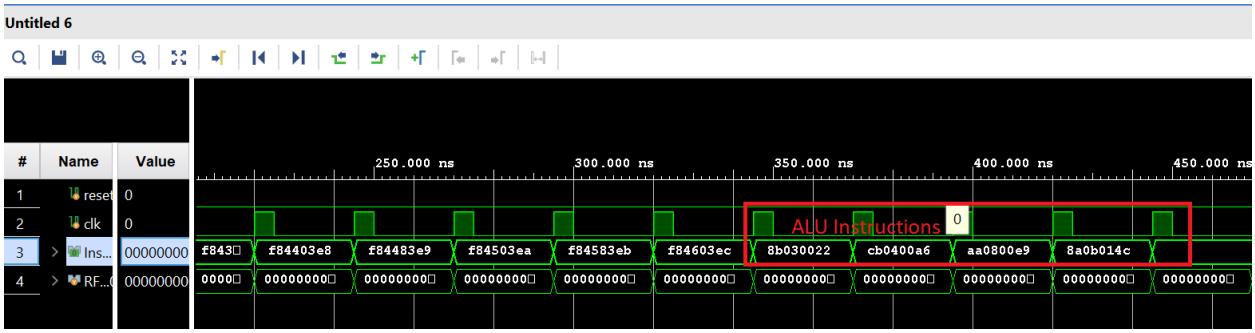
Module Name: PCIMIDwithRFALUDM

Test Module Name: PCIMIDwithRFALUDM_tb

Below screen shot show the waveform for pipeline:

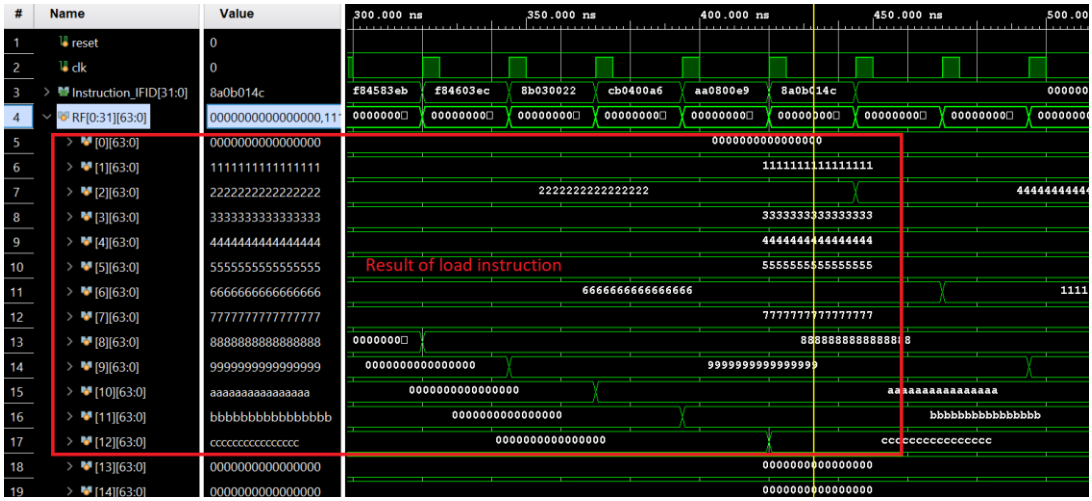


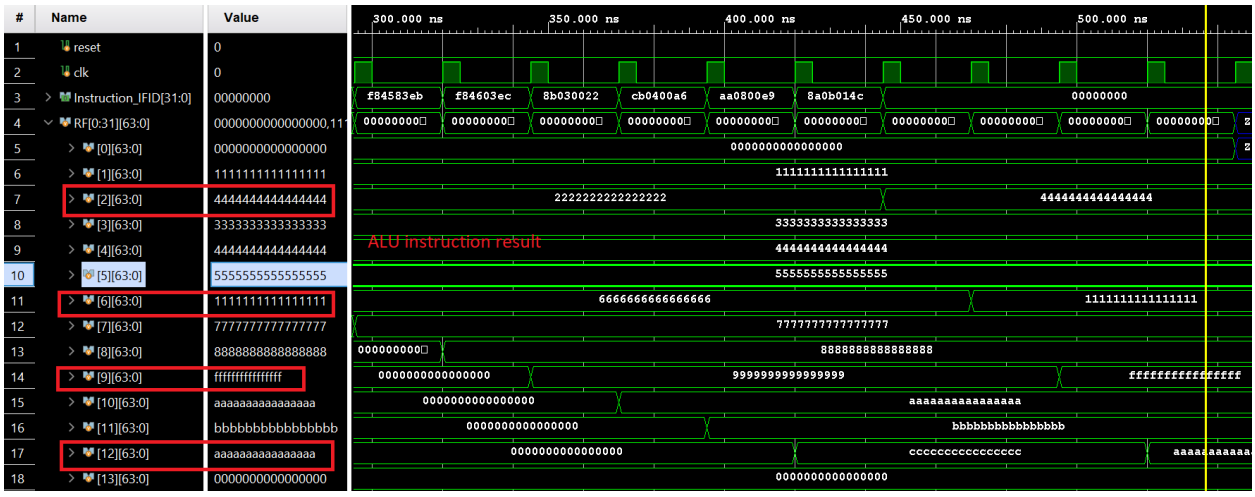
Here we are loading register 1 -12 from data memory DM[0]-DM[96] using load instruction. These are total 12 load instructions.



Here there are total four ALU instruction to perform below ALU instructions:

```
ADD X2, X1, X3          -- X2 = 64'h 4444 4444 4444 4444
SUB X6, X5, X4          -- X6 = 64'h 1111 1111 1111 1111
OR X9, X7, X8           -- X9 = 64'h ffff ffff ffff ffff
AND X12, X10, X11       -- X12 = 64'h aaaa aaaa aaaa aaaa
```





Here it takes total 20 cycle to produce result of 16 instructions using 5 stage pipeline with pipelining registers.