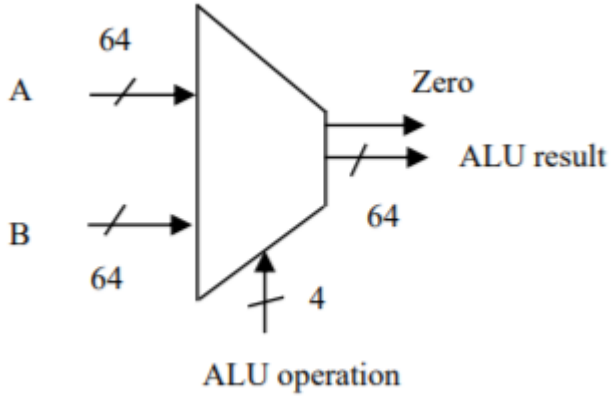
Simulation of ALU

The ALU has two data inputs A and B, and aa control input 'ALU_operation': data inputs are 64 bits wide, and the control is 4 bit wide. It will output the result as 'ALU_result' (also 64 bits wide) and a 1 bit output 'Zero' if the result of the operation is zero.Below are the steps involved in this lab assignment:

1. Design ALU using data inputs A and B which are 64 bit wide, control input which is 4 bit wide. It will generate result of ALU operation in ALU_result which is 64 bit wide and a Zero Flag.
2. Design combinational logic that generates ALU_operation input signal for ALU unit's control signal.
3. Combine above two design to simulate Arithmetic Logic Unit.

- Simulation of the ALU



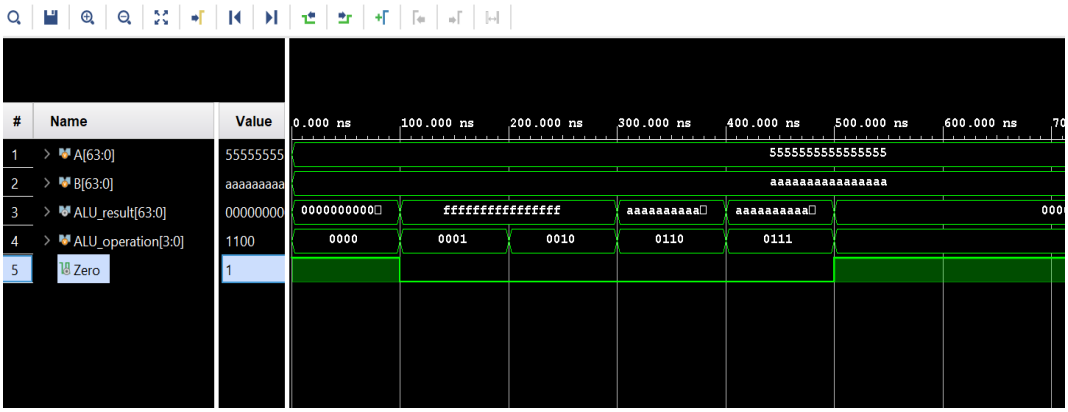
ALU Operation parameters are as below:

- Input A and B 64 bit
- Input ALU operation 4 bit
- Output ALU result 64 bit
- Output Zero flag

Module Name: LEGv8ALU

Test Module Name: LEGv8ALU_tb

Below screen shot show the waveform for input and output parameters of ALU



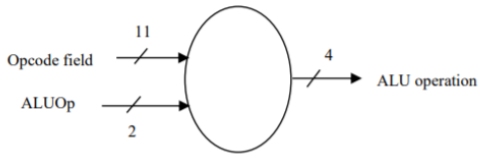
Here A input is set to 64'h5555555555555555 and B input is set to 64'haaaaaaaaaaaaaaaa.
Refer below table for result of all operation.

ALU Operation	Function	ALU Result	Result	Zero Flag
0000	AND	A & B	0	1
0001	OR	A | B	ffffffffffffffff	0
0010	ADD	A + B	ffffffffffffffff	0
0110	SUBTRACT	A – B	aaaaaaaaaaaaaaab	0
0111	PASS B	B	aaaaaaaaaaaaaaaa	0
1100	NOR	~(A | B)	0	1

Zero flag is set to 1 if the result of the operation is zero otherwise is reset.

If you see the subtraction operation the result's LSB is b, this is because LSB of A is 5 and LSB of B is a. 5 is less than a hence in hex value calculation we take borrow from next bit which becomes 5+ 16 = 21. Now if we do subtraction the result will be b, 21-a = b.

- Simulation of the ALU Control Logic



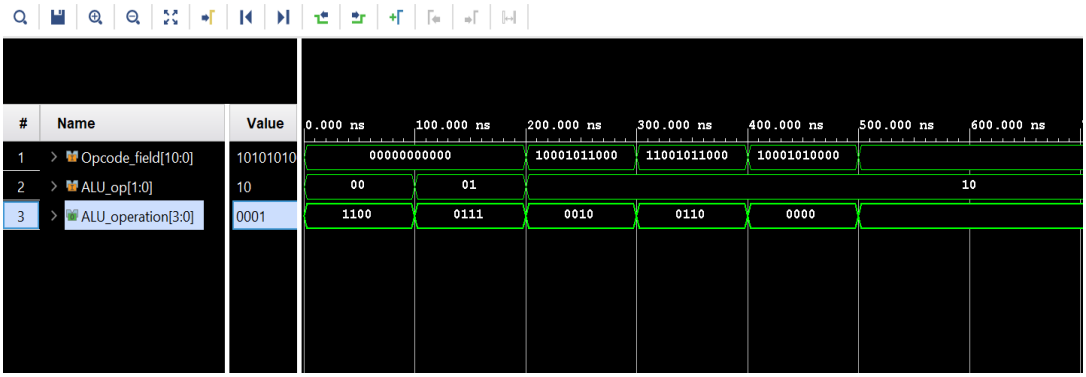
ALU Control Logic parameters are as below:

- Input opcode field 11 bit
- Input ALUOp 2 bit
- Output ALU operation 4 bit

Module Name: LEGv8ALU_control

Test Module Name: LEGv8ALU_control_tb

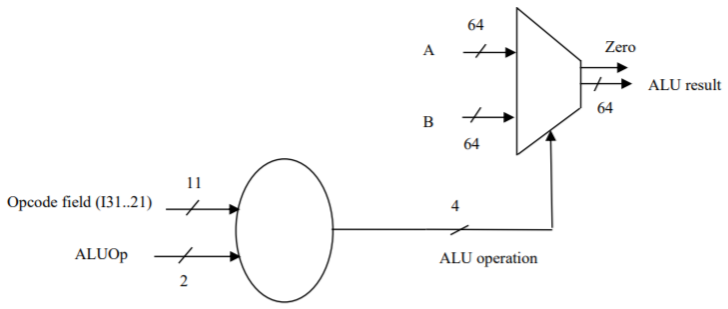
Below screen shot show the waveform for input and output parameters of ALU control Logic



Refer below table for ALU control logic result:

ALUOp		Opecode Field											ALU_opertaration
ALUOp1	ALUOP2	I[31]	I[30]	I[29]	I[28]	I[27]	I[26]	I[25]	I[24]	I[23]	I[22]	I[21]	
0	0	X	X	X	X	X	X	X	X	X	X	X	1100
X	1	X	X	X	X	X	X	X	X	X	X	X	0111
1	X	1	0	0	0	1	0	1	1	0	0	0	0010
1	X	1	1	0	0	1	0	1	1	0	0	0	0110
1	X	1	0	0	0	1	0	1	0	0	0	0	0000
1	X	1	0	1	0	1	0	1	0	0	0	0	0001

- Simulation of the ALU with its Control Logic



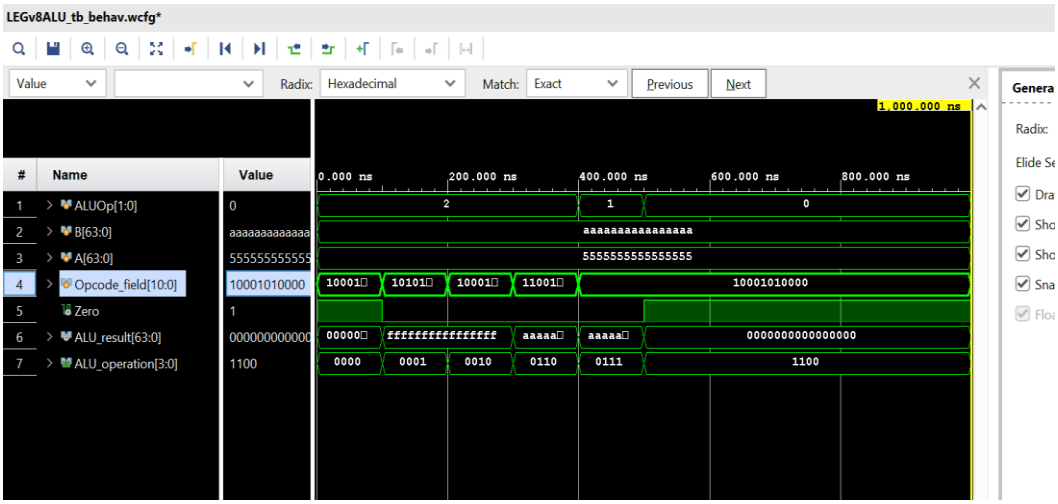
ALU with its Control Logic are as below:

- Input Opecode fiels 11 bit
- Input ALUOp 2 bit
- Input A 64 bit
- Input B 64 bit
- Output ALU result 64 bit
- Output Zero flag

Module Name: LEGv8ALUwithControl

Test Module Name: LEGv8ALUwithControl_tb

Below screen shot show the waveform for input and output parameters of ALU with its Control Logic



We set our A input to 64'h5555555555555555 and B input to 64'haaaaaaaaaaaaaaaa.

Refer below table for ALU with its Control Logic:

Opecode Field	ALUOP	Function	ALU Result	Result	Zero
1X	10001010000	AND	A & B	0	1
1X	10101010000	OR	A | B	ffffffffffffffff	0
1X	10001011000	ADD	A + B	ffffffffffffffff	0
1X	11001011000	SUBTRACTION	A – B	aaaaaaaaaaaaaaab	0
X1	XXXXXXXXXXX	PASS B	B	aaaaaaaaaaaaaaaa	0
00	XXXXXXXXXXX	NOR	~ (A | B)	0	1