PCIMID with RFALUDMRF

To simulate data path for R and D type instruction. Integration of Program Counter (PC), Instruction Memory (IM), Instruction Decoder (ID), Register File (RF), Arithmetic Logical Unit (ALU), Data Memory (DM) module developed in previous project. Below are the steps involved:

a. Define and Integrate Program counter with adder unit, Instruction memory unit, register file unit, MUX unit [Instruction memory to register file MUX unit, register file to ALU MUX unit, Data memory to Register file MUX unit], sign Extend Unit, ALU Control unit, ALU Unit, data memory Unit, instruction decoder unit.

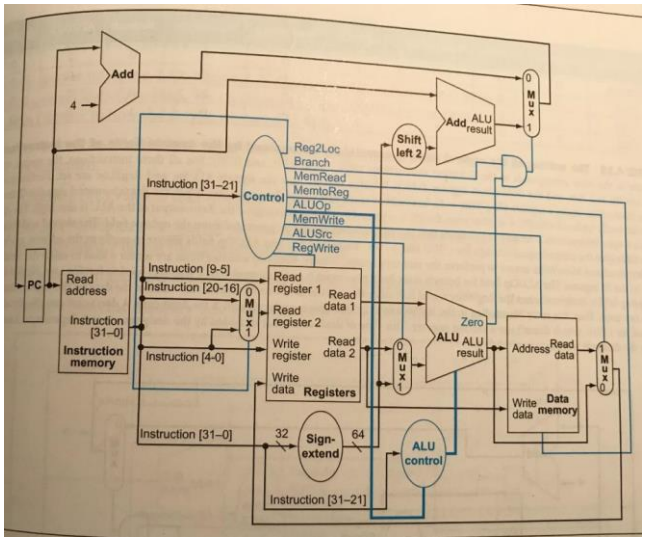


Figure shows the data path for R and D type instruction. We will not consider Brach instructions for this lab assignment.

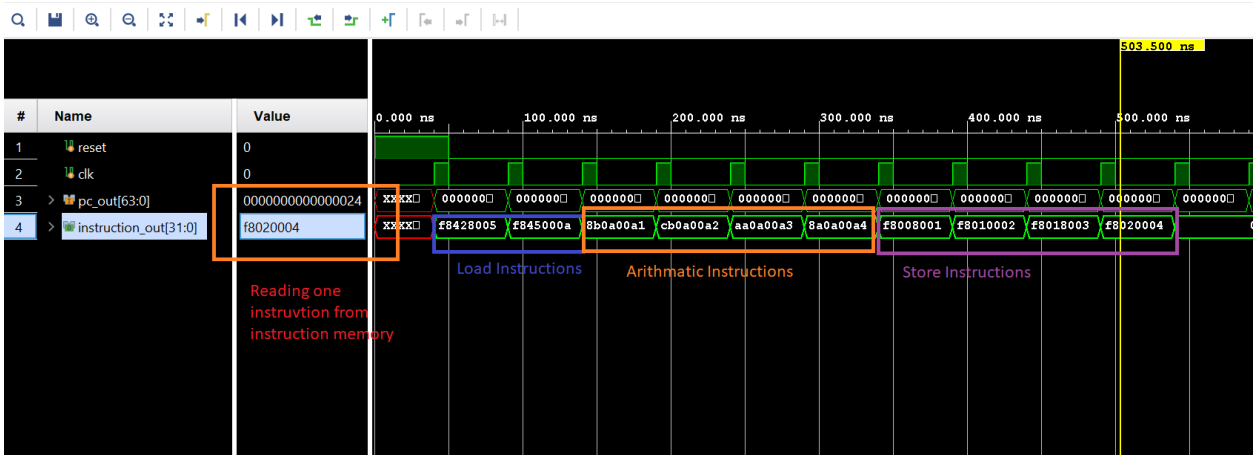
Operation parameters:

- Input clk 1 bit
- Input reset 1 bit

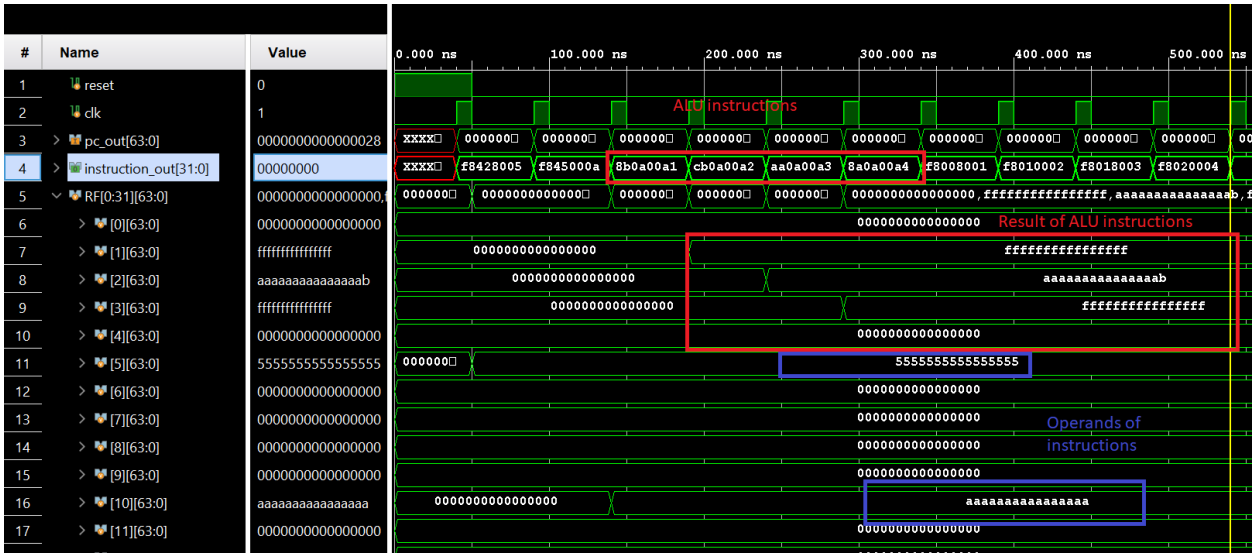
Module Name: PCIMIDwithRFALUDM

Test Module Name: PCIMIDwithRFALUDM_tb

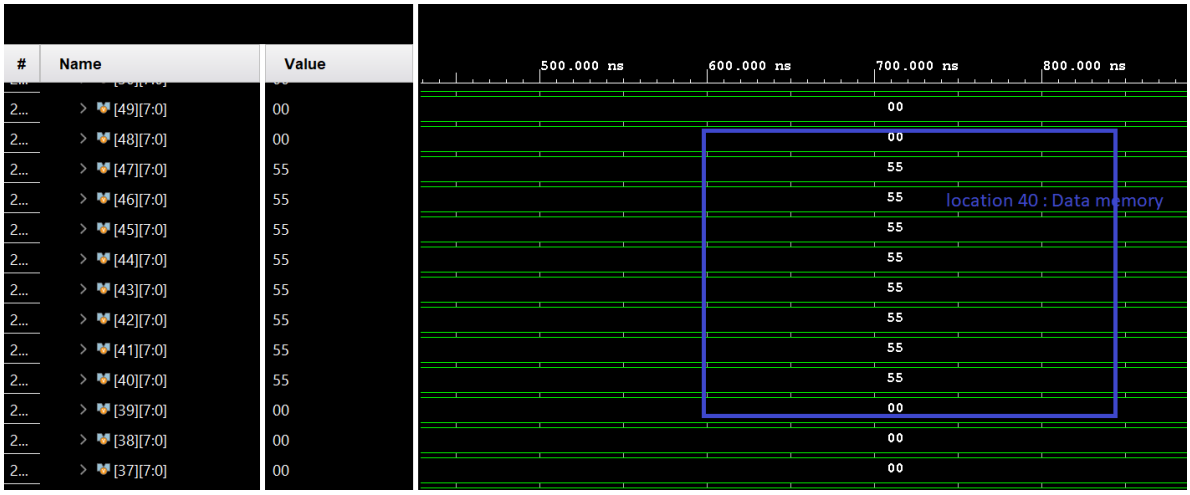
Below screen shot show the waveform for parameters of datapath:

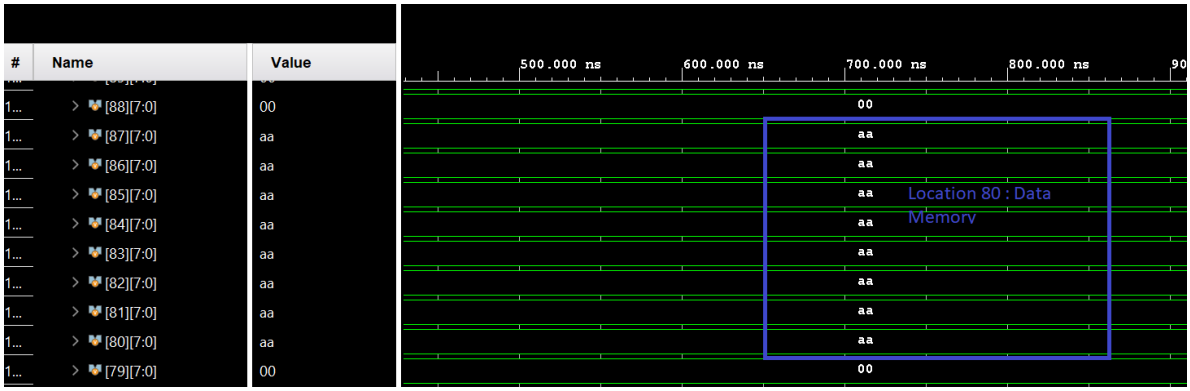


Here we are storing 10 instruction into the instruction memory and using program counter unit we are reading one instruction in each cycle. These are load, store and Arithmetic instructions. We are currently supporting D and R type instructions.

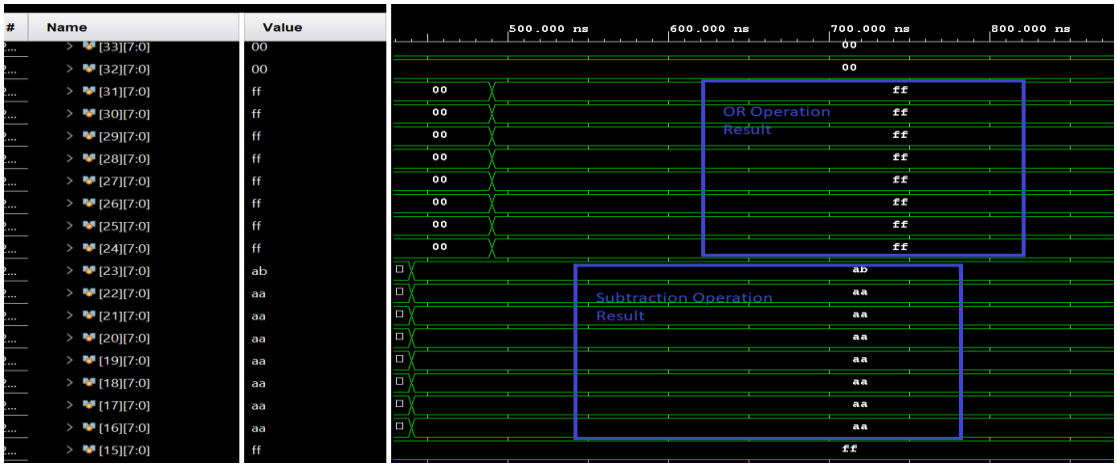


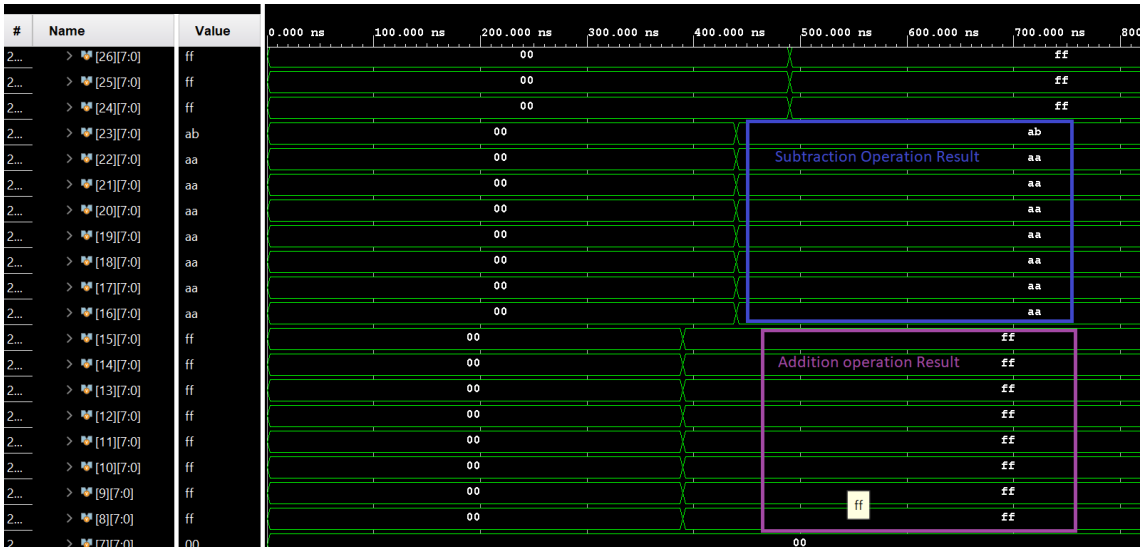
Here the Operands of Arithmetic instruction are read from registers and results are stored back to registers. Operands are in register 5, 10 while the arithmetic results are in register 1,2,3,4 where the results are of ADD, AND, OR, SUB operations respectively. This will support R type instruction.

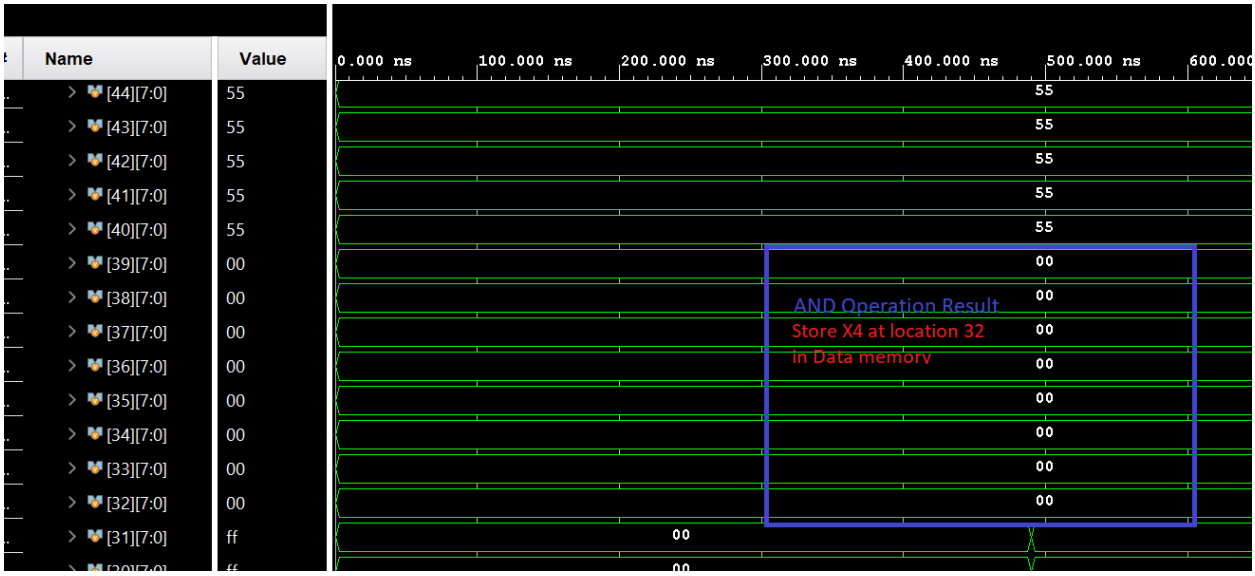




Here we can see location 40 and 80 in Data memory. These values are loaded to register 5 and 10 in register file to perform arithmetic operations. This will support load Instructions.







Here we are storing register 1,2,3,4 back to data memory at location 8,16,24,32 respectively. This will support store instruction.