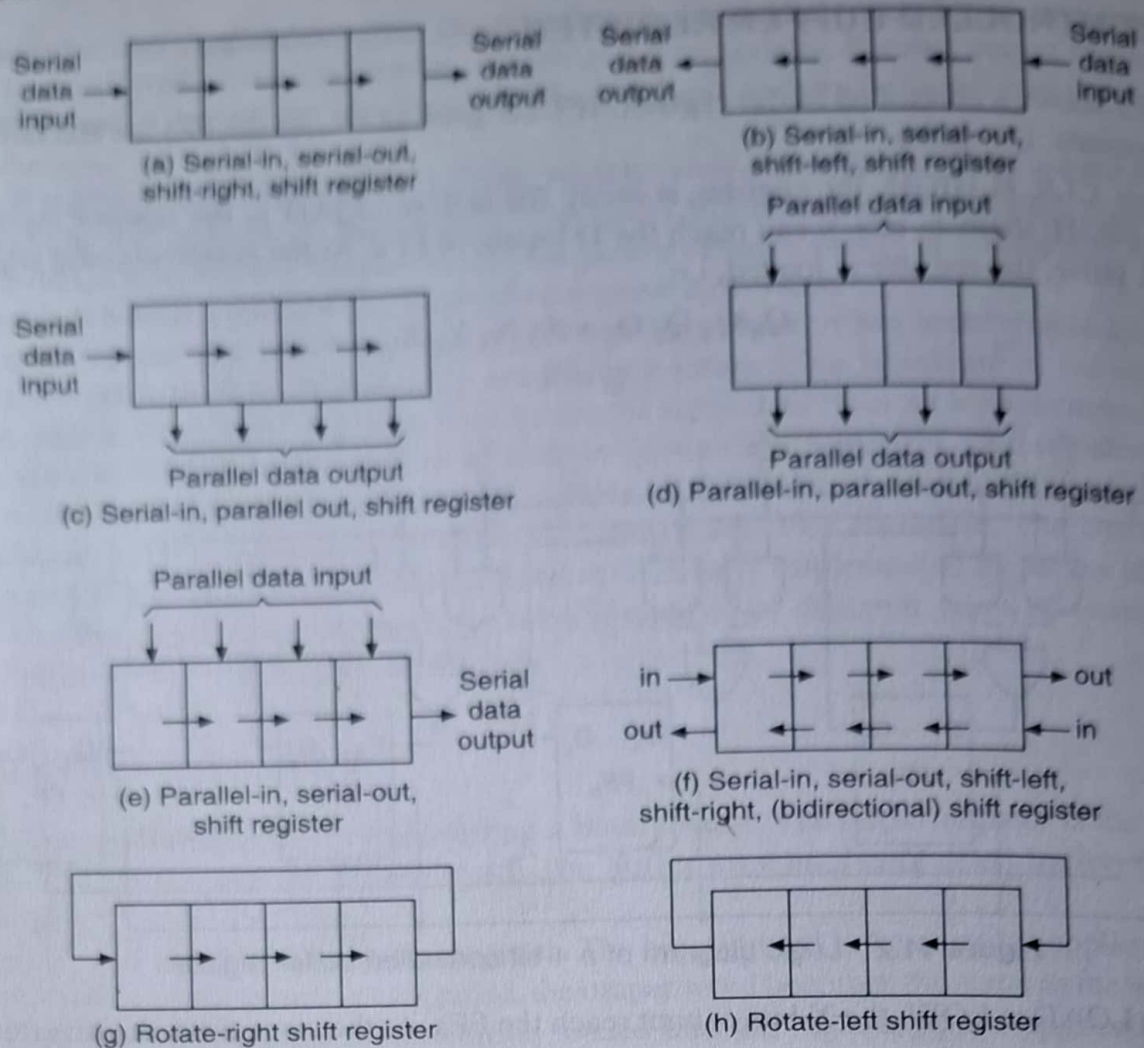


Figure 11.3 Data transfer in registers.

11.5 SERIAL-IN, SERIAL-OUT, SHIFT REGISTER

This type of shift register accepts data serially, i.e. one bit at a time, and also outputs data serially.

The logic diagram of a 4-bit serial-in, serial-out, shift-right, shift register is shown in Figure 11.4. With four stages, i.e. four FFs, the register can store upto four bits of data. Serial data is applied at the D input of the first FF. The Q output of the first FF is connected to the D input of the second FF, the Q output of the second FF is connected to the D input of the third FF and the Q output of the third FF is connected to the D input of the fourth FF. The data is outputted from the Q terminal of the last FF.

When serial data is transferred into a register, each new bit is clocked into the first FF at the positive-going edge of each clock pulse. The bit that was previously stored by the first FF is transferred to the second FF. The bit that was stored by the second FF is transferred to the third FF, and so on. The bit that was stored by the last FF is shifted out.

A shift register can also be constructed using J-K FFs or S-R FFs as shown in Figures 11.5a and 11.5b, respectively. The data is applied at the J(S) input of the first FF. The complement of this is fed to the K(R) terminal of the first FF. The Q output of the first FF is connected to J(S)

input of the second FF, the Q output of the second FF to J(S) input of the third FF, and so on. Also, $\bar{Q}_1$ is connected to K_2 (R_2), $\bar{Q}_2$ is connected to K_3 (R_3), and so on.

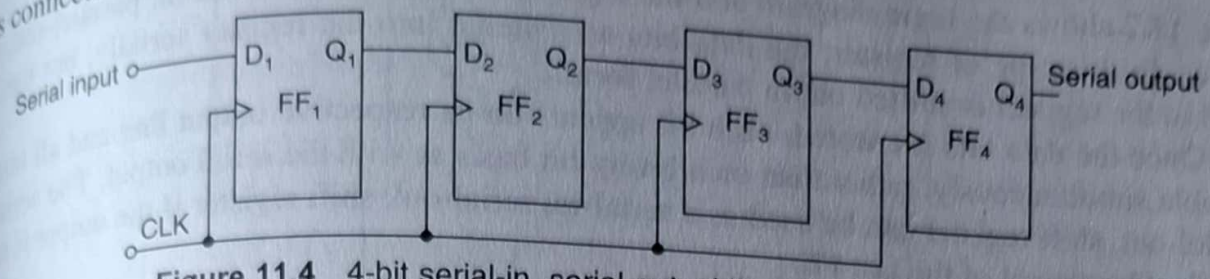
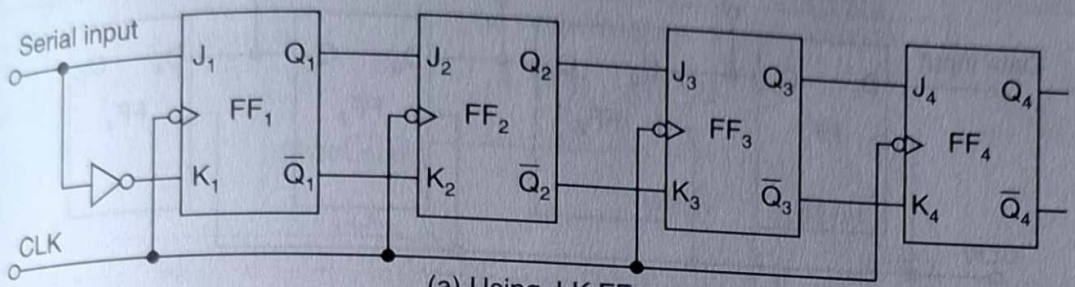
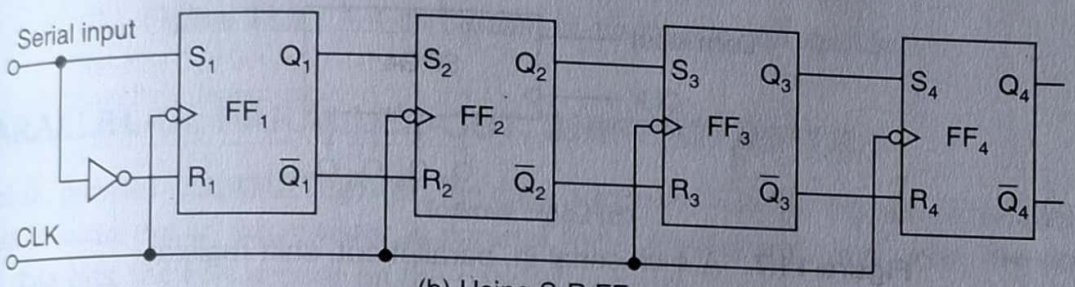


Figure 11.4 4-bit serial-in, serial-out, shift-right, shift register.



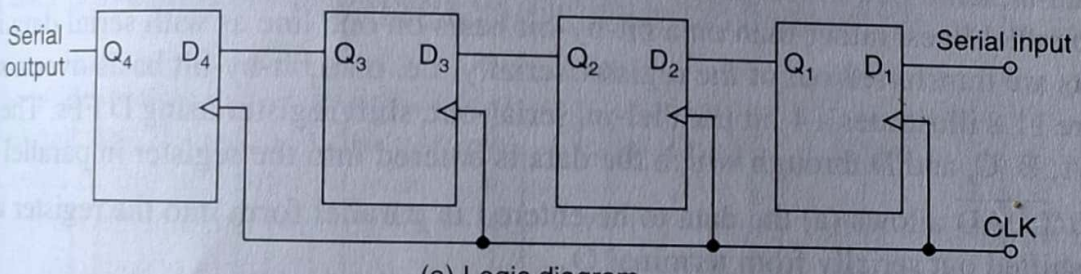
(a) Using J-K FFs



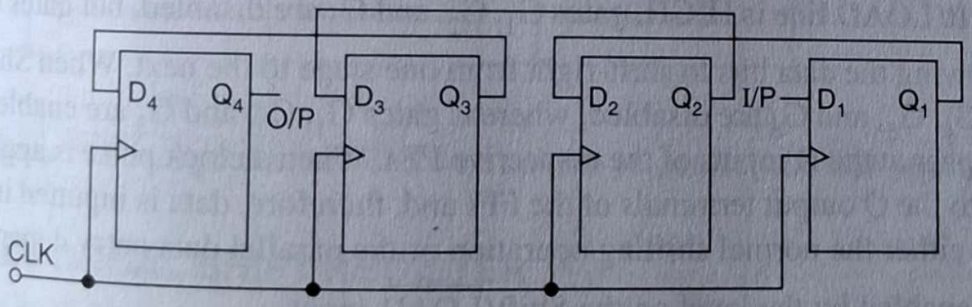
(b) Using S-R FFs

Figure 11.5 A 4-bit serial-in, serial-out, shift register.

Figure 11.6 shows the logic diagrams of a 4-bit serial-in, serial-out, shift-left, shift register.



(a) Logic diagram



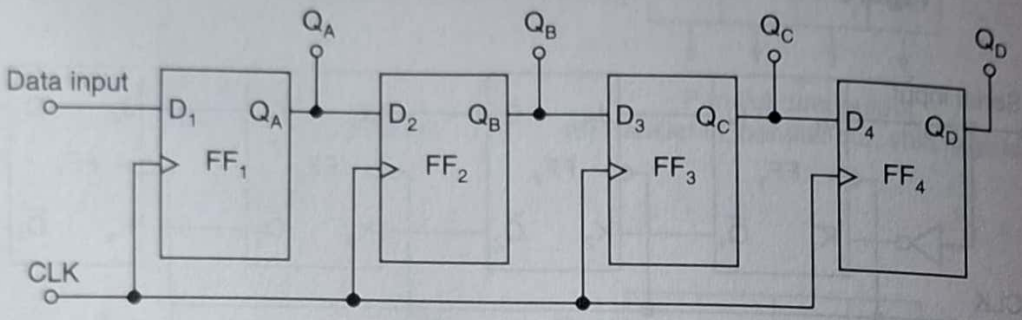
(b) Logic diagram

Figure 11.6 A 4-bit serial-in, serial-out, shift-left, shift register.

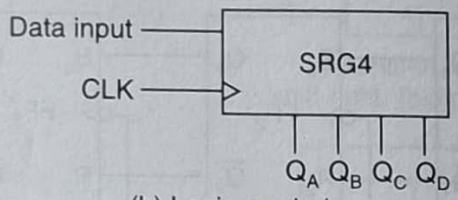
11.6 SERIAL-IN, PARALLEL-OUT, SHIFT REGISTER

Figure 11.7 shows the logic diagram and the logic symbol of a 4-bit serial-in, parallel-out, shift register. In this type of register, the data bits are entered into the register serially, but the data stored in the register is shifted out in parallel form.

Once the data bits are stored, each bit appears on its respective output line and all bits are available simultaneously, rather than on a bit-by-bit basis as with the serial output. The serial-in, parallel-out, shift register can be used as a serial-in, serial-out, shift register if the output is taken from the Q terminal of the last FF.



(a) Logic diagram



(b) Logic symbol

Figure 11.7 A 4-bit serial-in, parallel-out, shift register.

11.7 PARALLEL-IN, SERIAL-OUT, SHIFT REGISTER

For a parallel-in, serial-out, shift register, the data bits are entered simultaneously into their respective stages on parallel lines, rather than on a bit-by-bit basis on one line as with serial data inputs, but the data bits are transferred out of the register serially, i.e. on a bit-by-bit basis over a single line.

Figure 11.8 illustrates a 4-bit parallel-in, serial-out, shift register using D FFs. There are four data lines A, B, C, and D through which the data is entered into the register in parallel form. The signal Shift/$\overline{\text{LOAD}}$ allows (a) the data to be entered in parallel form into the register and (b) the data to be shifted out serially from terminal Q_4.

When Shift/$\overline{\text{LOAD}}$ line is HIGH, gates G_1, G_2, and G_3 are disabled, but gates G_4, G_5, and G_6 are enabled allowing the data bits to shift-right from one stage to the next. When Shift/$\overline{\text{LOAD}}$ line is LOW, gates G_4, G_5, and G_6 are disabled, whereas gates G_1, G_2, and G_3 are enabled allowing the data input to appear at the D inputs of the respective FFs. When a clock pulse is applied, these data bits are shifted to the Q output terminals of the FFs and, therefore, data is inputted in one step. The OR gate allows either the normal shifting operation or the parallel data entry depending on which AND gates are enabled by the level on the Shift/$\overline{\text{LOAD}}$ input.

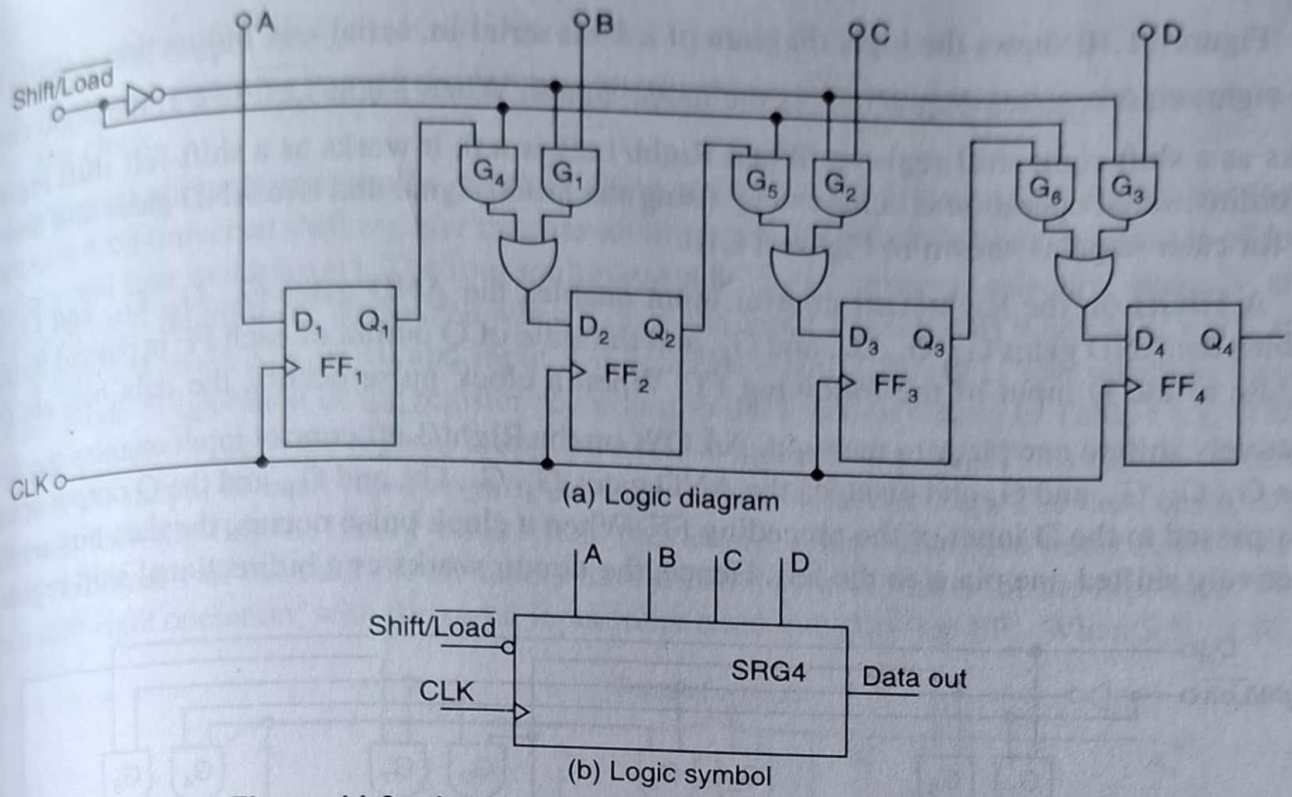


Figure 11.8 A 4-bit parallel-in, serial-out, shift register.

11.8 PARALLEL-IN, PARALLEL-OUT, SHIFT REGISTER

In a parallel-in, parallel-out, shift register, the data is entered into the register in parallel form, and also the data is taken out of the register in parallel form. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.

Figure 11.9 shows a 4-bit parallel-in, parallel-out, shift register using D FFs. Data is applied to the D input terminals of the FFs. When a clock pulse is applied, at the positive-going edge of that pulse, the D inputs are shifted into the Q outputs of the FFs. The register now stores the data. The stored data is available instantaneously for shifting out in parallel form.

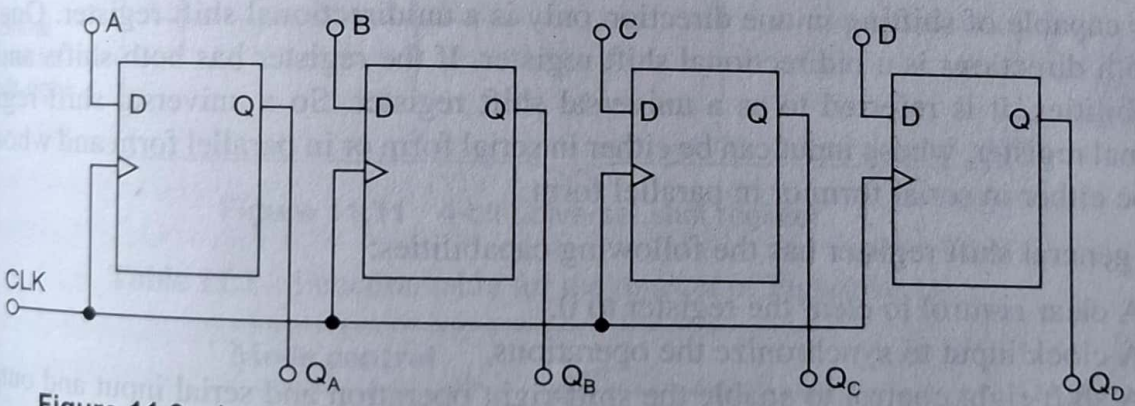


Figure 11.9 Logic diagram of a 4-bit parallel-in, parallel-out, shift register.

11.9 BIDIRECTIONAL SHIFT REGISTER

A bidirectional shift register is one in which the data bits can be shifted from left to right or from right to left.

Figure 11.10 shows the logic diagram of a 4-bit serial-in, serial-out, bidirectional (shift-left, shift-right) shift register. Right/$\overline{\text{Left}}$ is the mode signal. When Right/$\overline{\text{Left}}$ is a 1, the logic circuit works as a shift-right shift register. When Right/$\overline{\text{Left}}$ is a 0, it works as a shift-left shift register. The bidirectional operation is achieved by using the mode signal and two AND gates and one OR gate for each stage as shown in Figure 11.10.

A HIGH on the Right/$\overline{\text{Left}}$ control input enables the AND gates G_1, G_2, G_3, and G_4 and disables the AND gates G_5, G_6, G_7, and G_8, and the state of Q output of each FF is passed through the gate to the D input of the following FF. When a clock pulse occurs, the data bits are then effectively shifted one place to the right. A LOW on the Right/$\overline{\text{Left}}$ control input enables the AND gates G_5, G_6, G_7, and G_8 and disables the AND gates G_1, G_2, G_3, and G_4, and the Q output of each FF is passed to the D input of the preceding FF. When a clock pulse occurs, the data bits are then effectively shifted one place to the left. Hence, the circuit works as a bidirectional shift register.

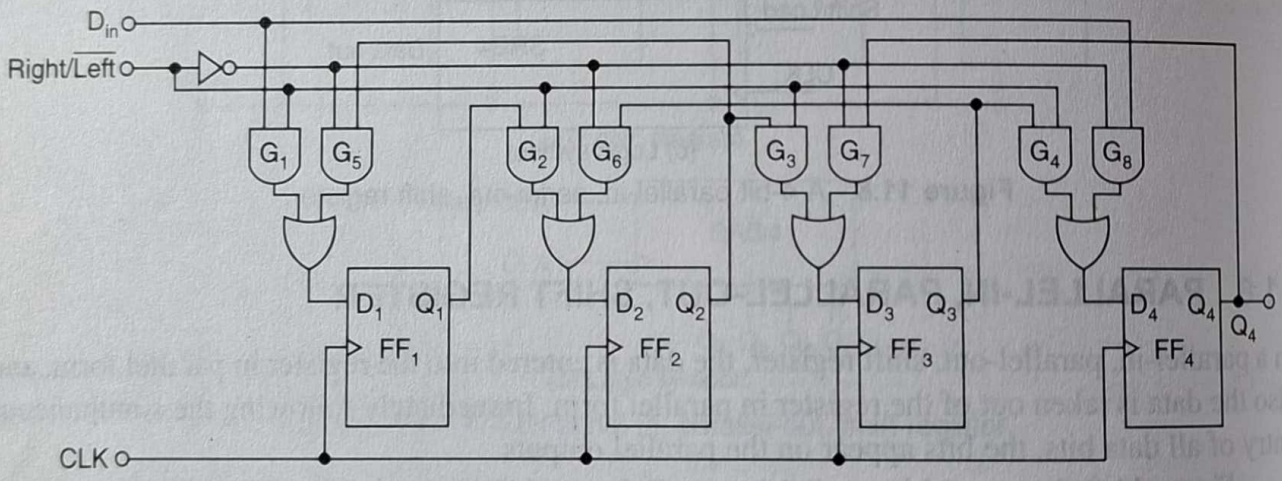


Figure 11.10 Logic diagram of a 4-bit bidirectional shift register.

11.10 UNIVERSAL SHIFT REGISTERS

A register capable of shifting in one direction only is a unidirectional shift register. One that can shift in both directions is a bidirectional shift register. If the register has both shifts and parallel load capabilities, it is referred to as a universal shift register. So a universal shift register is a bidirectional register, whose input can be either in serial form or in parallel form and whose output also can be either in serial form or in parallel form.

The most general shift register has the following capabilities:

1. A clear control to clear the register to 0.
2. A clock input to synchronize the operations.
3. A shift-right control to enable the shift-right operation and serial input and output lines associated with the shift-right.
4. A shift-left control to enable the shift-left operation and the serial input and output lines associated with the shift-left.
5. A parallel load control to enable a parallel transfer and the n input lines associated with the parallel transfer.