SM590/SM591/SM595

4-Bit Microcomputer (Controller for Low Power Systems)

■ Description

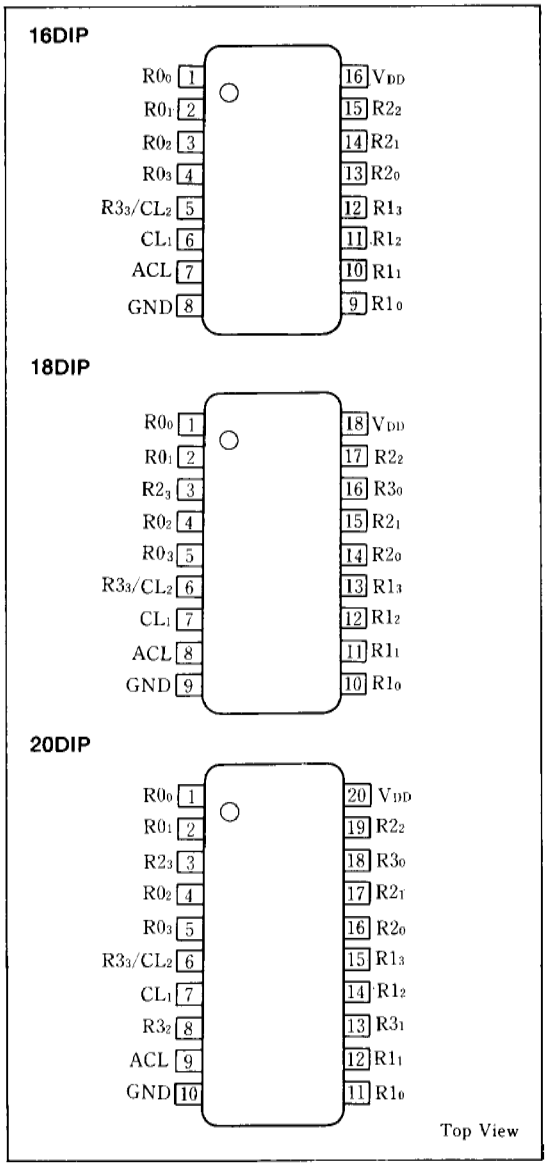
The SM590/SM591/SM592 is a CMOS 4-bit microcomputer which integrates a 762×8-bit ROM, a 41 instruction set, a 4-level subroutine stack, a 15 I/O port (for 20-pin DIP), and a stand-by function in a single chip.

Operated from 1 μs instruction cycle with low power consumption, this microcomputer is applicable to replacement of a compact controller circuit or any circuits consisting of conventional standard ICs.

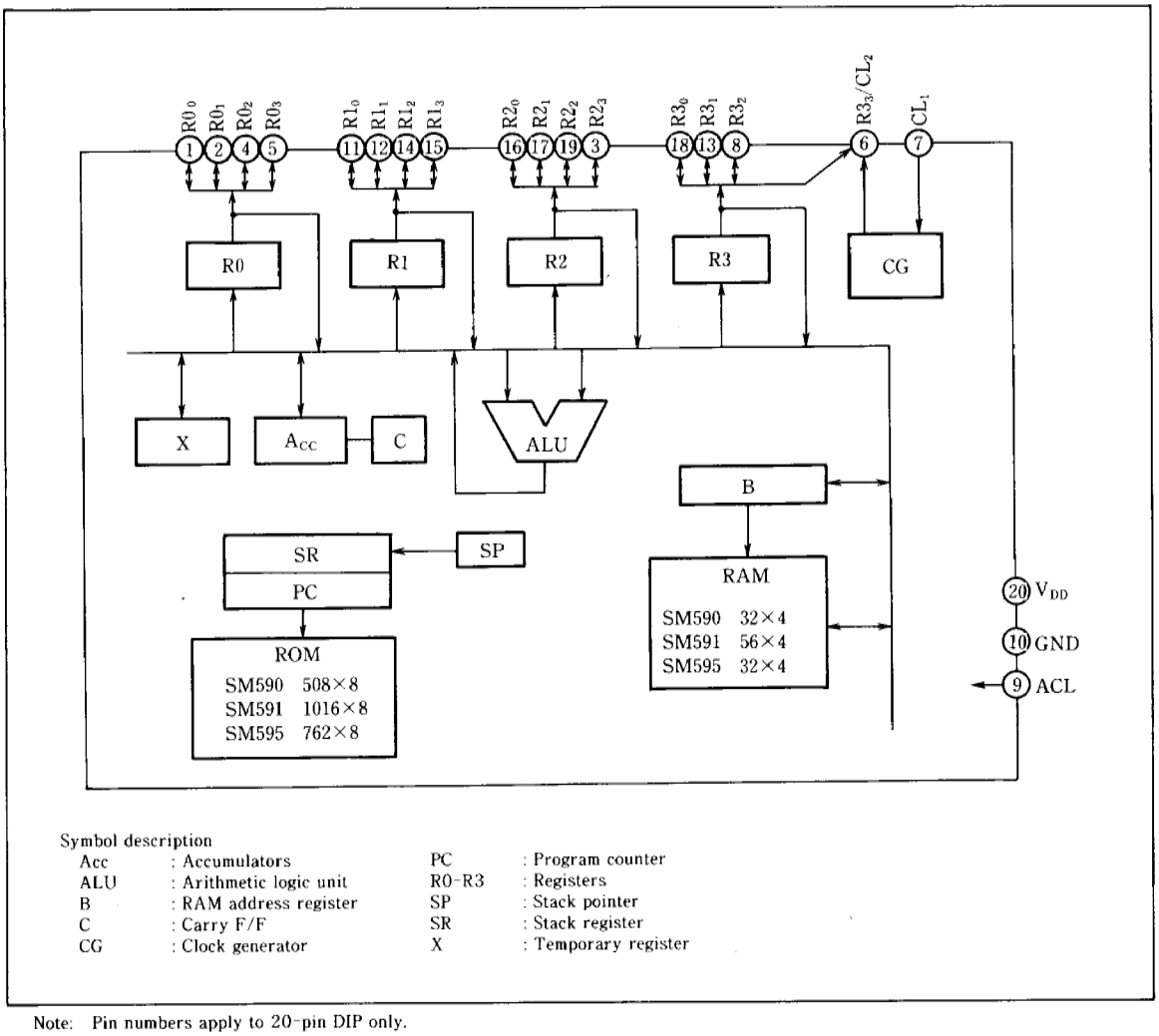
■ Features

1. CMOS process
2. ROM capacity
   SM590: 508×8 bits
   SM591: 1016×8 bits
   SM595: 762×8 bits
3. RAM capacity
   SM590: 32×4 bits
   SM591: 56×4 bits
   SM595: 32×4 bits
4. Instruction set 41
5. Subroutine nesting 4 levels
6. Input/Output ports
   11 bits (16DIP)
   13 bits (18DIP)
   15 bits (20DIP)
7. Output current (10 bits MAX.)
   SM590/SM591: 10mA (MAX.)
   SM595: 7mA (MAX.)
8. Clock oscillator
   - Ceramic oscillator
   - Resistor
   - External clock
9. Standby mode
10. Power supply (2.5 to 5.5V)
11. Instruction cycle
    V_{DD}=3V: 4 μs (MIN.)
    V_{DD}=5V: 1 μs (MIN.)
12. 16-pin DIP (DIP16-P-300)
    18-pin DIP (DIP18-P-300)
    20-pin DIP (DIP20-P-300)

■ Pin Connections



■ Block Diagram



Symbol description

Acc	: Accumulators	PC	: Program counter
ALU	: Arithmetic logic unit	R0-R3	: Registers
B	: RAM address register	SP	: Stack pointer
C	: Carry F/F	SR	: Stack register
CG	: Clock generator	X	: Temporary register

Note: Pin numbers apply to 20-pin DIP only.

■ Pin Description

Pin name	I/O	Circuit type	Function	Note
$R0_0$-$R0_3$	I/O	Pull down	Input/Output ports	1
$R1_0$-$R1_3$	I/O	Pull down	Input/Output ports	1
$R2_0$-$R2_3$	I/O	Pull down	Input/Output ports	2
$R3_0$-$R3_2$	I/O	Pull down	Input/Output ports	1
ACL	I	Pull down	Auto clear	
CL_1			System clock oscillation	
$R3_3/CL_2$	O		Output/system clock oscillation	3
V_{DD}			Power supply for logic circuit	
GND			Ground	

Note 1: Open drain I/O or CMOS outputs selectable with a mask option.
Note 2: Open drain I/O is selectable with a mask option.
Note 3: An external clock should be applied when the $R3_3$ output port is selected with a mask option.

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3 to +7.5	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Source output current sum	ΣI_{OH}	120	mA
Sync output current sum	ΣI_{OL}	20	mA
Operating temperature	Topr	−10 to +70	℃
Storage temperature	Tstg	−55 to +150	℃

■ Recommended Operating Conditions

(Ta=−10 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.5		5.5	V
Instruction cycle	t_{SYS}	V_{DD}=3V±0.5V	4		50	μs
		V_{DD}=5V±0.5V	1		50	

■ Electrical Characteristics

(V_{DD}=2.7 to 5.5V, Ta=−10 to +70℃)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}			0.7V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.3V_{DD}	V	
	V_{IH2}			V_{DD}−0.5		V_{DD}	V	2
	V_{IL2}			0		0.5	V	
	V_{IL3}	V_{DD}=5V±10%	SM590/SM591	0.7	1.4	2.1	V	3
		V_{DD}=3V	SM595			0.5		
		V_{DD}=5V	SM595			0.7		
	ΔV_I	V_{DD}=5V±10%	SM590/SM591	1.1	2.0	3.1	V	
	V_{IH3}	V_{DD}=3V	SM595	2.8			V	
		V_{DD}=5V	SM595	4.6				
Input current	I_{IH1}	V_{IN}=V_{DD}	V_{DD}=3V±10%	15	70	200	μA	1
			V_{DD}=5V±10%	70	250	750		
	I_{IH2}	V_{IN}=V_{DD}	V_{DD}=3V±10%		7	20	μA	4
			V_{DD}=5V±10%		20	60		
Current consumption	I_{A1}	t_{SYS}=2μs	V_{DD}=5V±10%		1	3	mA	5
	I_{A2}	t_{SYS}=10μs	V_{DD}=3V±10%		100	200	μA	
			V_{DD}=5V±10%		200	500		
	I_{ST}	Standby mode			1	2	μA	
Output current	I_{OH1}	V_{DD}=5V±10%	SM590/SM591	10			mA	6
		V_{OH}=V_{DD}−2V	SM595	7				
		V_{OH}=V_{DD}−0.5V		1				
	I_{OL1}	V_{OL}=0.4V	V_{DD}=5V±10%	1.6			mA	
		CMOS output		0.8				
		V_{OL}=0.4V	V_{DD}=5V±10%	15			μA	
		Pull-down output		8				
	I_{OH2}	V_{DD}=5V±10%	SM590/SM591	4			mA	7
		V_{OH}=V_{DD}−2V	SM595	3				
		V_{OH}=V_{DD}−0.5V	SM590/SM591	0.5				
			SM595	0.4				
	I_{OL2}	V_{OL}=0.4V	V_{DD}=5V±10%	15			μA	
		Pull-down output		8				
	I_{OH3}	V_{DD}=5V±10%	SM590/SM591	4			mA	8
		V_{OH}=V_{DD}−2V	SM595	3				
		V_{OH}=V_{DD}−0.5V	SM590/SM591	0.5				
			SM595	0.4				
	I_{OL3}	V_{OL}=0.4V	V_{DD}=5V±10%	1.6			mA	
		CMOS output		0.8				
		V_{OL}=0.4V	V_{DD}=5V±10%	15			μA	
		Pull-down output		8				
	I_{OH4}	V_{DD}=5V±10%	SM590/SM591	10			mA	9, 10
		V_{OH}=V_{DD}−2V	SM595	7				
		V_{OH}=V_{DD}−0.5V		1				
		V_{DD}=5V±10%	SM590/SM591	3				9, 11
		V_{OH}=V_{DD}−2V	SM595	2				
		V_{OH}=V_{DD}−0.5V	SM590/SM591	0.4				
			SM595	0.3				
	I_{OL4}	V_{OL}=0.4V	V_{DD}=5V±10%	1.6			mA	9
		CMOS output		0.8				
		V_{OL}=0.4V	V_{DD}=5V±10%	15			μA	
		Pull-down output		8				

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	Note
Output current	I_{OH5}	$V_{DD}=5V\pm10\%$	SM590/SM591	1			mA	12
		$V_{OH}=V_{DD}-2V$	SM595	0.7				
		$V_{OH}=V_{DD}-0.5V$	SM590/SM591	0.15				
			SM595	0.1				
	I_{OL5}	$V_{OL}=0.4V$	$V_{DD}=5V\pm10\%$	0.6			mA	
		CMOS output		0.3				

Note 1: Applied to pins $R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R3_0$–$R3_3$.
Note 2: Applied to pins ACL and CL_1.
Note 3: Applied to pin $R2_2$. (When a standby clear signal is input.)
V_{IL3}: Oscillation start input voltage (No oscillation is occurred under this level.)
V_{IH3}: Systemclock start voltage (See Fig. 7)
ΔV_1: $V_{IH3}-V_{IL3}$
Note 4: Applied to pin ACL.
Note 5: No load condition.
Note 6: Applied to pins $R0_0$–$R0_3$, $R1_0$–$R1_3$, $R3_1$.
Note 7: Applied to pins $R2_0$–$R2_3$.
Note 8: Applied to pin $R3_0$.
Note 9: Applied to pin $R3_2$.
Note10: When the content of R latch is output from the pin $R3_2$.
Note11: When the clock input to the pin CL_1 is output from pin $R3_2$.
Note12: Applied to pin $CL_2/R3_3$.

■ Oscillator Circuits

CL_1 and CL_2 are the clock oscillator input and output ports respectively. The basic clock signal can be obtained by the ceramic oscillator and resistor. The external clock signal may also be provided. (See Fig. 1.)

For an external clock input, provide the external clock to the CL_1 pin. In this case, the CL_2 pin can be used as the output pin ($R3_3$ pin) with a mask option.

The internal system clock is equivalent to the basic clock supplied to the CL_1 pin divided by four.

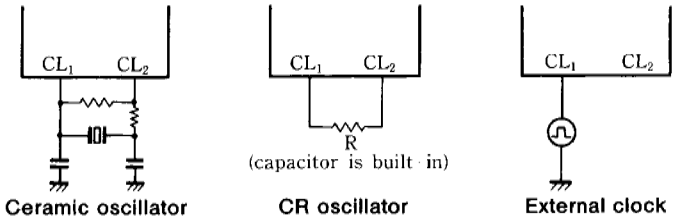
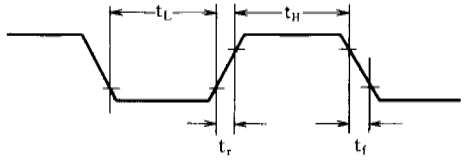


Fig. 1 Reference clock generator circuit

■ External Input Signal AC Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock rise time	t_r	$V_{DD}=2.5$ to $5.5V$			50	ns
Clock fall time	t_f	$V_{DD}=2.5$ to $5.5V$			50	
Clock pulse width	t_L	$V_{DD}=5V\pm0.5V$	0.08		6.3	μs
	t_H	$V_{DD}=3V\pm0.5V$	0.45		6.3	

Note: When external clock is input.



■ Pin Descriptions

(1) V_{DD}, GND (Power supply)

Apply 2.5 to 5.5V power supply to the V_{DD} pin with respect to GND pin which provides a reference level of the LSI.

(2) ACL (Reset pin)

The ACL pin is used to initialize the LSI. The LSI will be reset upon completion of two instruction cycles after ACL pin goes High. The ACL (reset) mode will be cleared upon completion of one instruction cycle after ACL pin goes LOW.

Connect a capacitor between ACL and V_{DD} to reset when power on. Two or more instruction cycles should be taken for the ACL input.

When a ceramic oscillator is used for a system clock, take a certain period of ACL time with the oscillation to be stabled.

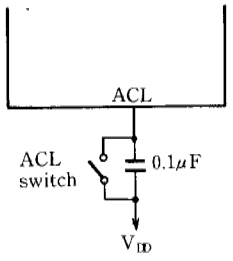


Fig. 2 ACL circuit

(3) $R3_i$-$R0_i$ (i=0 to 3) I/O pin

$R3_i$-$R0_i$ (i=0 to 3) pins may be used for both input and output, and a pull-down resistor is connected to the output buffer.

Data should be transferred between ports ($R3_i$-$R0_i$) specified by the BL and the accumulator (A_{CC}) or data memory by instructions.

When $R3_i$-$R0_i$ pins are used as inputs, reset the output latch and connect a pull-down resistor to the I/O pins.

Note: Upon completion of RTA instruction for $R3_2$ pin, the contents of an internal output latch are loaded into the accumulator A_{CC}.

The circuit type of $R3_i$-$R0_i$ can be used not only as a pull-down type but also as the following two types with a mask option.

Mask option I

When the R port is used as only output port with a large sink current, it can be replaced with the CMOS buffer.

Applicable pins:

$R0_0$-$R0_3$, $R1_0$-$R1_3$, $R3_0$-$R3_2$

Not applicable pins:

$R2_0$-$R2_3$

Mask option II

When the R port is used as only input port with a reduced current flowing into the pull-down resistor, it can be replaced with an open drain with a protective diode not to be pulled-down.

Note: The $CL_2/R3_3$ pin can be used as $R3_3$ output pin with a mask option, and the circuit type should be set to the CMOS buffer.

■ Hardware Configuration

(1) Program counter and stack

The ROM addresses can be specified by a program counter (PC).

The program counter (PC) consists of 10 bits including 1 bit (P_U) for the field specification, 2 bits (P_M) for the page specification and 7 bits (P_L) for the step specification.

The P_M for the page specification is a binary counter, and the P_L for the step specification is a polynomial counter (provided that it is inhibited for P_L=7F).

A 4-bit stack register enables 4 levels of subroutine nesting.

(2) Program memory (ROM)

The program memory (ROM) is used to store programs. See Fig. 3 and Fig. 4 for ROM configuration.

1 field has a configuration of 4pages×127 steps ×8 bits.

The SM590 has 508 bytes of ROM which consists of 1 field (0)×127 steps×4 pages.

The SM591 has 1016 bytes of ROM which consists of 2 fields (0 and 1)×127 steps×4 pages.

The SM595 has 762 bytes of ROM which consists of 1 field (0)×127 steps×4 pages+1 field (1)×127 steps×2 pages.

The ACL program starts at field 0, page 0 and step 0.

When the standby mode is cleared, execute the program at field 0, page 1 and step 0.

P_M \ P_U	Field 0	Field 1
Page 0	ACL start	
Page 1	Standby mode start	
Page 2		
Page 3		
	← SM590 →	
	← SM591 →	

Fig. 3 ROM configuration (SM590/SM591)

P_M \ P_U	Field 0	Field 1
Page 0	ACL start	
Page 1	Standby mode start	
Page 2		
Page 3		

Fig. 4 ROM configuration (SM595)

The TR instruction is used to jump within a page, while the TL (two-word) instruction is used to jump to any desired address. The TLS instruction executes a subroutine jump to any desired address.

(3) Data memory (RAM) and B register

The data memory (RAM) is used to store data. The RAM size of the SM590 and SM595 is 16×2 ×4 (128 bits), while that of the SM591 is 16×3.5 ×4 (244 bits).

Each file consists of a 16 word×4-bit configuration as shown in Fig. 5.

The RAM address is specified by a B register composed of 1-bit for the SM590/SM595 or 2 bits for the SM591 of B_M and 4 bits of B_L.

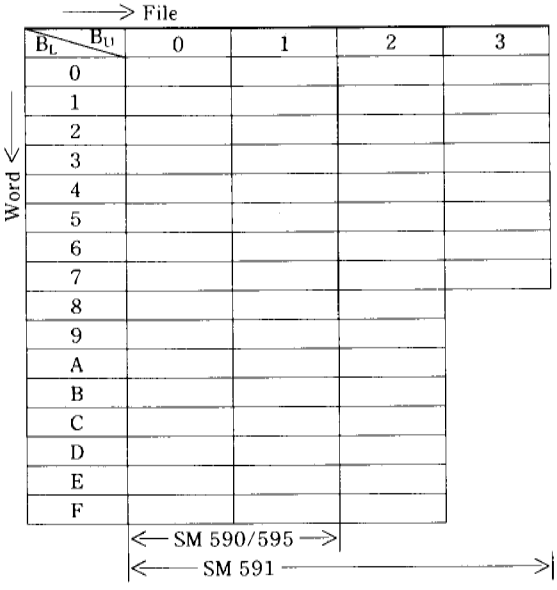


Fig. 5 RAM Configuration

(4) Accumulator (A_{CC}) and X register

The accumlator (A_{CC}) is a 4-bit register. It transfers data to I/O ports and performs operations in combination with an arithmetic and logic unit (ALU), a carry flag (C) and a RAM.

The X register is a 4-bit register used as a temporary register which transfers and compares data with the A_{CC}.

(5) Arithmetic and logic unit (ALU) and carry flag (C)

The arithmetic and logic unit (ALU) performs 4-bit parallel arithmetic operations. Executing the ADC and ADCS instructions shifts the carry of operations into the carry flag (C).

(6) Output latches (R [0], R [1] R [2], R[3])

The output latches consist of 16 bits. 11 bits for 16 pin package, 13 bits for 18 pin package and 15 bits for 20 pin package of the output latches are connected to external pins. The rest of the output latches not connected to external pins can be used as temporary registers.

The R output latches are specified by B_L.

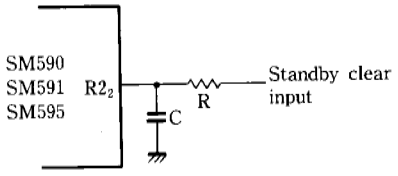


Fig. 6

(7) System clock generator circuit

The system clock generator circuit divides the basic clock supplied from the CL_1 pin, generates the system clock.

The circuit externally outputs the clock signals generated from clock oscillators (CL_1, CL_2) through $R3_2$ pin with a mask option.

This function enables to be synchronized with other LSIs.

Note that the instruction cycle time of 1 word instruction is equivalent to 1 cycle of system clocks.

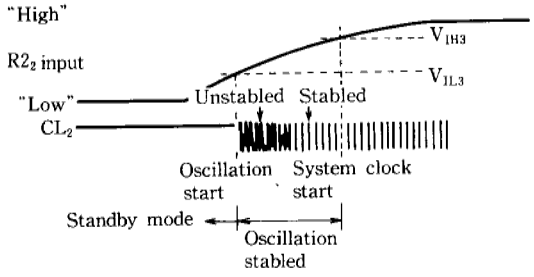


Fig. 7 Clock timing for a ceramic ascillator

(8) Standby function

Executing an instruction places the device in standby mode to reduce current consumption.

The oscillator and the system clock are iactivated in standby mode.

When the $R2_2$ accepts High level in standby mode, the standby mode is cleared and restarts program execution at field 0, page 1 and step 0.

If a ceramic oscillator is used as a clock generator, a delay circuit shown in Fig. 6 is required to obtain the clock oscillation time to be stabled.

Fig. 7 shows the timing in this case.

(9) Reset function (ACL)

Applying a High level signal to the ACL pin resets the carry flag (c) and the output latch, and the input pins are pulled-down.

Be sure not to apply High level to both $R2_0$ and $R2_1$ pins in the reset (ACL) mode.

Applying a Low level signal to the ACL pin starts execution of the program at field 0, page 0, step 0.

■ Instruction Set

(1) ROM address instructions

Mnemonic	Machine code	Operation
TR x	80-FE	$P_L \leftarrow I_6\text{-}I_0$ (jump within a page)
TL xyz	78-7B	$P_U \leftarrow I_9$, $P_M \leftarrow I_8$, I_7
	00-FE	$P_L \leftarrow I_6\text{-}I_0$ (jump to any page)
TLS xyz	7C-7F	$SP \leftarrow SP+1$, $SR \leftarrow PC+2$
	00-FE	$P_U \leftarrow I_9$, $P_M \leftarrow I_8$, I_7, $P_L \leftarrow I_6\text{-}I_0$
RTN	4C	$SP \leftarrow SP-1$, $PC \leftarrow SR$
RTNS	4D	$SP \leftarrow SP-1$, $PC \leftarrow SR$, Skip

(2) Data transfer instructions

Mnemonic	Machine code	Operation
LAX x	30-3F	$A_{CC} \leftarrow I_3\text{-}I_0$ Skip if last instruction is LAX
LBLX x	20-2F	$B_L \leftarrow I_3\text{-}I_0$
LBMX x	74-77	$B_M \leftarrow I_1, I_0$
STR	4A	$M \leftarrow A_{CC}$
LDA	40	$A_{CC} \leftarrow M$
EXC	41	$M \longleftrightarrow A_{CC}$
EXCI	42	$M \longleftrightarrow A_{CC}$, $B_L \leftarrow B_L+1$ Skip if Carry = 1
EXCD	43	$M \longleftrightarrow A_{CC}$, $B_L \leftarrow B_L-1$ Skip if Borrow = 1
EXAX	5D	$A_{CC} \longleftrightarrow X$
ATX	5C	$X \leftarrow A_{CC}$
XBLA	57	$A_{CC} \longleftrightarrow B_L$
BLTA	56	$A_{CC} \leftarrow B_L$

(3) Arithmetic instructions

Mnemonic	Machine code	Operation
ADX x	00-0F	$A_{CC} \leftarrow A_{CC}+x$, Skip if Carry = 1
ADD	70	$A_{CC} \leftarrow A_{CC}+M$
ADS	71	$A_{CC} \leftarrow A_{CC}+M$, Skip if Carry = 1
ADC	72	$A_{CC} \leftarrow A_{CC}+M+C$, $C \leftarrow$ Carry
ADCS	73	$A_{CC} \leftarrow A_{CC}+M+C$, $C \leftarrow$ Carry Skip if Carry = 1
COMA	44	$A_{CC} \leftarrow \overline{A_{CC}}$
INBL	52	$B_L \leftarrow B_L+1$, Skip if Carry = 1
DEBL	53	$B_L \leftarrow B_L-1$, Skip if Borrow = 1
INBM	50	$B_M \leftarrow B_M+1$
DEBM	51	$B_M \leftarrow M_M-1$

(4) Test instructions

Mnemonic	Machine code	Operation
TAX x	10-1F	Skip if $A_{CC} = x$
TBA x	64-67	Skip if $A_{CCX} = 1$ (x = 3 to 0)
TM x	60-63	Skip if Mx = 1 (x = 3 to 0)
TAM	45	Skip if $A_{CC} = M$
TC	54	Skip if C = 1

(5) Bit manipulation instructions

Mnemonic	Machine code	Operation
SM x	6C-6F	$Mx \leftarrow 1$ (x = 3 to 0)
RM x	68-6B	$Mx \leftarrow 0$ (x = 3 to 0)
SC	49	$C \leftarrow 1$
RC	48	$C \leftarrow 0$

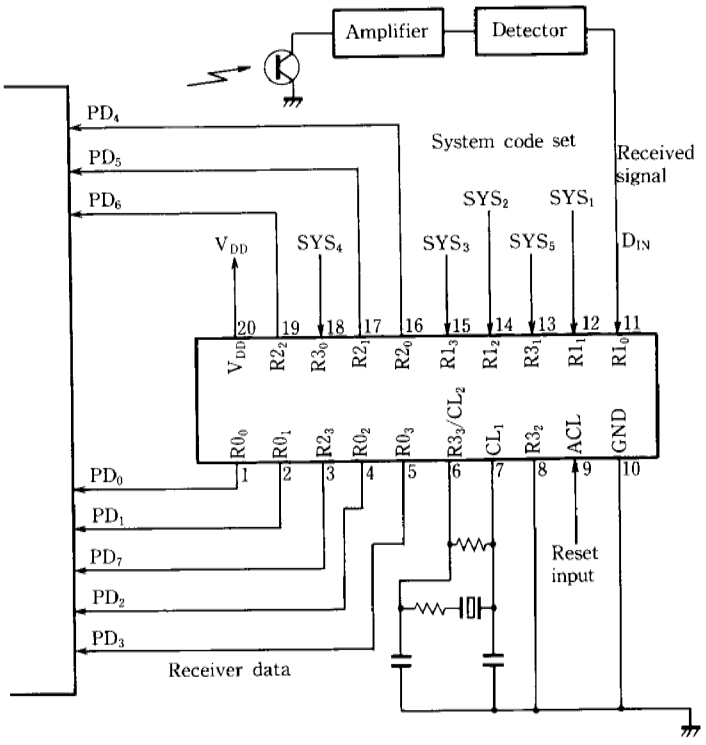
(6) I/O instructions

Mnemonic	Machine code	Operation
ATR	46	$R(B_L) \leftarrow A_{CC}$
MTR	47	$R(B_L) \leftarrow M$
RTA	55	$A_{CC} \leftarrow R(B_L)$

(7) Special instructions

Mnemonic	Machine code	Operation
NOP	00	No Operation
CCTRL	4B	Standby Mode

■ System Configuration Example



Remote control receiver