```
1   //
2   //
3   // a gated d latch
4   module d_latch (
5      Clk,
6      D,
7      Q
8   );
9
10  input Clk, D;
11  output Q;
12
13  wire S, R, R_g, S_g, Qa, Qb /* synthesis keep */ ;
14
15  assign S = D;
16  assign R = ~D;
17
18  assign R_g = R & Clk;
19  assign S_g = S & Clk;
20  assign Qb = ~(~R_g & Qa);
21  assign Qa = ~(~S_g & Qb);
22
23  assign Q = Qa;
24
25  endmodule
26
27
28  module Part2(
29     SW,
30     LEDR
31  );
32
33  input [1:0] SW;
34  output [1:0] LEDR;
35
36  d_latch(SW[0], SW[1], LEDR[0]);
37
38  endmodule
39
```