```
1   // A gated RS latch
2   // Neil Nie
3
4   module RSLatch (
5      Clk,
6      R,
7      S,
8      Q
9   );
10
11  input Clk, R, S;
12  output Q;
13
14  wire R_g, S_g, Qa, Qb /* synthesis keep */;
15
16  assign R_g = R & Clk;
17  assign S_g = S & Clk;
18  assign Qa = ~(R_g | Qb);
19  assign Qb = ~(S_g | Qa);
20
21  assign Q = Qa;
22
23  endmodule
24
25  module Part1(
26     SW,
27     LEDR,
28  );
29
30  input [3:0] SW;
31  output LEDR;
32
33  endmodule
34
```