```
1   //
2
3   module d_flip_flop(
4
5      clk,
6      D,
7      Q
8   );
9
10  input D, clk;
11  output Q;
12
13  wire Qm, Qs;
14
15  d_latch(~clk, D, Qm);
16  d_latch(clk, Qm, Qs);
17
18  assign Q = Qs;
19
20  endmodule
21
22  // A gated d latch
23  module d_latch (
24     Clk,
25     D,
26     Q
27  );
28
29  input Clk, D;
30  output Q;
31
32  wire S, R, R_g, S_g, Qa, Qb /* synthesis keep */ ;
33
34  assign S = D;
35  assign R = ~D;
36
37  assign R_g = R & Clk;
38  assign S_g = S & Clk;
39  assign Qb = ~(~R_g & Qa);
40  assign Qa = ~(~S_g & Qb);
41
42  assign Q = Qa;
43
44  endmodule
45
46  module Part3(
47     SW,
48     LEDR
49  );
50
51  input [1:0] SW;
52  output [1:0] LEDR;
53
54  d_flip_flop(SW[0], SW[1], LEDR[0]);
55
56  endmodule
57
58
```