```
1   //
2   // Digital Logic Lab Part 3
3   // Ripple Carry Adder
4   // (c) Neil Nie
5   // Oct 31st, 2018
6   //
7
8   module full_adder(
9
10      a,
11      b,
12      out,
13      cin,
14      cout
15  );
16
17  input a;
18  input b;
19  input cin;
20  output out;
21  output cout;
22
23  assign cout = (a & b) | cin & (~a & b | ~b & a);
24  assign out = cin & ~a & ~b | ~cin & ~a & b | cin & a & b | ~cin & a & ~b;
25
26  endmodule
27
28  module Part3(
29
30      SW,
31      LEDR
32
33  );
34
35  input [7:0] SW;
36  output [3:0] LEDR;
37
38  endmodule
39
```