```
 1
 2
 3   module ped_flip_flop(clk, D, Q);
 4
 5   input D, clk;
 6   output Q;
 7
 8   wire Qm, Qs;
 9
10   gated_d_latch latch1(
11      .clk(~clk),
12      .D(D),
13      .Q(Qm)
14   );
15
16   gated_d_latch latch2(
17      .clk(clk),
18      .D(Qm),
19      .Q(Qs)
20   );
21
22   assign Q = Qs;
23
24   endmodule
25
```