```
1
2   module clock_1hz(clk, out);
3
4   input clk;
5   output out;
6
7   // generate 1 Hz from 50 MHz
8   reg [25:0] count_reg = 0;
9   reg out_1hz = 0;
10
11  always @(posedge clk) begin
12
13      if (count_reg < 25000000) begin
14          count_reg <= count_reg + 1;
15      end else begin
16          count_reg <= 0;
17          out_1hz <= ~out_1hz;
18      end
19  end
20
21  assign out = out_1hz;
22
23  endmodule
24
```