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1   //
2   // Verilog Lab Part 5
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4   // CS 603, Ben Bakker
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6   //
7
8   // Lab Part 3
9
10  module two_bit_4to1_mux(
11     in0,
12     in1,
13     in2,
14     in3,
15     sel,
16     out
17  );
18
19  input [1:0] in0;
20  input [1:0] in1;
21  input [1:0] in2;
22  input [1:0] in3;
23  input [1:0] sel;
24  output [1:0] out;
25
26  wire [1:0] buffer_1;
27  wire [1:0] buffer_2;
28
29  assign buffer_1[0] = (~sel[0] & in0[1]) | (sel[0] & in1[1]);
30  assign buffer_1[1] = (~sel[0] & in0[0]) | (sel[0] & in1[0]);
31  assign buffer_2[0] = (~sel[0] & in2[1]) | (sel[0] & in3[1]);
32  assign buffer_2[1] = (~sel[0] & in2[0]) | (sel[0] & in3[0]);
33
34  assign out[1] = (~sel[1] & buffer_1[0]) | (sel[1] & buffer_2[0]);
35  assign out[0] = (~sel[1] & buffer_1[1]) | (sel[1] & buffer_2[1]);
36
37  endmodule
38
39  module display(
40     in,
41     hex
42  );
43
44  input [1:0] in;
45  output [6:0] hex;
46
47  assign hex[0] = (~in[1] & ~in[0]) + (in[1] & ~in[0]);
48  assign hex[1] = (~in[1] & in[0]);
49  assign hex[2] = (~in[1] & in[0]);
50  assign hex[3] = (in[1] & ~in[0]);
51  assign hex[4] = (in[1] & ~in[0]);
52  assign hex[5] = (~in[1] & ~in[0]) + (in[1] & ~in[0]);
53  assign hex[6] = (in[1] & ~in[0]) + (in[1] & in[0]);
54
55  endmodule
56
57
58  module Part5(
59
60     SW,
61     HEX0,
62     HEX1,
63     HEX2,
64     HEX3
65  );
66
67  input  [9:0] SW;
68  output [6:0] HEX0;
69  output [6:0] HEX1;
70  output [6:0] HEX2;
71  output [6:0] HEX3;
72
73  wire [1:0] mux0_out;
74  wire [1:0] mux1_out;
75  wire [1:0] mux2_out;
76  wire [1:0] mux3_out;
```

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77
78    two_bit_4to1_mux(SW[1:0], SW[3:2], SW[5:4], SW[7:6], SW[9:8], mux0_out);
79    two_bit_4to1_mux(SW[3:2], SW[5:4], SW[7:6], SW[1:0], SW[9:8], mux1_out);
80    two_bit_4to1_mux(SW[5:4], SW[7:6], SW[1:0], SW[3:2], SW[9:8], mux2_out);
81    two_bit_4to1_mux(SW[7:6], SW[1:0], SW[3:2], SW[5:4], SW[9:8], mux3_out);
82
83    wire [6:0] display_out0;
84    wire [6:0] display_out1;
85    wire [6:0] display_out2;
86    wire [6:0] display_out3;
87
88    display(mux0_out, display_out0);
89    display(mux1_out, display_out1);
90    display(mux2_out, display_out2);
91    display(mux3_out, display_out3);
92
93
94    assign HEX0 = display_out0;
95    assign HEX1 = display_out1;
96    assign HEX2 = display_out2;
97    assign HEX3 = display_out3;
98
99
100   endmodule
101
102
```