```
1   //
2   // Part 4 Verilog
3   // Neil Nie
4   // (C) Oct 24th, 2018
5   // Seven Segment Decoder
6
7   module Part4(
8
9      SW,
10     HEX0
11
12  );
13
14  input [1:0] SW;
15  output [6:0] HEX0;
16
17  wire [1:0] in;
18
19  assign in = SW;
20
21  assign HEX0[0] = ~in[1] & ~in[0];
22  assign HEX0[1] = (~in[1] & in[0]);
23  assign HEX0[2] = (~in[1] & in[0]) + (in[1] & ~in[0]);
24  assign HEX0[3] = 0;
25  assign HEX0[4] = 0;
26  assign HEX0[5] = (~in[1] & ~in[0]) + (in[1] & ~in[0]);
27  assign HEX0[6] = 0;
28
29  endmodule
30
```