```
1   //
2   // Lab Part 3
3   // Neil Nie (c) 2018
4   //
5
6   module Part3(
7
8      SW,
9      LEDR
10
11  );
12
13  input [9:0] SW;
14  output [1:0] LEDR;
15
16  wire [1:0] U;
17  wire [1:0] V;
18  wire [1:0] W;
19  wire [1:0] X;
20  wire [1:0] out;
21  wire [1:0] sel;
22  wire [1:0] buffer_1;
23  wire [1:0] buffer_2;
24
25  assign U = SW[1:0];
26  assign V = SW[3:2];
27  assign W = SW[5:4];
28  assign X = SW[7:6];
29  assign sel = SW[9:8];
30
31  assign buffer_1[1] = (~sel[0] & U[1]) | (sel[0] & V[1]);
32  assign buffer_1[0] = (~sel[0] & U[0]) | (sel[0] & V[0]);
33  assign buffer_2[1] = (~sel[0] & W[1]) | (sel[0] & X[1]);
34  assign buffer_2[0] = (~sel[0] & W[0]) | (sel[0] & X[0]);
35
36  assign LEDR[1] = (~sel[1] & buffer_1[0]) | (sel[1] & buffer_2[0]);
37  assign LEDR[0] = (~sel[1] & buffer_1[1]) | (sel[1] & buffer_2[1]);
38
39  endmodule
40
```