```
1   //
2   // Learning Verilog
3   // Lab 1
4   // Neil Nie, (c) 2018
5   //
6
7   module Part2(
8      SW,       // the switchs
9      LEDR      // output LEDs
10  );
11
12
13  input [8:0] SW;   // assign those switches as inputs
14  output [3:0] LEDR;// assigne the LEDs as outputs
15
16  wire X;
17  wire Y;
18  wire S;
19
20  assign X = SW[3:0];
21  assign Y = SW[7:4];
22  assign S = SW[8];
23
24  //assign LEDR
25
26  assign LEDR[3] = (~SW[8] & SW[3]) | (SW[8] & SW[7]);
27  assign LEDR[2] = (~SW[8] & SW[2]) | (SW[8] & SW[6]);
28  assign LEDR[1] = (~SW[8] & SW[1]) | (SW[8] & SW[5]);
29  assign LEDR[0] = (~SW[8] & SW[0]) | (SW[8] & SW[4]);
30
31
32  endmodule
33
```