8088,80286 MICROPROCESSORS AND ISA BUS

OBJECTIVES

this chapter enables the student to:

- State the function of the pins of the 8088.
- List the functions of the 8088 data, address, and control buses.
- State the differences in the 8088 microprocessor in maximum mode versus minimum mode.
- Describe the function of the pins of the 8284 clock generator chip.
- Describe the function of the pins of the 8288 bus controller chip.
- Explain the role of the 8088, 8284A, and 8288.

OBJECTIVES (cont)

this chapter enables the student to:

- Explain how bus arbitration between the CPU and DMA is accomplished.
- State the function of the pins of the 80286.
- Describe the differences between real and protected modes.
- Describe the operation of the 80286 data, address, and control buses.
- Describe the purpose of the expansion slots of the IBM PC AT (ISA)bus.
- Describe the ISA bus system.

8088 MICROPROCESSOR

- 8088 is a 40-pin microprocessor chip that can work in two modes: minimum mode and maximum mode.
  - Maximum mode is used to connect to 8087 coprocessor.
    - If a coprocessor is not needed, 8088 is used in minimum mode.

8088 MICROPROCESSOR data bus

– Due to chip packaging limitations in the 1970s, there was great effort to use the minimum number of pins for external connections.
  - Intel multiplexed address & data buses, using the same pins to carry two sets of information: address & data.
– Pins 9-16 (**AD0–AD7**) are used for both data and addresses in 8088.
  - **AD** stands for "address/data."
– The **ALE** (address latch enable) pin signals whether the information on pins AD0–AD7 is address or data.

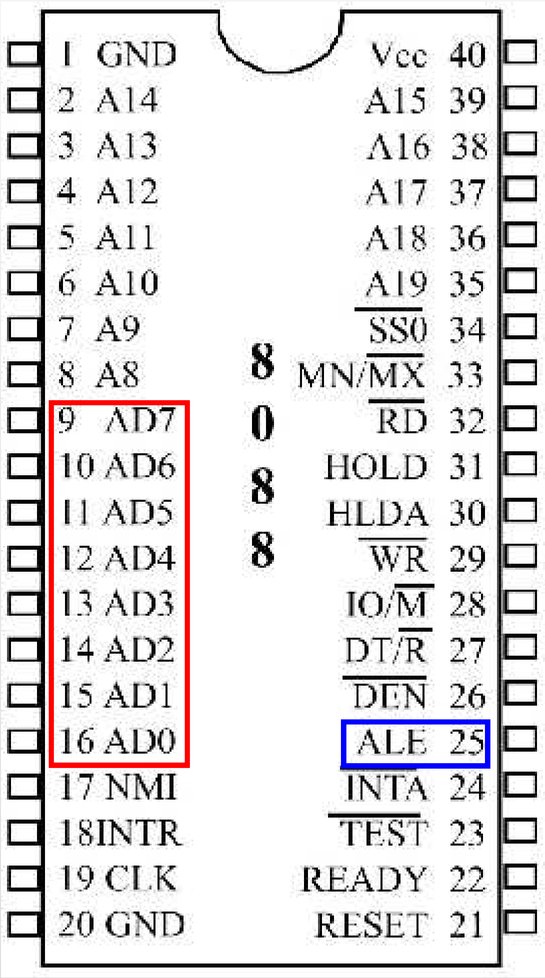


Fig. 9-1a 8088 in minimum mode

8088 MICROPROCESSOR
data bus

- When 8088 sends out an address, it activates (sets *high*) the **ALE**, to indicate the information on pins **AD0**–**AD7** is the *address* (**A0**–**A7**).
  - This information must be *latched*, then pins AD0–AD7 are used to carry data.
- When data is to be sent out or in, **ALE** is low, which indicates that **AD0**–**AD7** will be used as *data* buses (**D0**–**D7**).
- The process of separating address and data from pins AD0–AD7 is called *demultiplexing*.

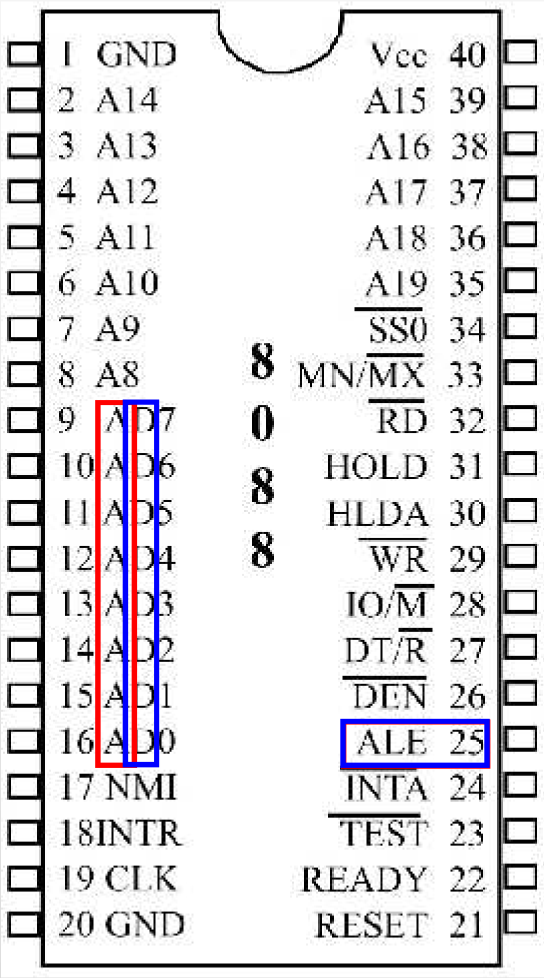


Fig. 9-1a 8088 in minimum mode

8088 MICROPROCESSOR address bus

- 8088 has 20 address pins (**A0–A19**), allowing it to address a maximum of one megabyte of memory (2^{20} = 1M).
  - To demultiplex address signals, a latch must be used to grab the addresses.
- Widely used is the 74LS373 IC, also 74LS573, a 74LS373 variation.
  - **AD0** to **AD7** go to the 74LS373 latch, providing the 8-bit address **A0–A7**.
  - **A8–A15** come directly from the microprocessor (pins **2–8** & pin **39**).
- The last 4 bits of the address come from **A16–A19**, pin numbers **35–38**.

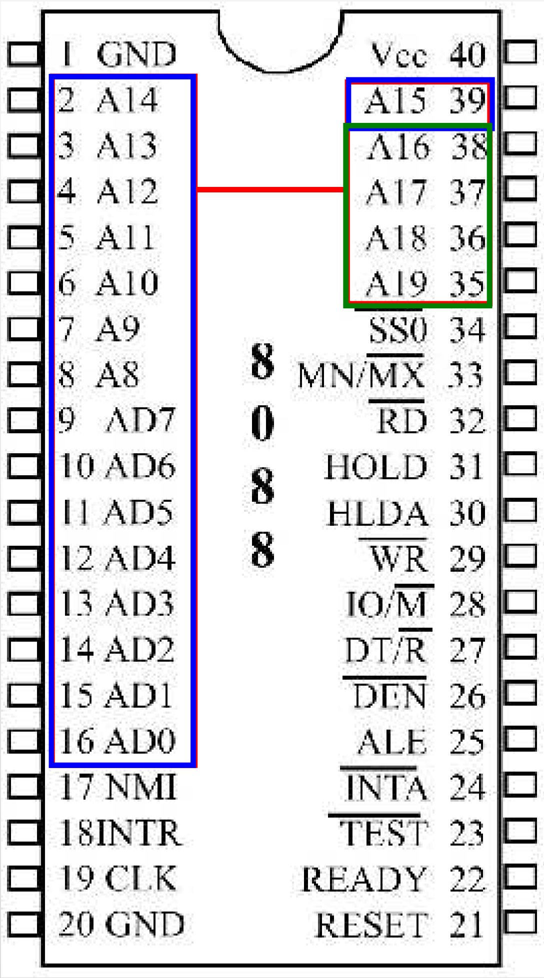


Fig. 9-1a 8088 in minimum mode

8088 MICROPROCESSOR
address bus

The most widely used latch is the 74LS373 IC.
Also used is the 74LS573, a 74LS373 variation.

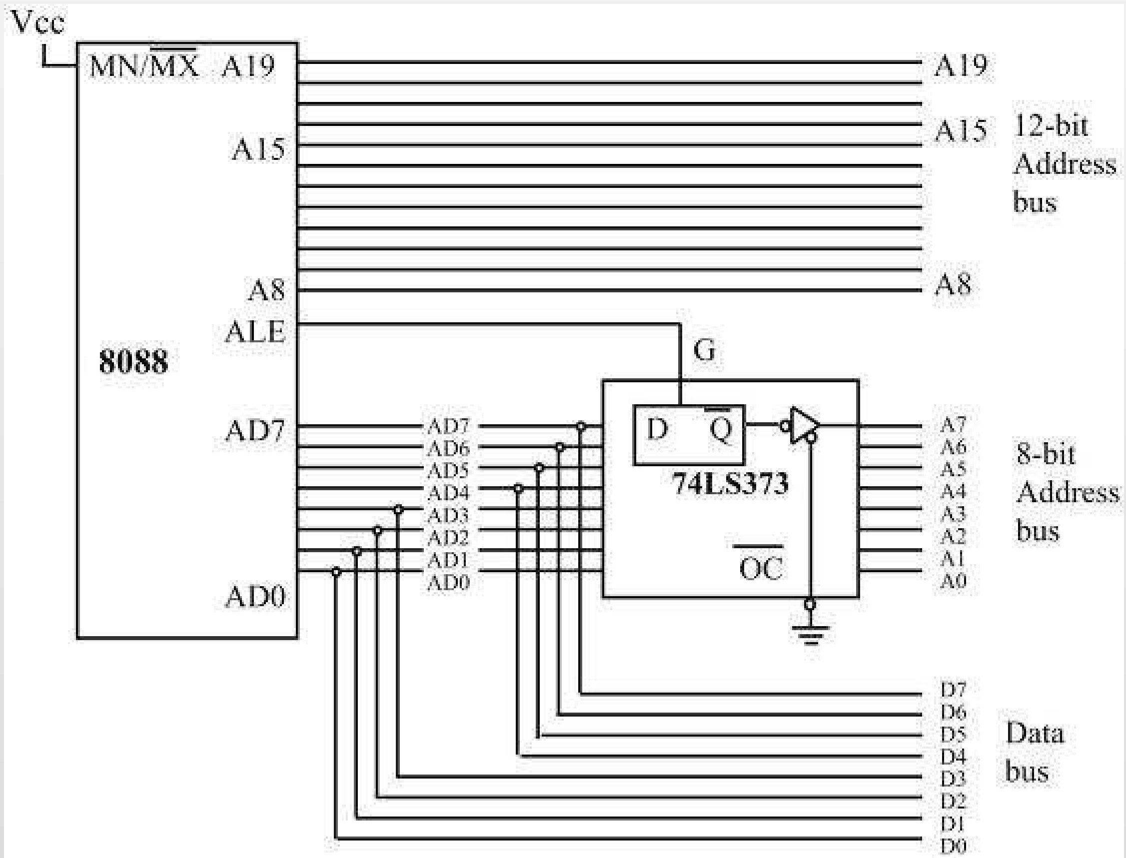
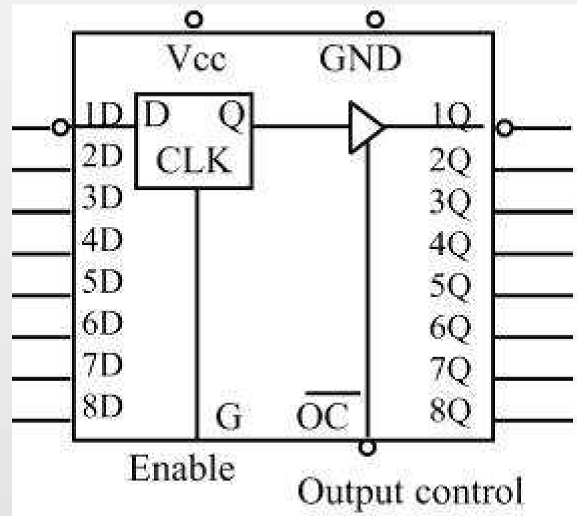


Fig. 9-2 Role of ALE in address/data demultiplexing

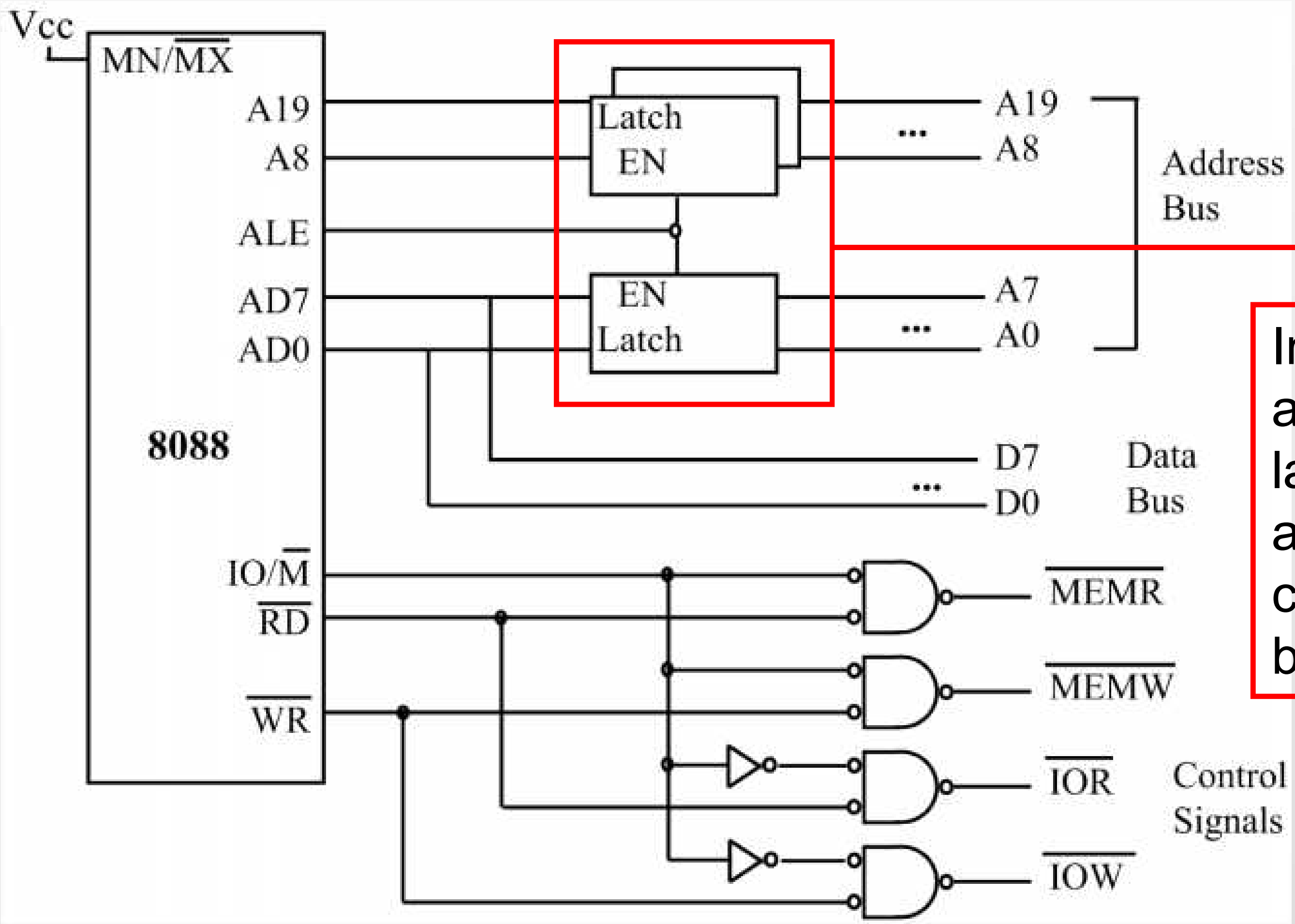


Function Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Fig. 9-3 74 LS373 D Latch

8088 MICROPROCESSOR
address bus



In any system, all addresses must be latched to provide a stable, high-drive-capability address bus.

Fig. 9-5 Address,Data,and Control Buses in 8088-based System

8088 MICROPROCESSOR
control bus

- 8088 can access both memory and I/O devices for read and write operations, four operations, which need four control signals:
  - $\overline{\textbf{MEMR}}$ (memory read); $\overline{\textbf{MEMW}}$ (memory write).
  - $\overline{\textbf{IOR}}$ (I/O read); $\overline{\textbf{IOW}}$ (I/O write).

8088 MICROPROCESSOR control bus

- 8088 provides three pins for control signals:
  - RD, WR, and IO/$\overline{M}$.
    - RD & WR pins are both *active-low*.
    - IO/$\overline{M}$ is *low* for memory, *high* for I/O devices.

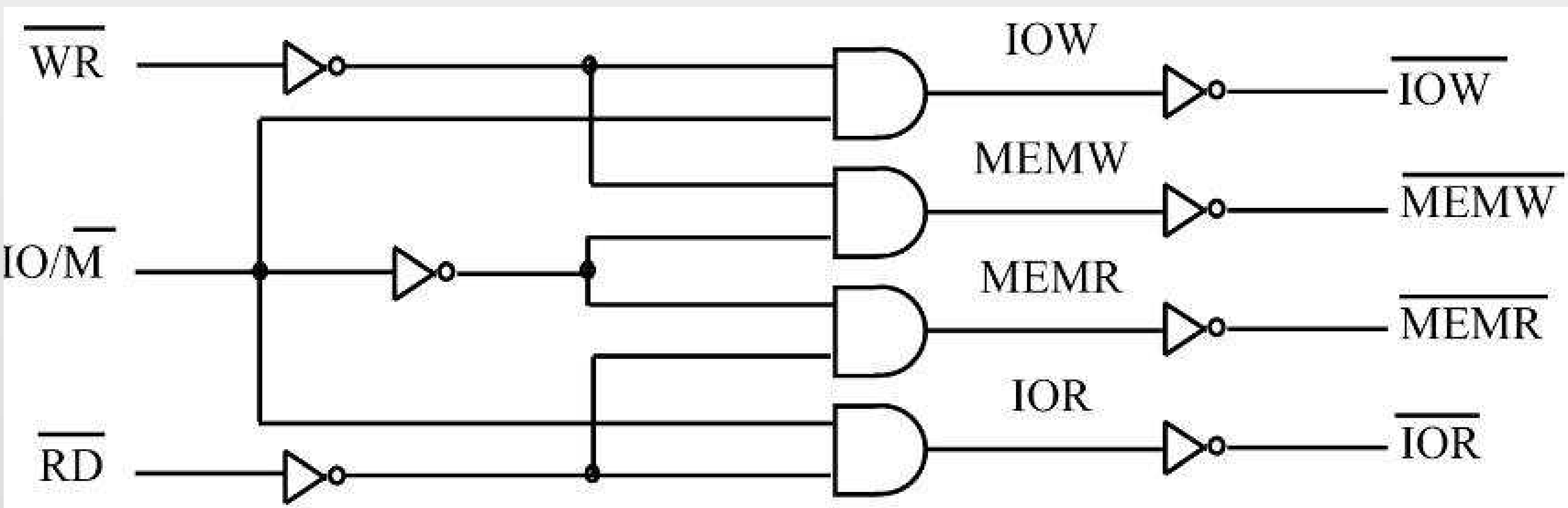


Fig. 9-4 Control signal generation

8088 MICROPROCESSOR
control bus

- 8088 provides three pins for control signals:
  - RD, WR, and IO/$\overline{\text{M}}$.
    - RD & WR pins are both *active-low*.
    - IO/$\overline{\text{M}}$ is *low* for memory, *high* for I/O devices.

Four control signals are generated:

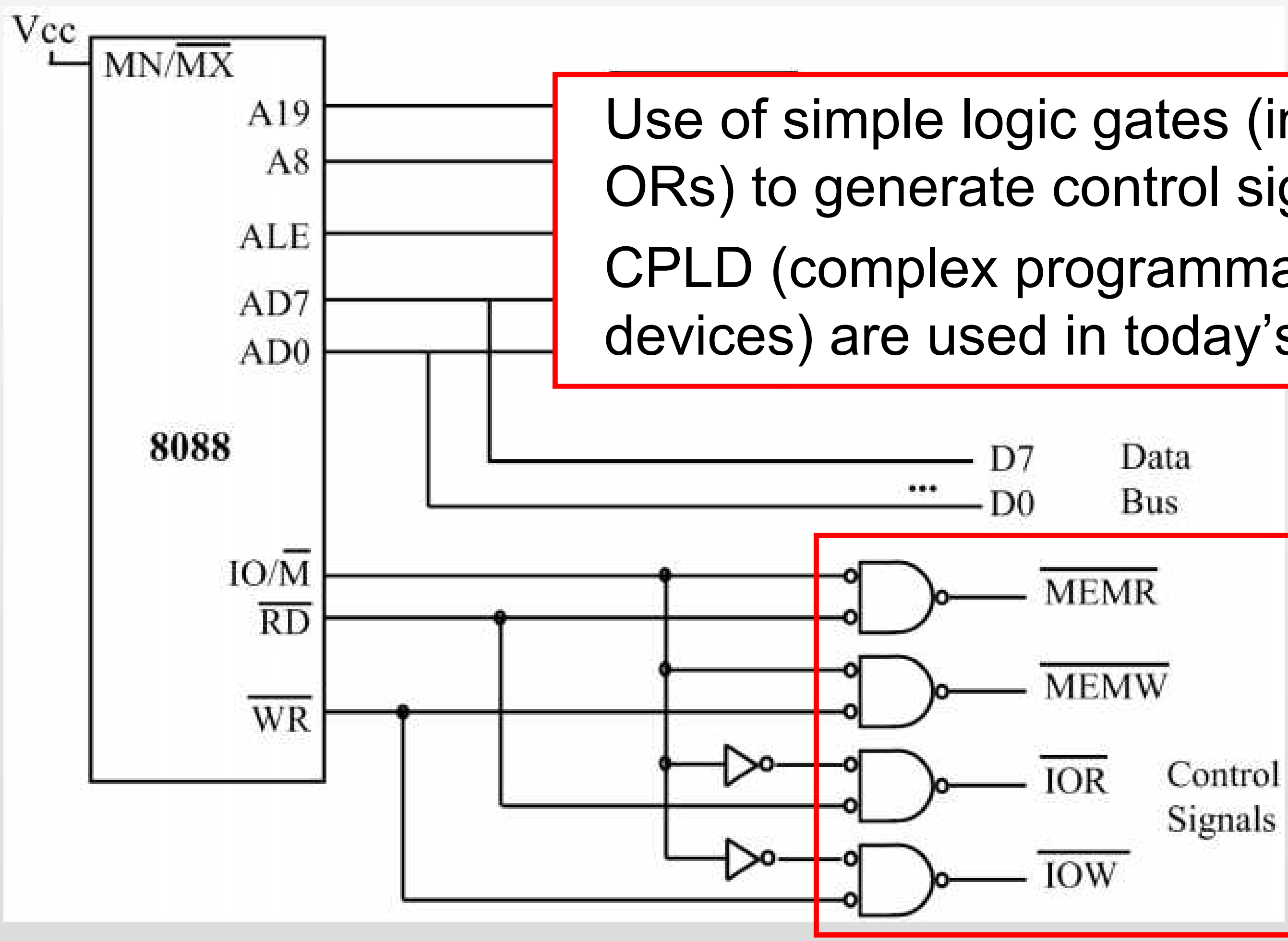
$\overline{\textbf{IOR}}$; **$\overline{\textbf{IOW}}$**;
$\overline{\textbf{MEMR}}$; **$\overline{\textbf{MEMW}}$**.

All of these signals must be active-low.

Table 9-1: Control Signal Generation

RD	WR	IO/M	Signal
0	1	0	$\overline{\text{MEMR}}$
1	0	0	$\overline{\text{MEMW}}$
0	1	1	$\overline{\text{IOR}}$
1	0	1	$\overline{\text{IOW}}$
0	0	x	Never happens

8088 MICROPROCESSOR control bus



Use of simple logic gates (inverters and ORs) to generate control signals.

CPLD (complex programmable logic devices) are used in today's PC chipsets.

Fig. 9-5 Address,Data,and Control Buses in 8088-based System

8088 MICROPROCESSOR
bus timing of the 8088

- 8088 uses 4 clocks for memory & I/O bus activities.
  - In read timing, **ALE** latches the address in the first clock cycle.
  - In the second and third cycles, the read signal is provided.
  - By the end of the fourth, data must be at the CPU pins.
  - The entire read or write cycle time is only 4 clock cycles.

If reading/writing takes more than 4 clocks, wait states (WS) can be requested from the CPU.

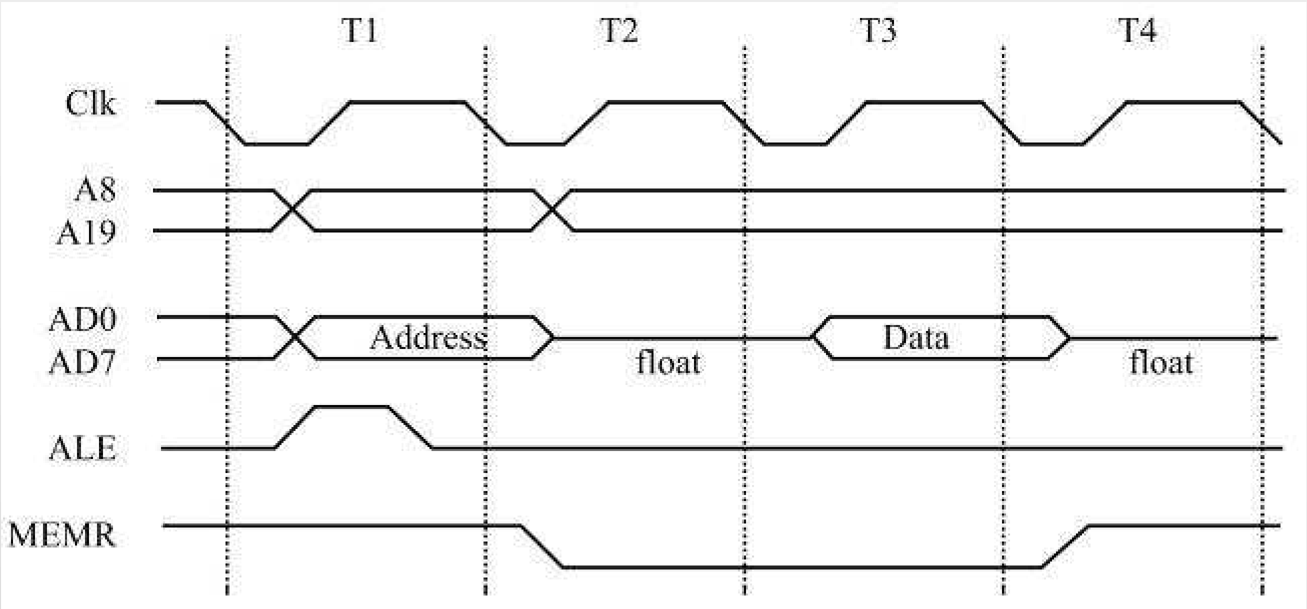


Fig. 9-6 ALE Timing

8088 MICROPROCESSOR
other pins

- Pins 24–32 have different functions depending on whether 8088 is in minimum or maximum mode.
  - In maximum mode, 8088 needs supporting chips to generate the control signals.

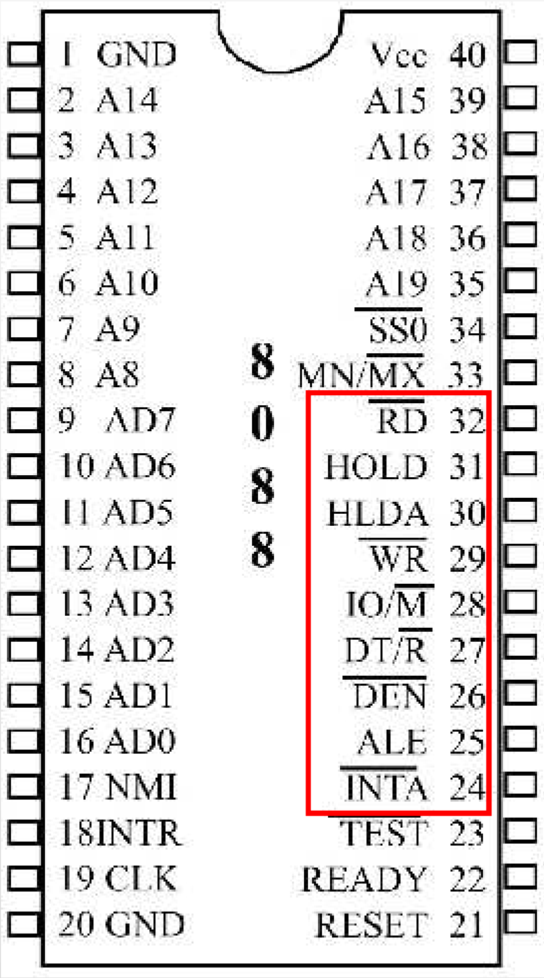


Fig. 9-1a 8088 in minimum mode

8088 MICROPROCESSOR other pins

Functions of 8088 pins 24–32 in minimum mode.

Table 9-2: Pins 24–32 in Minimum Mode

Pin	Name and Function
24	INTA (interrupt acknowledge) Active-low output signal. Informs interrupt controller that an INTR has occurred and that the vector number is available on the lower 8 lines of the data bus.
25	ALE (address latch enable) Active-high output signal. Indicates that a valid address is available on the external address bus.
26	DEN (data enable) Active-low output signal. Enables the 74LS245. This allows isolation of the CPU from the system bus.
27	DT/R (data transmit/receive) Active-low output signal used to control the direction of data flow through the 74LS245 transceiver.
28	IO/M (input-output or memory) Indicates whether the address bus is accessing memory or an I/O device. In the 8088, it is low when accessing memory and high when accessing I/O. This pin is used along with RD and WR pins to generate the four control signals MEMR, MEMW, IOR, and IOW.

8088 MICROPROCESSOR other pins

Functions of 8088 pins 24–32 in minimum mode.

Table 9-2: Pins 24–32 in Minimum Mode

Pin	Name and Function
29	WR (write) Active-low output signal. Indicates that the data on the data bus is being written to memory or an I/O device. Used along with signal IO/M (pin 28) to generate the MEMW and IOW control signals for write operations.
30	HLDA (hold acknowledge) Active-high output signal. After input on HOLD, the CPU responds with HLDA to signal that the DMA controller can use the buses.
31	HOLD (hold) Active-high input from the DMA controller that indicates that the device is requesting access to memory and I/O space and that the CPU should release control of the local buses.
32	RD (Read) Active-low output signal. Indicates that the data is being read (brought in) from memory or I/O to the CPU. Used along with signal IO/M (pin 28) to generate MEMR and IOR control signals for read operations.

8088 MICROPROCESSOR
other pins

- **MN/MX** (minimum/maximum) - minimum mode is selected by connecting MN/MX (pin number 33) directly to +5 V.
  - Maximum mode is selected by grounding this pin.
- **NMI** (nonmaskable interrupt) - an edge-triggered (*low* to *high*) input signal to the processor that will make the microprocessor jump to the interrupt vector table after it finishes the current instruction.
  - Cannot be masked by software.
- **CLOCK** - an input signal, connected to the 8284 clock generator.

8088 MICROPROCESSOR
other pins

- **INTR** (interrupt request) - an *active-high* level-triggered input signal continuously monitored by the microprocessor for an external interrupt.
  - This pin & INTA are connected to the 8259 interrupt controller chip.
- **READY** - an input signal, used to insert a wait state for slower memories and I/O.
  - It inserts wait states when it is *low*.
- **TEST** - in maximum mode, an input from the 8087 math coprocessor to coordinate communications.
  - Not used In minimum mode.

8088 MICROPROCESSOR
other pins

- **RESET** - terminates present activities of the processor when a *high* is applied to the **RESET** input pin.

A presence of *high* will force the microprocessor to stop all activity and set the major registers to the values shown at right.

Table 9-3: IP and Segment Register Contents after Reset

Register	Contents
CS	FFFF
IP	0000
DS	0000
SS	0000
ES	0000

8088 SUPPORTING CHIPS

- In maximum mode, 8088 requires the use of the 8288 to generate some of the control signals.
  - 8288 is a 20-pin chip specially designed to provide all the control signals when the 8088 is in maximum mode.
  - Modern microprocessors such as the Pentium® have 8284 and 8288 incorporated into a single chip.

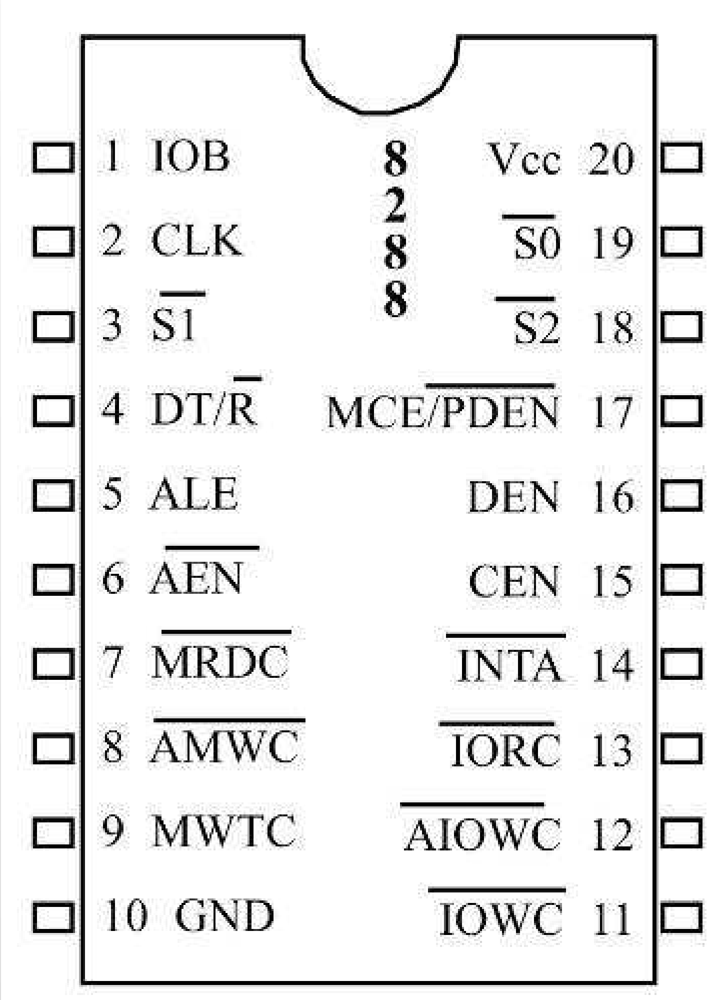


Fig. 9-8 8288 Bus Controller

8088 SUPPORTING CHIPS

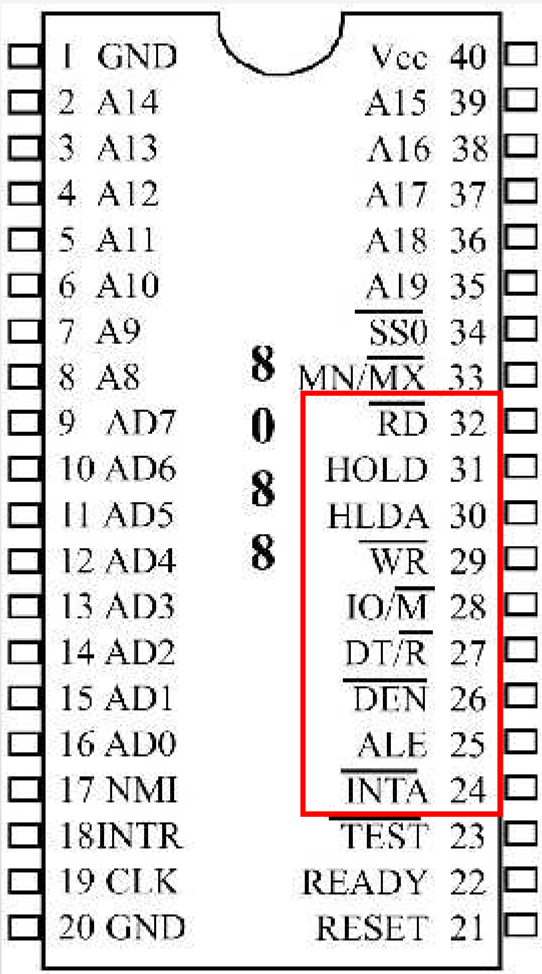


Fig. 9-1a 8088 in **minimum** mode

Comparing Fig. 9-1, 8088 in **minimum** mode, with Fig. 9-7, 8088 in **maximum** mode, shows that pins 24–32 have different functions.

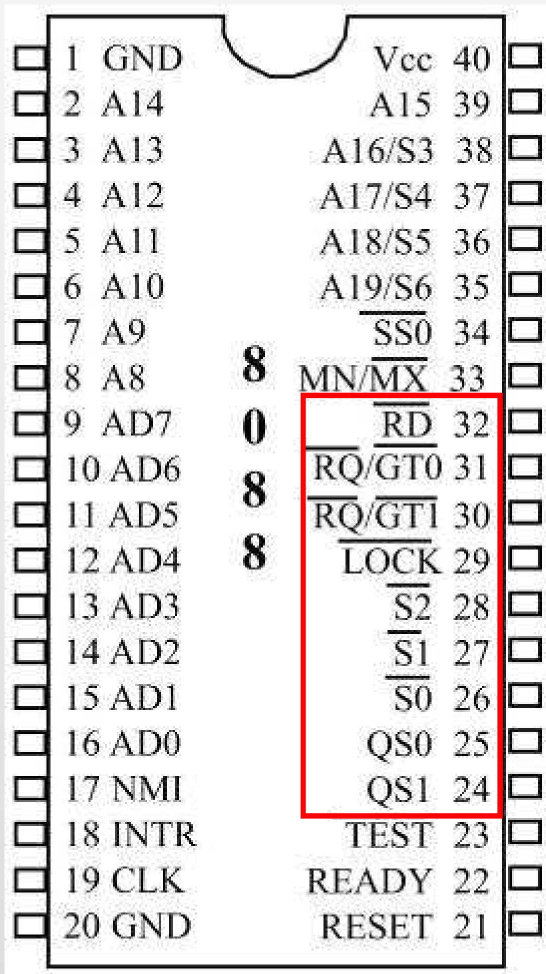


Fig. 9-7a 8088 in **maximum** mode

8088 SUPPORTING CHIPS
8288 bus controller input signals

- $\overline{\textbf{S0}}$, $\overline{\textbf{S1}}$, $\overline{\textbf{S2}}$ (status input) - input to these pins comes from the 8088.
  - Depending upon the input from the CPU, the 8288 will provide one of the commands or control signals shown:

Table 9-4: Status Pins of the 8288 and Their Meaning

S2	S1	S0	Processor State	8288 Command
0	0	0	Interrupt acknowledge	$\overline{\text{INTA}}$
0	0	1	Read input/output port	$\overline{\text{IORC}}$
0	1	0	Write input/output port	$\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$
0	1	1	Halt	None
1	0	0	Code access	$\overline{\text{MRDC}}$
1	0	1	Read memory	$\overline{\text{MRDC}}$
1	1	0	Write memory	$\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$
1	1	1	Passive	None

8088 SUPPORTING CHIPS
8288 bus controller input signals

- **CLK** (clock) - input from the 8284 clock generator, providing the clock pulse to the 8288 to synchronize all command and control signals with the CPU.
- $\overline{\textbf{AEN}}$ (address enable) - *active-low* signal, activates 8288 command output at least 115 ns after its activation.
- **CEN** (command enable) - *active-high* signal is used to activate/enable the command signals and **DEN**.
- **IOB** (input/output bus mode) - *active-high* signal makes the 8288 operate in input/output bus mode rather than in system bus mode.

8088 SUPPORTING CHIPS
8288 bus controller output signals

- $\overline{\textbf{MRDC}}$ (memory read command) - *active-low* and provides the $\overline{\textbf{MEMR}}$ (memory read) control signal.
  - Activates the selected device or memory to release its data to the data bus.
- $\overline{\textbf{MWTC}}$ (memory write command) and $\overline{\textbf{AMWC}}$ (advanced memory write) - two *active-low* signals used to tell memory to record data present on the data bus.
- $\overline{\textbf{IORC}}$ (I/O read command) - an *active-low* signal that tells the I/O device to release its data to the data bus. (called $\overline{\textbf{IOR}}$ (I/O read) control signal on the PC)

8088 SUPPORTING CHIPS
8288 bus controller output signals

- $\overline{\textbf{IOWC}}$ (I/O write command) and $\overline{\textbf{AIOWC}}$ (advanced I/O write command) - *active-low* signals used to tell the I/O device to pick up the data on the data bus.
- $\overline{\textbf{INTA}}$ (interrupt acknowledge) - an *active-low* signal will inform the interrupting device that its interrupt has been acknowledged and will provide the vector address to the data bus.
  - In the IBM PC, connected to **INTA** of the 8259.

8088 SUPPORTING CHIPS
8288 bus controller output signals

- **DT/$\overline{\text{R}}$** (data transmit/receive) - used to control the direction of data in and out of the 8088.
  - In the IBM PC, it is connected to DIR of the 74LS245.
    - When the 8088 is writing data, this signal is *high* & allows data to go from the A to B side of 74LS245 & released to the bus.
    - When the CPU is reading data, this signal is *low*, allowing data in from the B to the A side of the 74LS245, so it can be received by the CPU.
- **DEN** (data enable) - *active-high* signal will make the data bus either a local or system data bus.
  - In the PC it is used with a signal from the 8259 to activate G of the 74LS245 transceiver.

8088 SUPPORTING CHIPS
8288 bus controller output signals

- **MCE/PDEN** (master cascade enable/peripheral data enable) - used with 8259 interrupt controller in master configuration.
  - In the PC the 8259 is used as a slave, this pin is ignored.
- **ALE** (address latch enable) - an *active-high* signal used to activate address latches.
  - 8088 multiplexes address & data through AD0–AD7 in order to save pins.
    - In the PC, ALE is connected to the G input of the 74LS373, making address demultiplexing possible.

8088 SUPPORTING CHIPS
8284 clock generator

- 8284 provides clock & timing for the 8088-based system.
  - Used in both minimum and maximum modes.
  - Shown is the 8284A, 18-pin chip especially designed for the 8088/86 microprocessor.
  - It provides synchronization, clock, and the READY signal for the insertion of wait states into the CPU bus cycle.

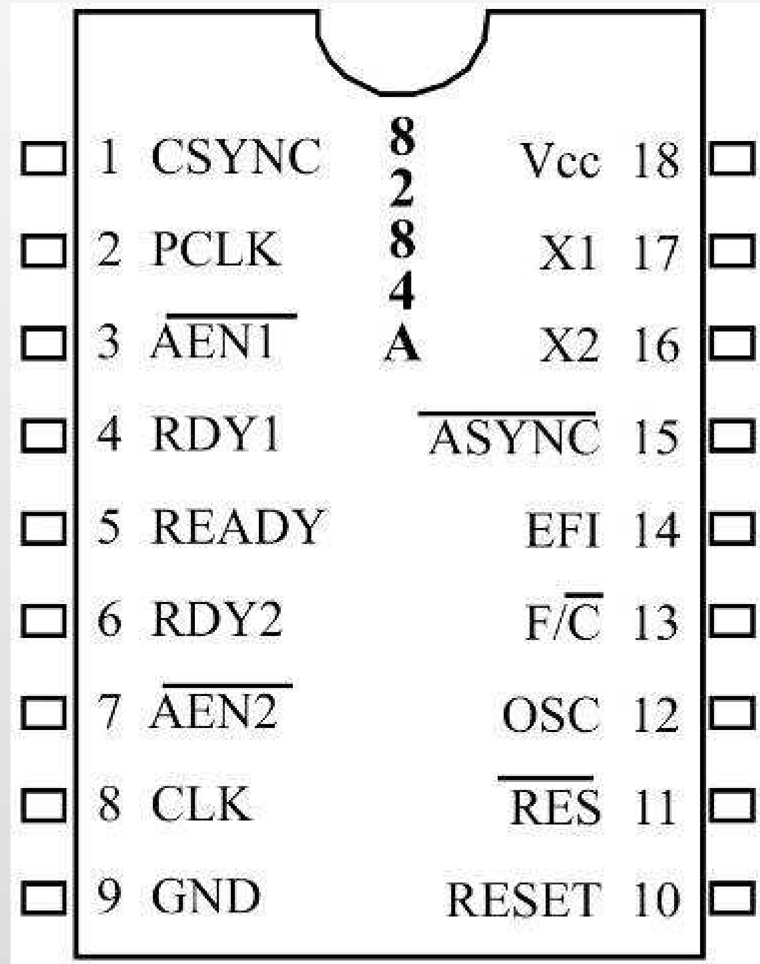


Fig. 9-9 8294A Chip

8088 SUPPORTING CHIPS
8284 clock generator input pins

- $\overline{\textbf{RES}}$ (reset in) - an input *active-low* signal to generate RESET.
  - When the PC power switch is turned on, assuming the power supply is good, a *low* signal is provided to this pin and 8284 in turn will activate the RESET pin, forcing the 8088 to reset, called a *cold boot*.
- **X1** and **X2** (crystal in) - the pins to which a crystal is attached.
  - Crystal frequency must be 3 times the desired frequency for the microprocessor; maximum for t8284A is 24 MHz.
    - The IBM PC is connected to a crystal of 14.31818 MHz.

8088 SUPPORTING CHIPS
8284 clock generator input pins

- **F/$\overline{\text{C}}$** (frequency/clock) - provides an option for the way the clock is generated.
  - If connected to *low*, the clock is generated by the 8284 with the help of a crystal oscillator.
  - If it is connected to *high*, it expects clocks at the **EFI** pin.
- **EFI** (external frequency in) - external frequency is connected to this pin if **F/$\overline{\text{C}}$** is connected to *high*.
  - Not connected in the PC since a crystal is used.
- **CSYNC** (clock synchronization) - *active-high* signal used to allow several 8284 chips to be connected together and synchronized.

8088 SUPPORTING CHIPS
8284 clock generator input pins

- **RDY1** is *active-high* and $\overline{\textbf{AEN1}}$(address enable) is *active-low*.
  - Used together to provide a ready signal to the processor, which will insert a WAIT state to the CPU read/write cycle.
  - **RDY1** is connected to **DMAWAIT** .
  - $\overline{\textbf{AEN1}}$ is connected to **RDY/WAIT**.
    - Allows a wait state to be inserted by either the CPU or DMA.

- **RDY2** and $\overline{\textbf{AEN2}}$ **-** function exactly like **RDY1** and $\overline{\textbf{AEN1}}$, but are designed to allow for multiprocessing.

8088 SUPPORTING CHIPS
8284 clock generator input pins

- **ASYNC -** called ready synchronization select.
  - An *active-low* is used for devices not able to adhere to the very strict **RDY** setup time requirement.
    - In the PC, connected to *low*, making the timing design of the system easier with slower logic gates.

8088 SUPPORTING CHIPS
8284 clock generator output signals

- **RESET** - *active-high* signal that provides a RESET signal to the 8088.
- **OSC** (oscillator) - provides a clock frequency equal to the crystal oscillator and is TTL compatible.
- **CLK** (clock) - an output clock frequency equal to one-third of the crystal oscillator, or **EFI** input frequency, with a duty cycle of 33%.
- **PCLK** (peripheral clock) - one-half of **CLK** (or one-sixth of the crystal) with a duty cycle of 50%, and is TTL compatible.

8088 SUPPORTING CHIPS
8284 clock generator output signals

- **READY** - connected to READY of the CPU.
  - In the PC it is used to signal the 8088 that the CPU needs to insert a wait state due to the slowness of the devices that the CPU is trying to contact.

8-BIT SECTION OF ISA BUS
bus history

- The original 1981 IBM PC 8088 used an 8-bit data bus, which led to the 8-bit section of the ISA bus.
  - In 1984, when the IBM PC/AT used the 80286, the data bus was expanded to 16 bits.
    - The 8-bit data bus is seen as a subsection of the 16-bit ISA bus.
- The 8-bit data bus was referred to as the IBM PC/XT (extended technology) bus, to differentiate it from the IBM PC AT (advanced technology).
  - The AT bus became known as the ISA (Industry Standard Architecture) bus since, “PC AT” was copyrighted by IBM.

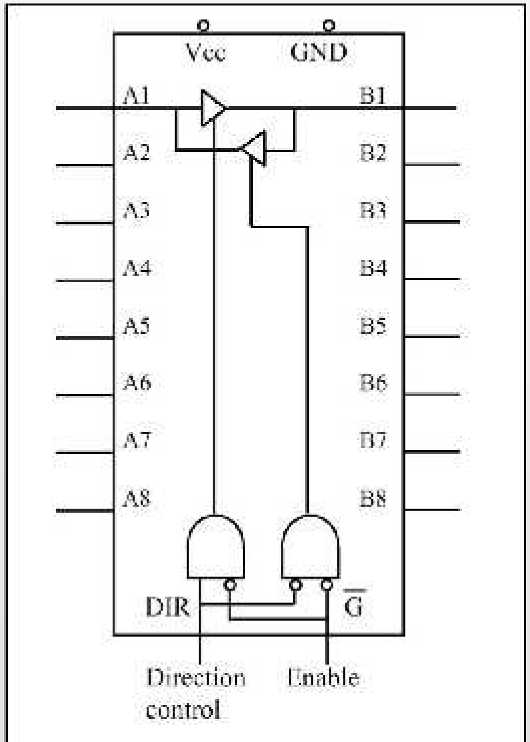
8-BIT SECTION OF ISA BUS
local bus vs. system bus

- The system bus provides necessary signals to all chips (RAM/ROM/peripheral) on the motherboard.
  - Also to the expansion slot for any plug-in expansion card.
- The local bus is connected directly to the CPU, and any communication with the CPU must go through the local bus.
  - A bridge between the local & system bus isolates them.
- The system bus is sometimes referred to as a *global bus*.

8-BIT SECTION OF ISA BUS
local bus vs. system bus

This diagram appears on page 238 of your textbook.

- Tri-state buffers isolate the local bus & system bus.
  - 74LS245 is a widely used chip for the data bus buffer since it is bidirectional.



Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Fig. 9-10 74SL245 Bidirectional Buffer

8-BIT SECTION OF ISA BUS
local bus vs. system bus

An overview of the 8088 & supporting chips in the original PC.

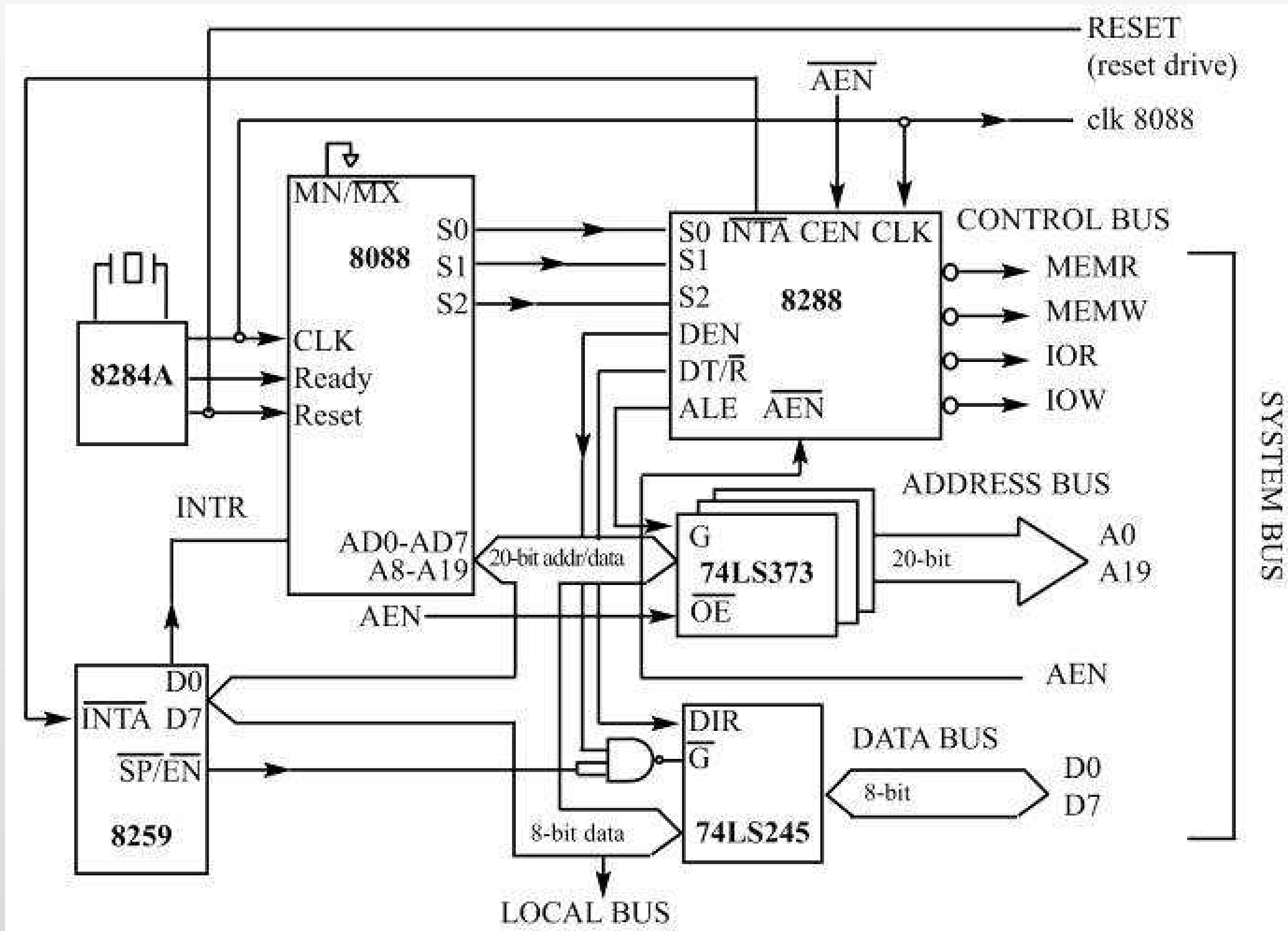


Fig. 9-11 8088 Connections and Buses in the PC/XT

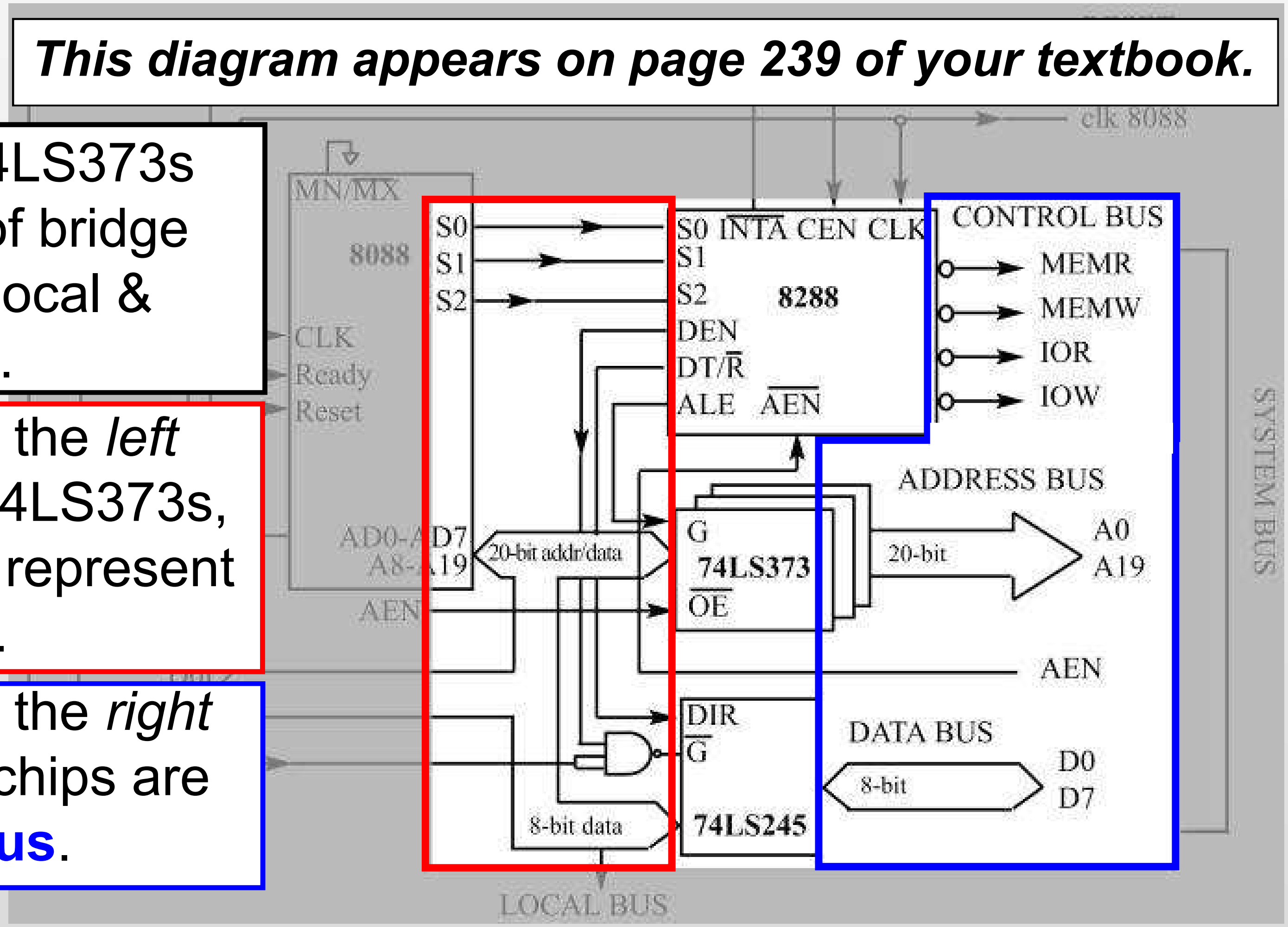
8-BIT SECTION OF ISA BUS
local bus vs. system bus

This diagram appears on page 239 of your textbook.

74LS245 & 74LS373s play the role of bridge to isolate the local & system buses.

Everything on the *left* of the 8288, 74LS373s, and 74LS245 represent the **local bus**.

Everything on the *right* side of those chips are the **system bus**.



8-BIT SECTION OF ISA BUS
address bus - 74LS373 functions

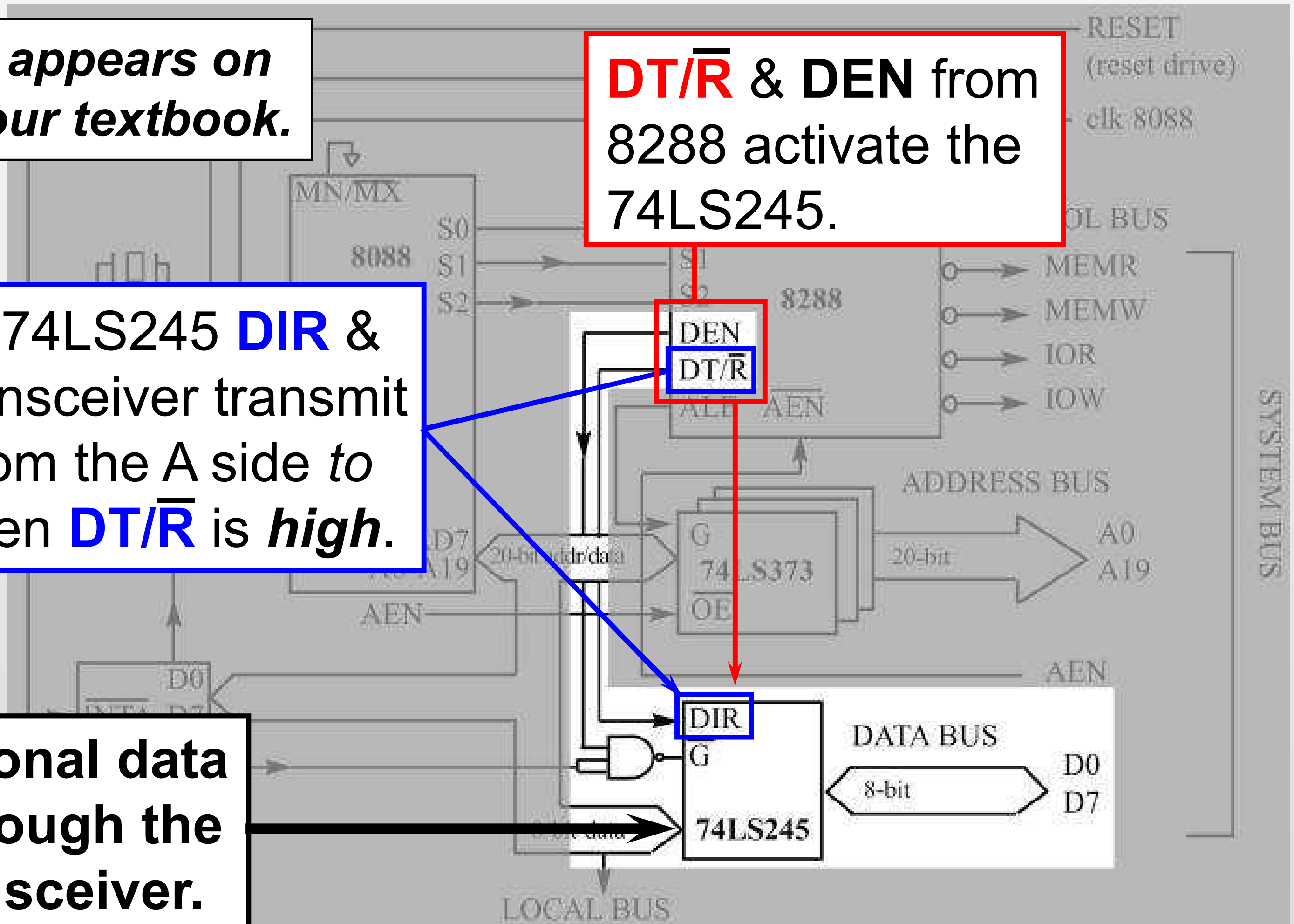
- The 74LS373 chips latch addresses from the 8088 and provide stable addresses to the computer.
  - Activated by control signals **AEN** & **ALE**.
    - When **AEN** is *low*, 8088 provides address buses to the system.
    - The 8288 **ALE** (connected to G) enables 74LS373 to latch addresses from the CPU, providing a 20-line stable address to memory, peripherals, and expansion slots.
  - Demultiplexing addresses A0–A7 is performed by the 74LS373 connected to pins AD0–AD7 of the CPU.
    - The CPU A8–A15 is connected to the second 74LS373.
    - A16–A19 is connected to the third one, and half of the third 74LS373 is unused.

8-BIT SECTION OF ISA BUS
address bus - 74LS373 functions

- The 74LS373 chips also isolate the system address buses from local address buses.
  - The system buses must be allowed to be used by the DMA or any other board through the expansion slot without disturbing the CPU.
    - Achieved by the 74LS373s through **AEN**.

8-BIT SECTION OF ISA BUS
data bus

This diagram appears on page 239 of your textbook.



DT/R̄ & **DEN** from 8288 activate the 74LS245.

DT/R̄ goes to 74LS245 **DIR** & makes the transceiver transmit information from the A side *to* the B side when **DT/R̄** is ***high***.

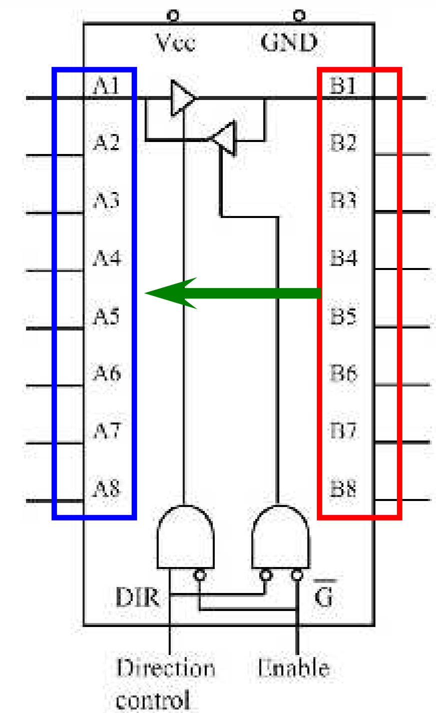
The bidirectional data bus goes through the 74LS245 transceiver.

8-BIT SECTION OF ISA BUS
data bus

This diagram appears on page 238 of your textbook.

When **$DT/\overline{R}$** makes **DIR *low***, the information transfers *from* the **B** *to* the **A** side, taking information from the system data bus and bringing it to the 8088.

The bidirectional data bus goes through the 74LS245 transceiver.



Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Fig. 9-10 74SL245 Bidirectional Buffer

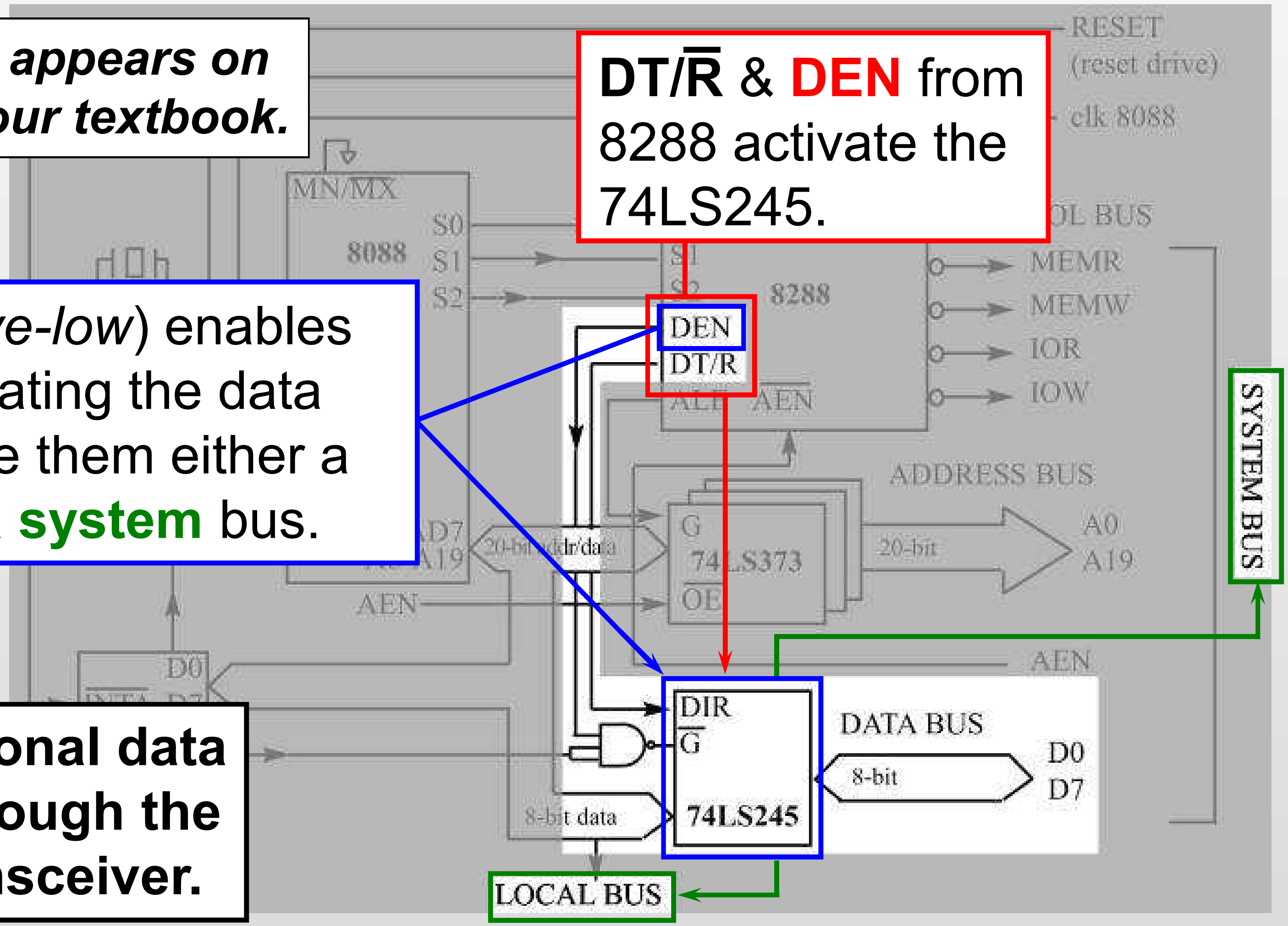
8-BIT SECTION OF ISA BUS
data bus

This diagram appears on page 239 of your textbook.

DT/$\overline{\text{R}}$ & **DEN** from 8288 activate the 74LS245.

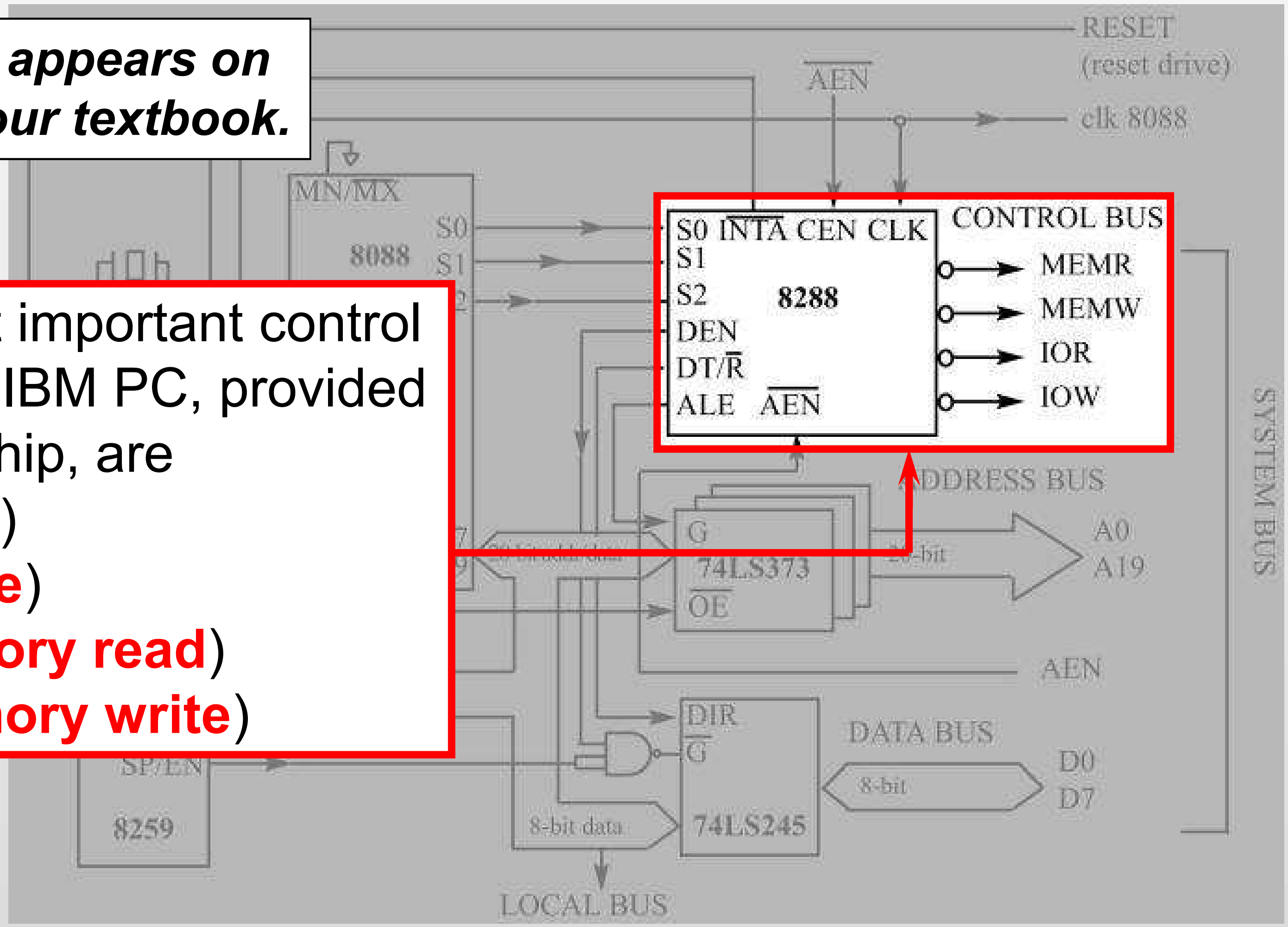
DEN (an *active-low*) enables 74LS245, isolating the data buses to make them either a **local** bus or a **system** bus.

The bidirectional data bus goes through the 74LS245 transceiver.



8-BIT SECTION OF ISA BUS control bus

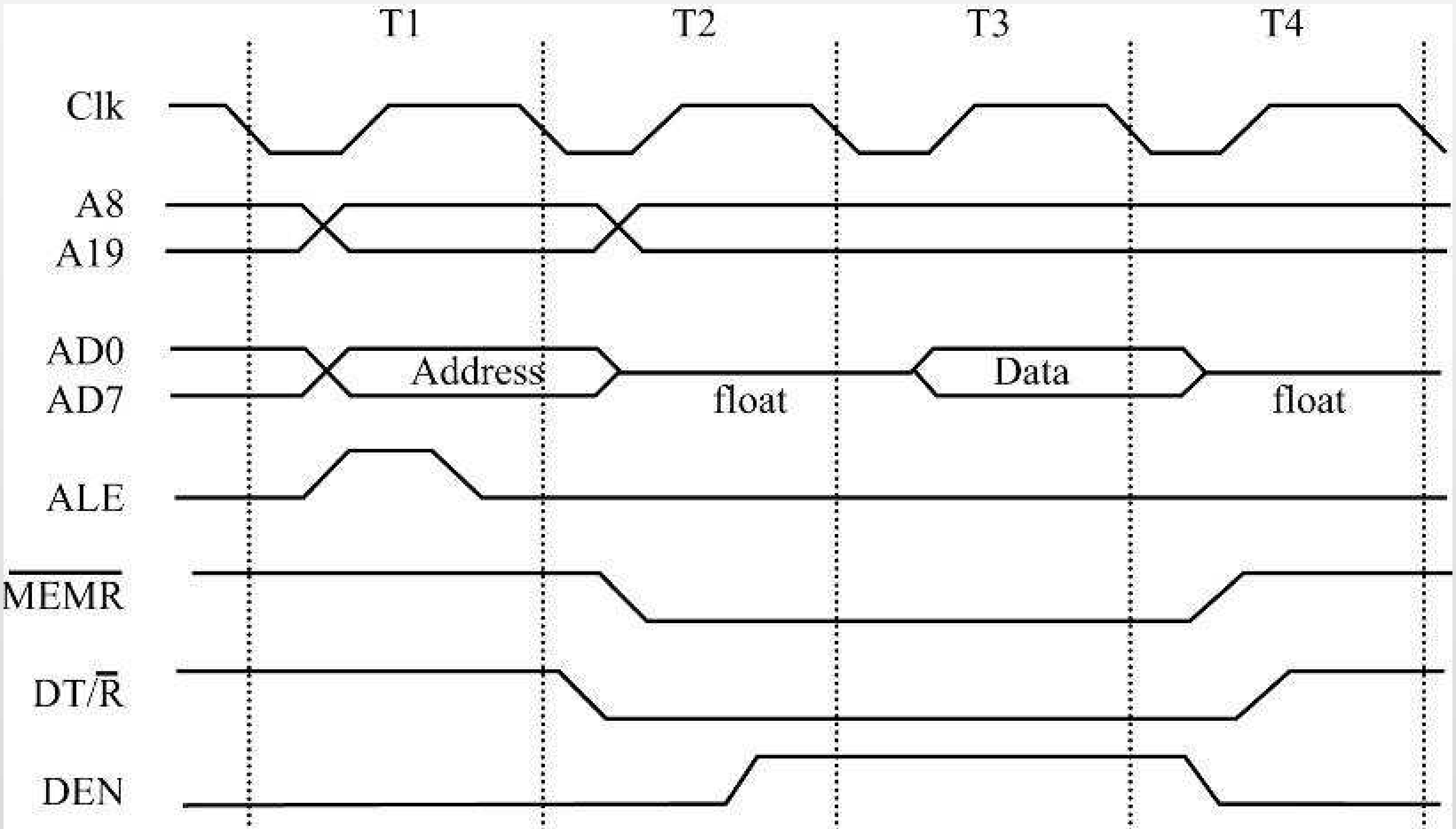
This diagram appears on page 239 of your textbook.



The four most important control signals of the IBM PC, provided by the 8288 chip, are
IOR (**I/O read**)
IOW (**I/O write**)
MEMR (**memory read**)
MEMW (**memory write**)

8-BIT SECTION OF ISA BUS
control bus

The timing for control bus activity.



8-BIT SECTION OF ISA BUS
one bus, two masters

- 8088 is unacceptably slow for transferring large numbers of bytes of data, as in hard disk transfers.
  - The 8237 chip is used for large data transfers.
- The 8237 must have access to all three buses.
  - *Bus arbitration*, achieved by the **AEN** (address enable) generation circuitry allows either the 8088 processor or the 8237 DMA to bus gain control.

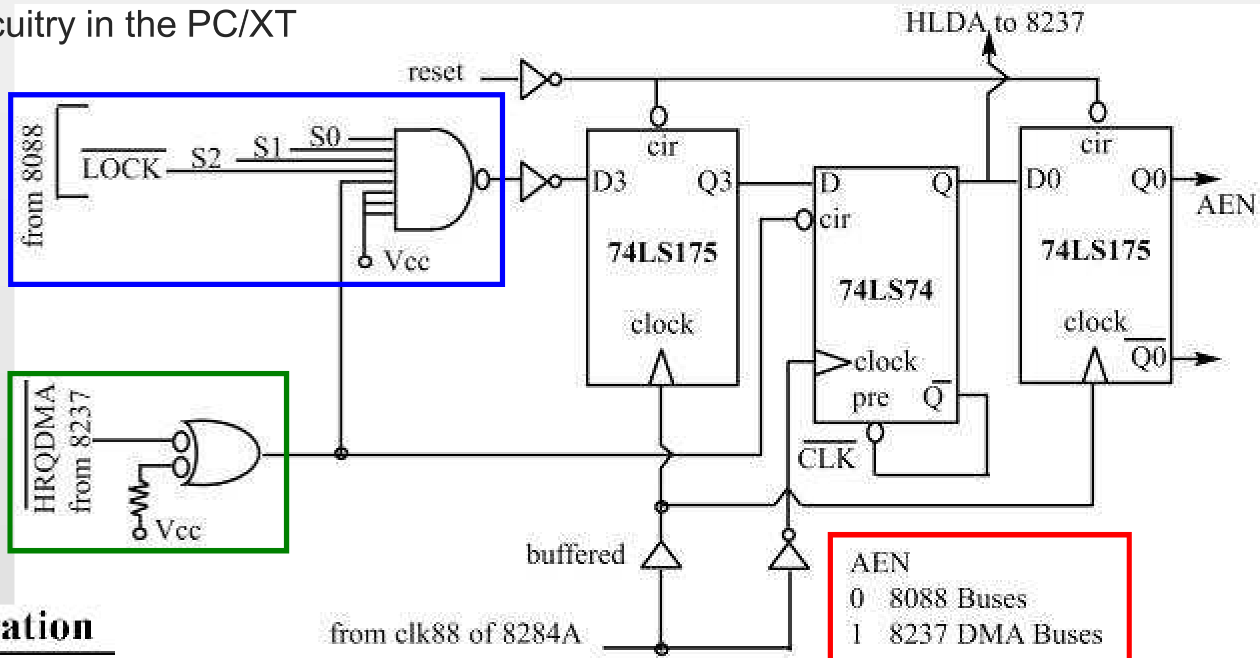
Table 9-5: AEN Bus Arbitration

AEN	Bus Control
0	Buses controlled by CPU
1	Buses controlled by DMA

8-BIT SECTION OF ISA BUS
AEN signal generation

- On power-up, the 8088 is in control of all the buses.
  - It maintains control while fetching & executing instructions.

Fig. 9-13 AEN Generation Circuitry in the PC/XT



Q is either ***low*** or ***high***, based on signal status.

Either the **CPU** or the **DMA** can access the buses.

Table 9-5: AEN Bus Arbitration

AEN	Bus Control
0	Buses controlled by CPU
1	Buses controlled by DMA

AEN is the output signal of the D flip-flop.

8-BIT SECTION OF ISA BUS
control of the bus by DMA

- When DMA receives a request for service, it notifies the CPU that it needs to use the system buses by putting a *low* on **HRQDMA**.
  - This provides a *high* on D3 output of the 74LS175
    - Assuming the current memory cycle is finished and **LOCK** is not activated.
- In the following clock, **HLDA** (hold acknowledge) is provided to the DMA and **AEN** becomes *high*.
  - Giving control over the buses to the DMA.

8-BIT SECTION OF ISA BUS
bus boosting

- It is common to combine the functions of bus isolation and bus boosting into a single chip. *Why?*
  - When a pulse leaves an IC chip it can lose strength, depending on distance to the receiving IC chip.
  - The more pins a signal is connected to, the stronger the signal must be to drive them all.
  - Every pin connected to a signal has input capacitance, which are in parallel, making one big capacitor load.
  - Signals provided by 8088 need boosting as it is a CMOS chip, with a much lower driving capability than TTL chips.
- 74LS373 boosts the 8088 addresses & 74LS245 is used for both data bus booster & data bus isolation.

8-BIT SECTION OF ISA BUS
8-bit section of the ISA bus

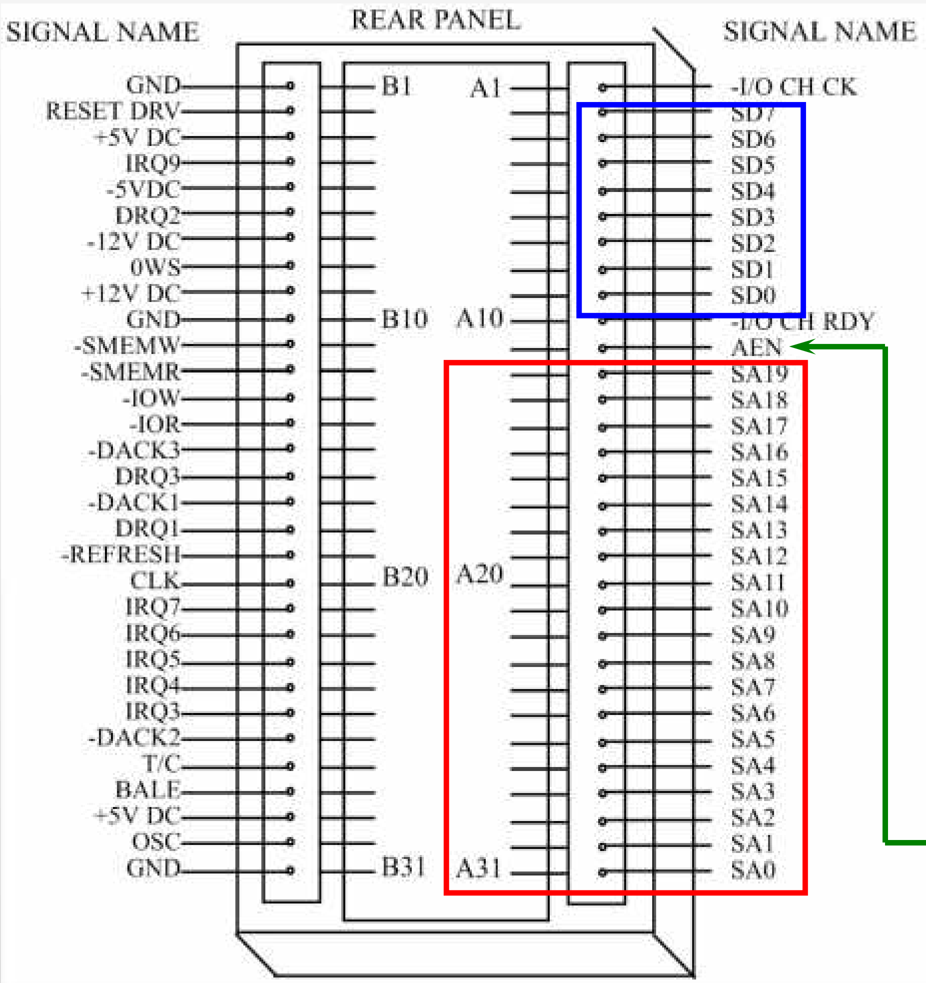


Fig. 9-14 ISA Bus Slot Signals Detail (8-bit section)

- The 80286 16-bit bus has come to be known as the ISA bus.
  - The original 8-bit 8088 bus is a subset, used in many peripheral boards.
- Note addresses **A0–A19** and data signals **D0–D7** are on the A side of the expansion slot.
- On the A side, also note the **AEN** pin.

8-BIT SECTION OF ISA BUS
8-bit section of the ISA bus

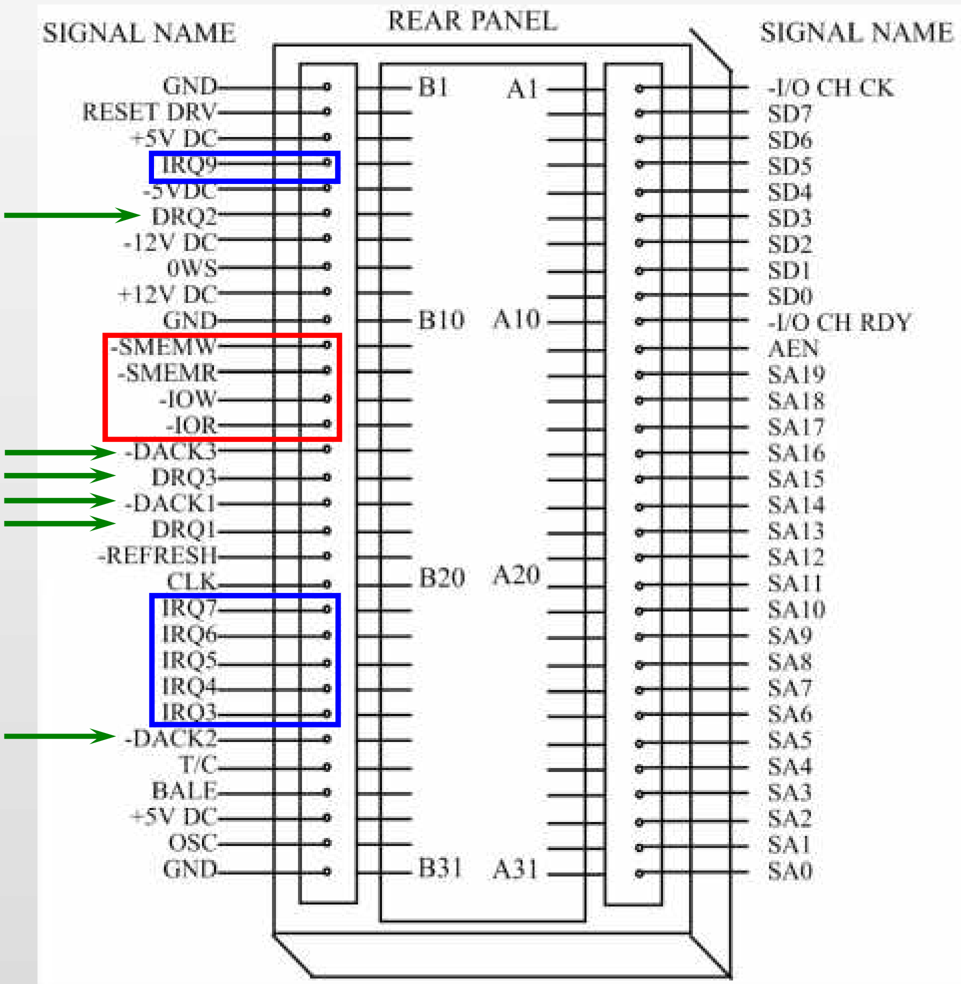


Fig. 9-14 ISA Bus Slot Signals Detail (8-bit section)

- On the B side are found control signals **IOR**, **IOW**, **MEMR**, and **MEMW**.
  - The "–" sign on these and other control signals implies an *active-low* signal.
- Signals associated with interrupts (**IRQ**) are covered in Chapter 14.
- Signals associated with Direct Memory Access (**DREQ** & **DACK**) are covered in Chapter 15.

80286 MICROPROCESSOR

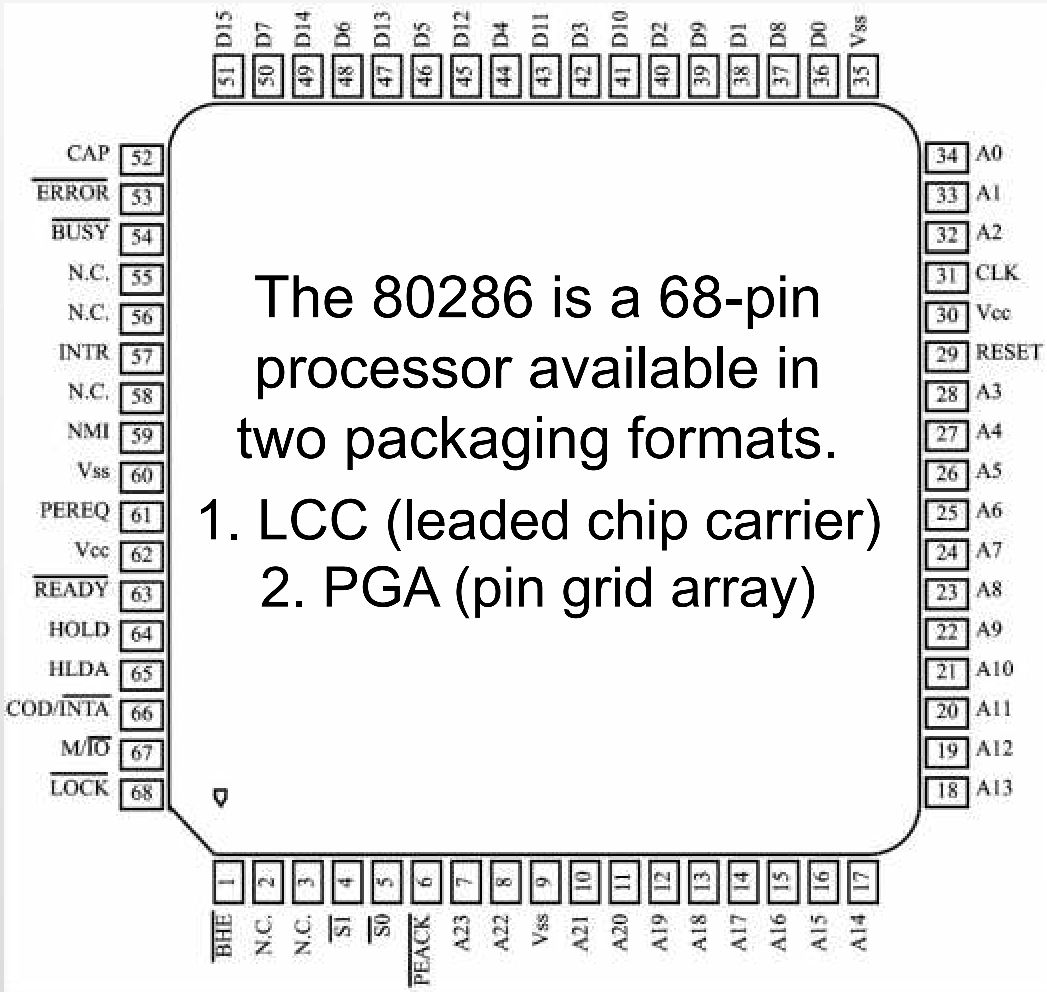


Fig. 9-15 80286 Microprocessor (LCC Packaging)

- 80286 works in real or protected mode.
- Real mode maximum memory access is 1M. (00000H to FFFFFH)
- In protected mode the entire 16M bytes of memory is available. (000000H to FFFFFFH)
  - Use in protected mode requires extremely complex memory management.

80286 MICROPROCESSOR
pin descriptions - address bus

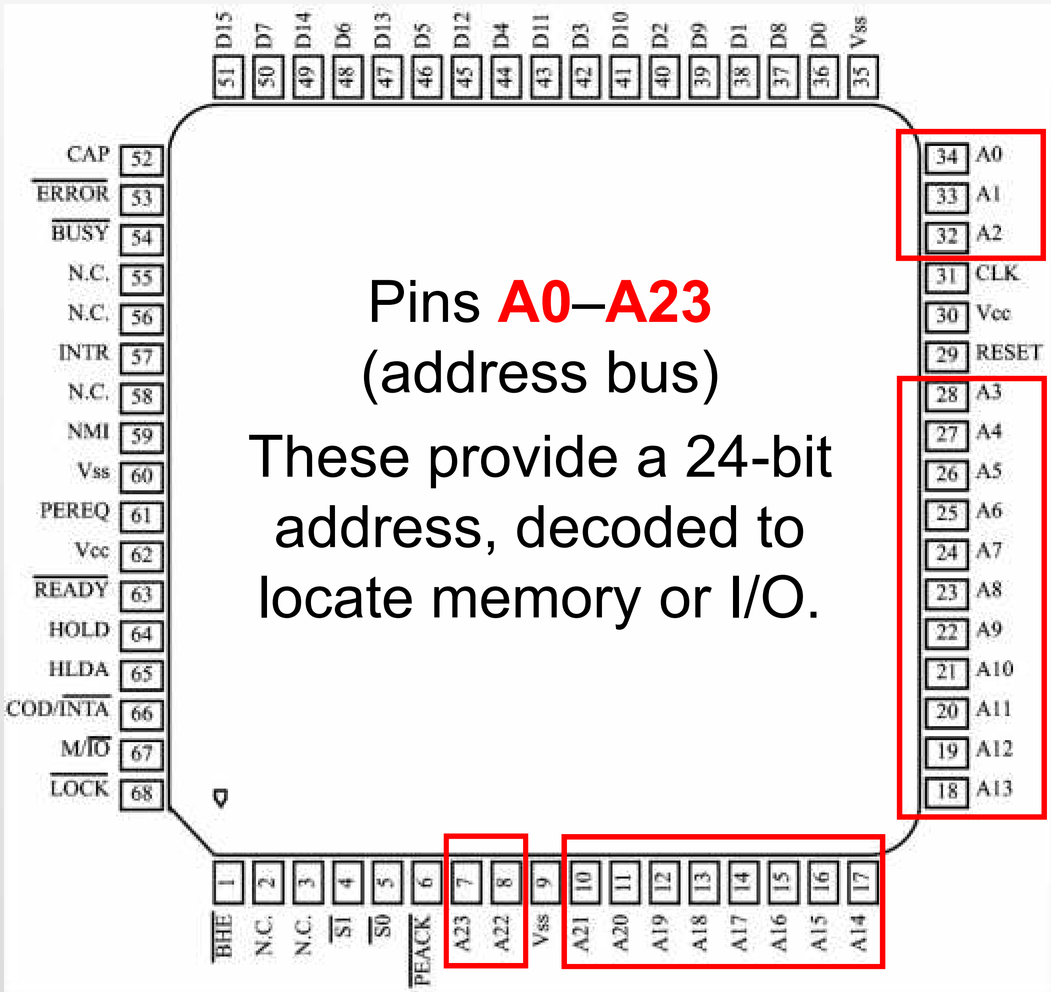


Fig. 9-15 80286 Microprocessor (LCC Packaging)

– Providing a memory address uses all 24 pins (A0–A23), a maximum of 16M.
  - For an I/O address, pins A0–A15 are used.

– If a 16-bit I/O address, A0–A15 provide the address & A16–A23 are *low*.
  - If an 8-bit address, only A0–A7 are used, and A8–A23 are all low.

80286 MICROPROCESSOR pin descriptions - data bus

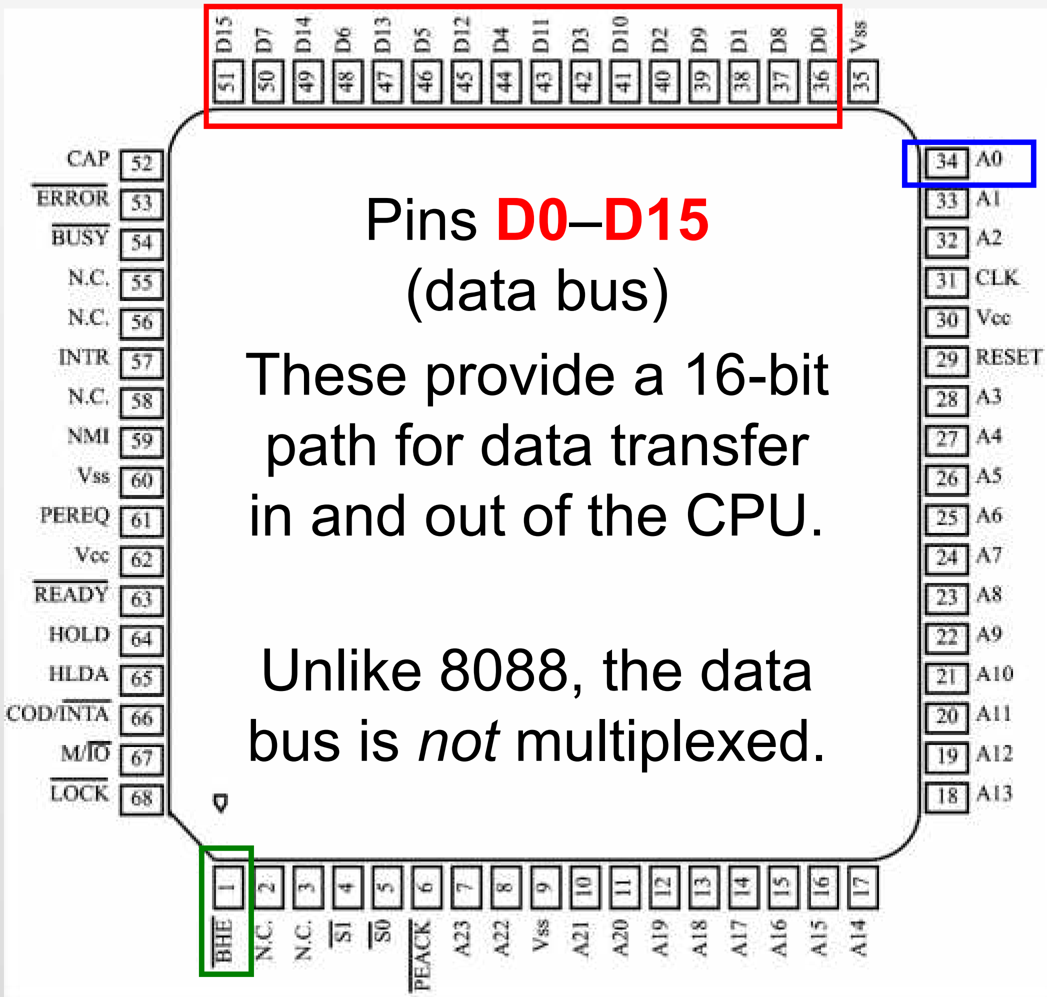


Fig. 9-15 80286 Microprocessor (LCC Packaging)

– Separate address/data pins results in higher pin counts, but saves time by eliminating the address demultiplexer.
  - The 2-byte data path allows the transfer of data on *either* byte or *both* bytes, depending on the operation.

– 80286 coordinates the activity on the data bus using **A0** and **BHE**.

80286 MICROPROCESSOR pin descriptions

- Pin $\overline{\textbf{BHE}}$ (bus high enable) - an *active-low* output signal used to indicate that data is being transferred on D8–D15.
  - $\overline{\textbf{BHE}}$ and **A0** are used to indicate whether the data transfer is on D0–D7, D8–D15, or the entire bus, D0–D15.

Table 9-6: BHE, A0, and Byte Selection in the 80286

BHE	A0	Data Bus Status
0	0	Transferring 16-bit data on D0–D15
0	1	Transferring a byte on the upper half of data bus D8–D15
1	0	Transferring a byte on the lower half of data bus D0–D7
1	1	Reserved (the data bus is idle)

80286 MICROPROCESSOR pin descriptions

- Pin **CLK** (clock) - an input providing the working frequency for the 80286.
  - The processor always works on half of this frequency.
- Pin **M/$\overline{\textbf{IO}}$** (memory I/O select) - an output signal used by the CPU to distinguish between I/O and memory access.
  - When *high*, memory is being accessed.
  - When *low*, I/O is being addressed.

80286 MICROPROCESSOR pin descriptions

- Pin **COD/$\overline{\textbf{INTA}}$** (code/interrupt acknowledge) - an output signal used by the CPU to indicate memory read/write, or an instruction fetch.
  - Also used to distinguish between the action of interrupt acknowledge and I/O cycle.
  - Along with the status signals and M/$\overline{\text{IO}}$, used to define the bus cycle.
- Pins $\overline{\textbf{S1}}$ and $\overline{\textbf{S0}}$ (status signals) - status signals for the bus cycle, output signals used by the CPU with **M/$\overline{\textbf{IO}}$** and **COD/$\overline{\textbf{INTA}}$** to define the type of bus cycle.

80286 MICROPROCESSOR pin descriptions

- Pins **HOLD** & **HLDA** (hold & hold acknowledge) - allow the CPU to control the buses.
  - **HOLD** is an input signal to 80286 and is *active-high*.
    - Used by devices like DMA to request permission to use buses.
  - In response, the CPU activates the output signal **HLDA** by putting a *high* on it to inform the requesting device that it has released the buses for the device's use.
  - DMA has control over the buses as long as **HOLD** is *high*, and in response the CPU keeps **HLDA** *high*.
    - When the DMA brings **HOLD** *low*, the CPU responds by making **HLDA** *low*, and regains control over the buses.

80286 MICROPROCESSOR pin descriptions

- **RESET** pin - an input signal, *active-high*.
  - On a **RESET** *low*-to-*high* transition (for at least 16 clocks), 80286 initializes all registers to predefined values.
  - Status of the following pins should be noted, as they are used in the memory design of the IBM PC/AT:
    - A20 = 1, A21 = 1, A22 = 1, A23 = 1.

Other output pins will have the status shown at right:

Table 9-7: Pin State During Reset

Pin Name	Signal Level at Reset
D0–D15	High impedance
A0–A23	High
$W/\overline{R}$	Low
$M/\overline{IO}$	High

80286 MICROPROCESSOR pin descriptions

- **RESET** pin - an input signal, *active-high*.
  - While **RESET** is *high*, no instruction/bus activity is allowed.
  - On **RESET,** 80286 is forced into real mode, and A20–A23 are set *high*, thus, the first instruction must be at physical address FFFFF0H.

80286 expects a far jump at location FFFFF0H, and when the **JMP** is executed, the 286 puts 0s on pins A20–A23, making it effectively a 1M range real-mode system.

Table 9-8: IP and Segment Registers After RESET

Register	Contents
CS	F000
IP	FFF0
DS	0000
SS	0000
ES	0000

80286 MICROPROCESSOR pin descriptions

- Pin **INTR** (interrupt request) - an input signal into the 80286 requesting suspension of the current program execution.
  - Used for external hardware interrupt expansion along with the 8259 interrupt controller chip.
- Pin **NMI** (nonmaskable interrupt request) - an *active-high* input signal.
  - On activation, 80286 will automatically perform **INT 2**.
    - No **INTA** response since **INT 2** is assigned to it.

80286 MICROPROCESSOR
pin descriptions

- **READY** pin - an active-low input signal used to insert a wait state and prolong the read/write cycle for slow memory and I/O devices.
  - Note the 2-clock cycle time for read.

80286 MICROPROCESSOR pin descriptions

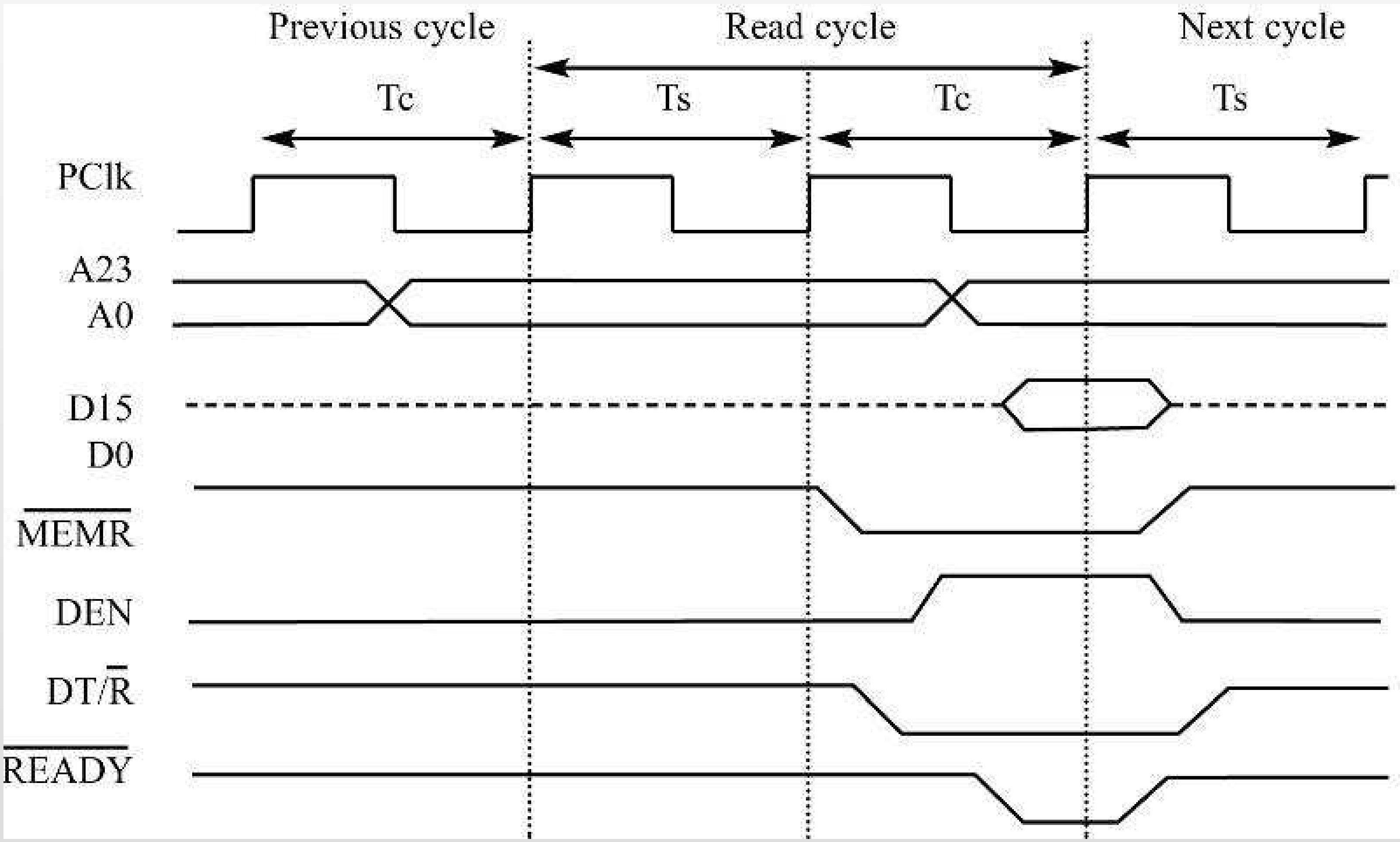


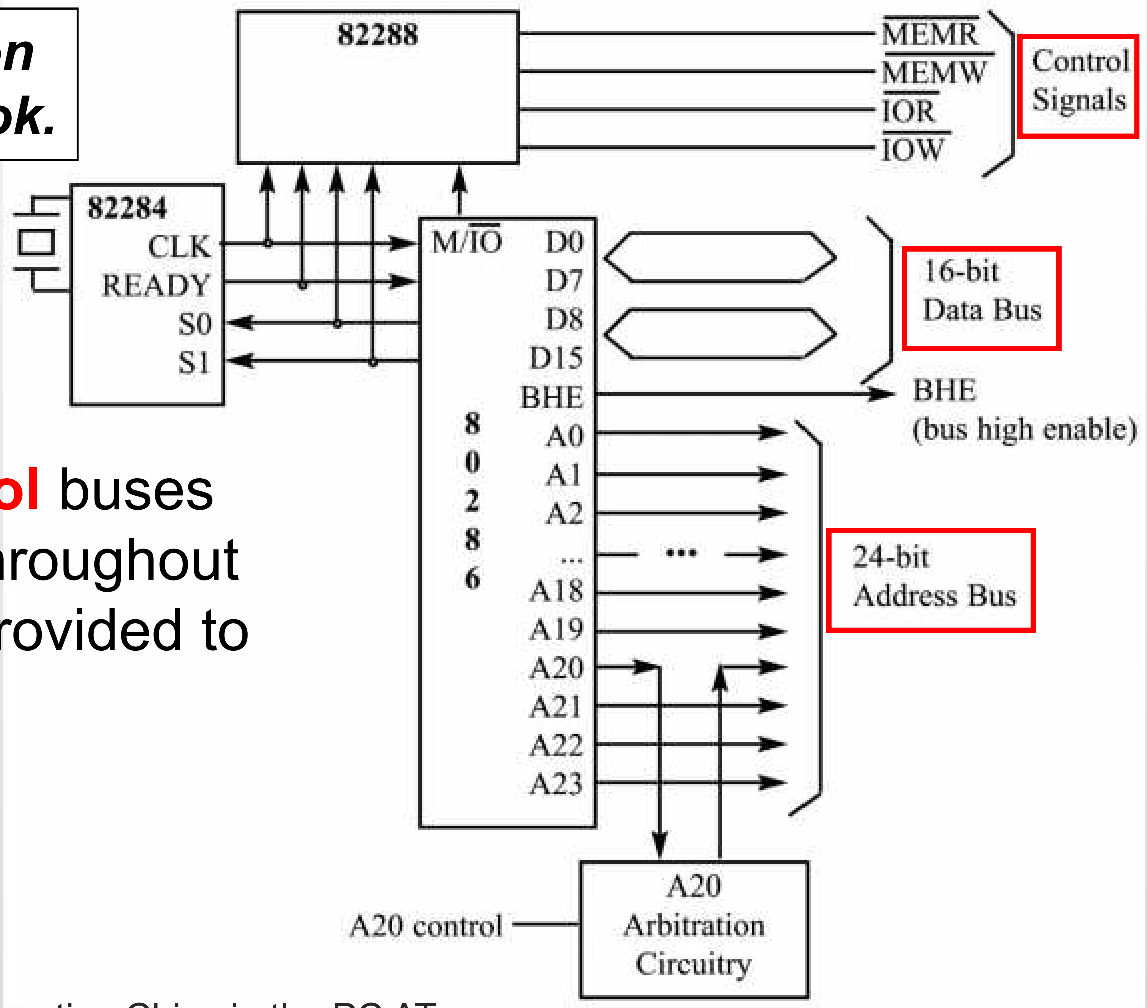
Fig. 9-16 ALE, DEN, and DTR Timing for 80286

16-BIT ISA BUS

- The origin of technical specifications of many of today's x86 PCs is the 80286-based IBM PC/AT.
  - A major legacy of those original PCs is the ISA (Industry Standard Architecture) bus slot.
- Material in this section is relevant and needs to be understood to design expansion cards for ISA slots.
  - For educational purposes, this book uses simple logic gates from the original PC to discuss design concepts.
    - Real world chipsets use CPLDs (Complex Programmable Logic Devices) with all the circuitry details buried inside.

16-BIT ISA BUS

This diagram appears on page 246 of your textbook.

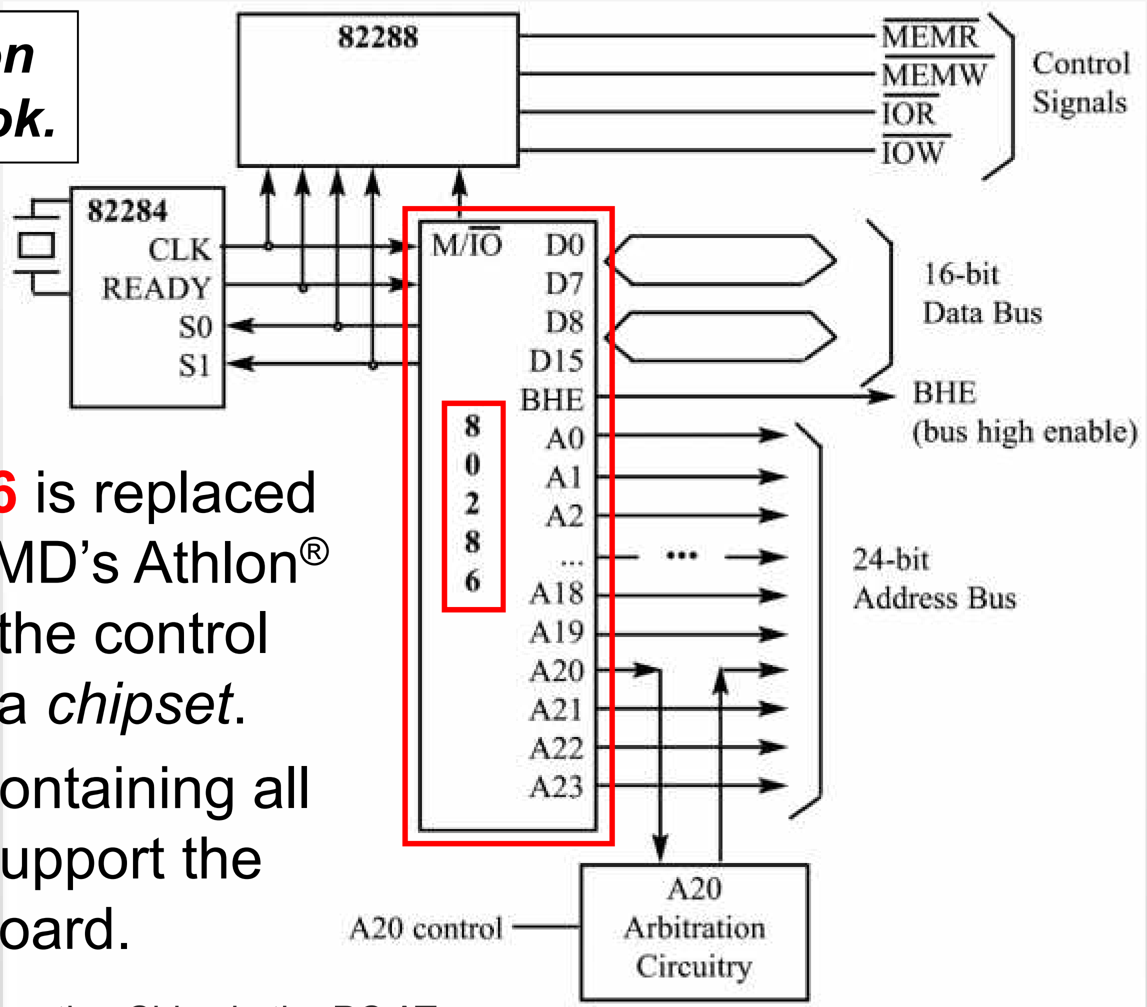


Address, **data** & **control** buses in this figure are used throughout the motherboard, and provided to the ISA expansion slot.

Fig. 9-17 80286 Block Diagram and Supporting Chips in the PC AT

16-BIT ISA BUS

This diagram appears on page 246 of your textbook.



In today's PC, the **80286** is replaced by Intel's Pentium® or AMD's Athlon® microprocessor, and all the control signals are provided by a *chipset*.

A chipset is an IC chip containing all the circuitry needed to support the CPU in a given motherboard.

Fig. 9-17 80286 Block Diagram and Supporting Chips in the PC AT

16-BIT ISA BUS
exploring ISA bus signals

- To maintain compatibility with the original PC, the 16-bit ISA slot used the 8-bit section as a subset.
  - The 8-bit section uses a 62-pin connector to provide access to the system buses.
    - A 36-pin connector was added to incorporate the new signals.
- In designing a plug-in peripheral card for the ISA slot we need to understand the basic features of the ISA signals.
  - The ISA bus has 24 address pins (A0–A23), 16 data pins (D0–D15), plus many control signals.

16-BIT ISA BUS
exploring ISA bus signals

- For compatibility with the IBM PC, the 16-bit ISA slot used the 8-bit section as a subset.
  - The 8-bit section uses a 62-pin connector to provide access to the system buses.

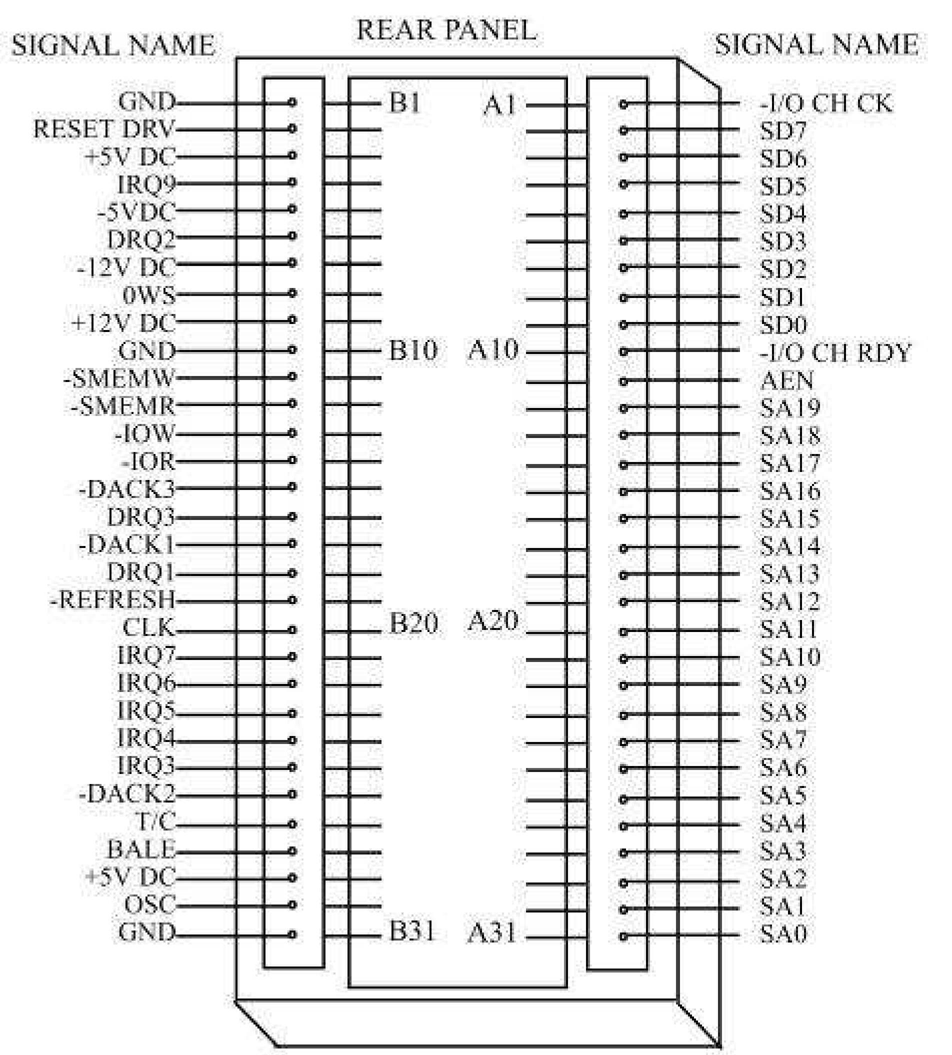


Fig. 9-18a ISA (IBM PC AT) Bus Slot Signals

16-BIT ISA BUS
exploring ISA bus signals

– A 36-pin connector was added to incorporate new signals.
  - In designing plug-in peripheral cards for the ISA slot, one must understand basic features of ISA signals.

The ISA bus has:

24 address pins. (A0–A23)
16 data pins. (D0–D15)
Many control signals.

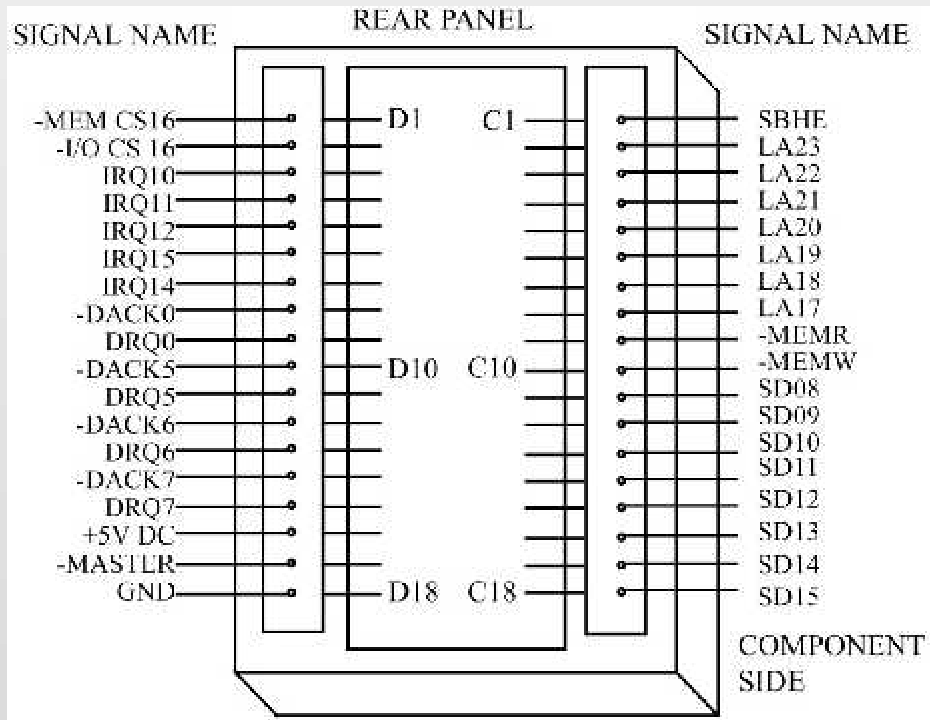


Fig. 9-18b ISA (IBM PC AT) Bus Slot Signals

16-BIT ISA BUS
address bus

- Addresses A0–A19 are latched using **ALE** - used throughout the motherboard and also provided to the 62-pin part of the ISA slot as SA0–SA19. (system address)
- A20–A23 part of the address is provided in the 36-pin section.
  - A17–A23 are provided as LA17–LA23 (latchable address).
- The **ALE** signal is provided as **BALE** (buffered **ALE**) and can be used to latch LA17–LA23.

16-BIT ISA BUS
data bus

- The data bus is composed of pins D0 to D15.
  - Buffered by a pair of 74ALS245 data bus transceivers, used by the motherboard to access memory and ports.
  - Also provided at the expansion slot as SD0–SD15. (system data)
- To select the upper byte or the lower byte of 16-bit data, use **BHE**. (bus high enable)
  - **BHE** is latched, used on the system board and provided at the expansion slot under **SBHE**. (system bus high enable)

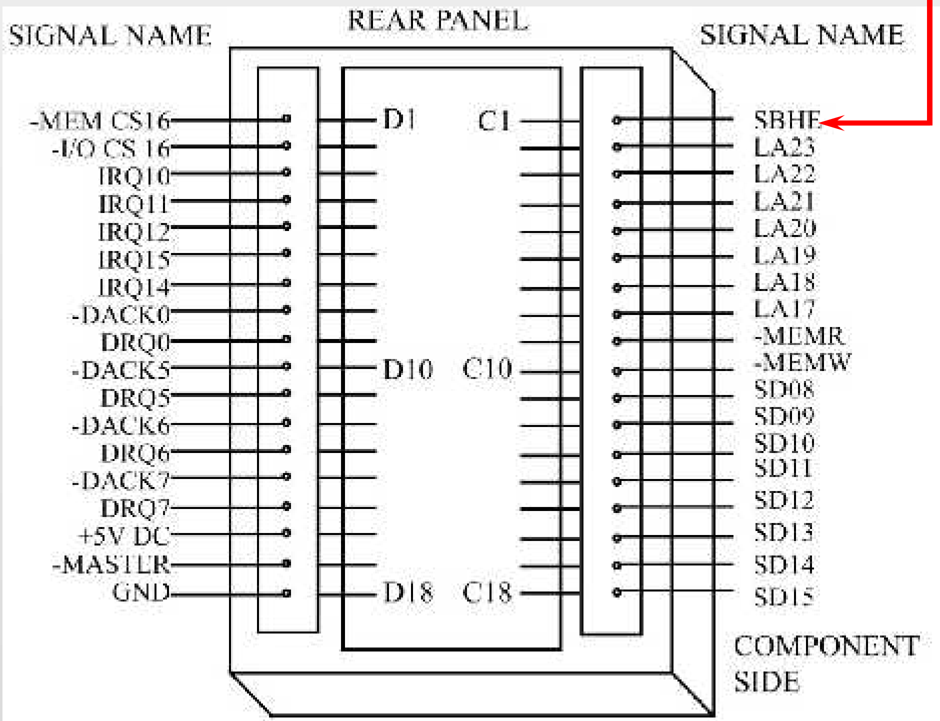
16-BIT ISA BUS
memory and I/O control signals

- **IOR** and **IOW** are control signals used to access ports throughout the system.
  - They show up on the 62-pin section of the ISA expansion slot, making them 8088 PC/XT compatible.
- **MEMR**, **MEMW** , **SMEMR** , and **SMEMW** are used to access memory.
  - To allow access to any memory within 16mb, read/write control signals are provided to the 36-pin section of the ISA expansion slot, designated **MEMR** and **MEMW**.

16-BIT ISA BUS
other control signals

- **ODD** & **EVEN** bytes and **BHE -** in the 36-pin section of the ISA bus there is a pin called **SBHE**.
  - Pin C1 is the same as the **BHE** pin from the 80286

As all general-purpose microprocessors, memory & I/O of x86 processors is byte addressable—every address location can provide a maximum of one byte of data.



16-BIT ISA BUS
other control signals

– If the CPU has an 8-bit data bus, the addresses are designated as 0 to **FFFFFH**, as shown at right.

– In Figure 9-19, the bus width for the data bus is **8 bits**.
  - Only 8 strips of wire connect the CPU's data bus to devices such as memory and I/O ports.

– The CPU's D0–D7 data bus is connected directly to the **D0–D7** data bus of memory & I/O devices.
  - A perfect match.

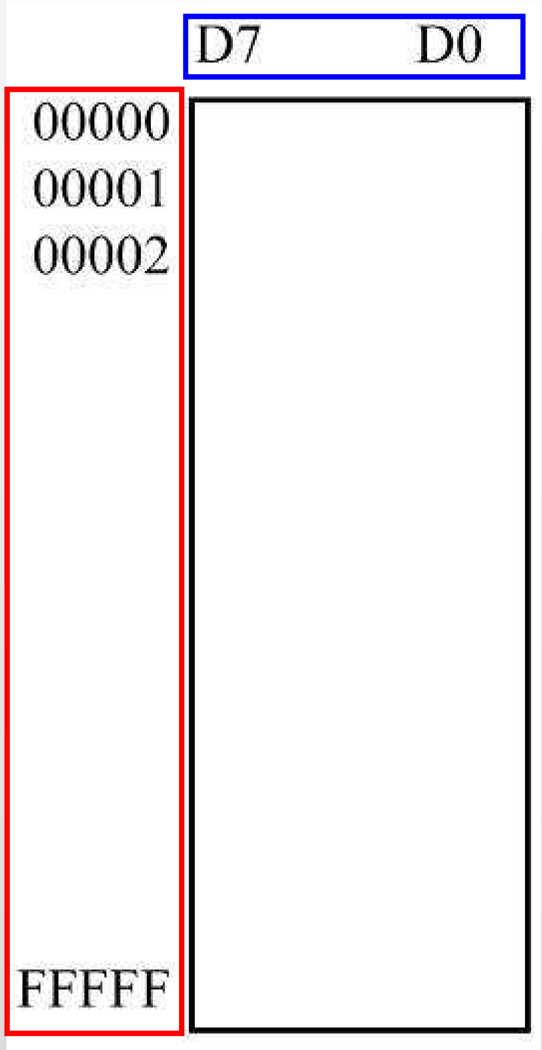


Fig. 9-19 Memory Byte Addressing in 8088 (8-Bit Data Bus)

16-BIT ISA BUS
other control signals

- If the CPU has a 16-bit data bus, address spaces are designated as odd and even bytes, as shown:

The **D0–D7** byte is designated as even.

D8–D15 byte as odd.

To distinguish between odd & even bytes, the 8086/286/386SX CPUs provide an extra signal called **BHE**.
(bus high enable)

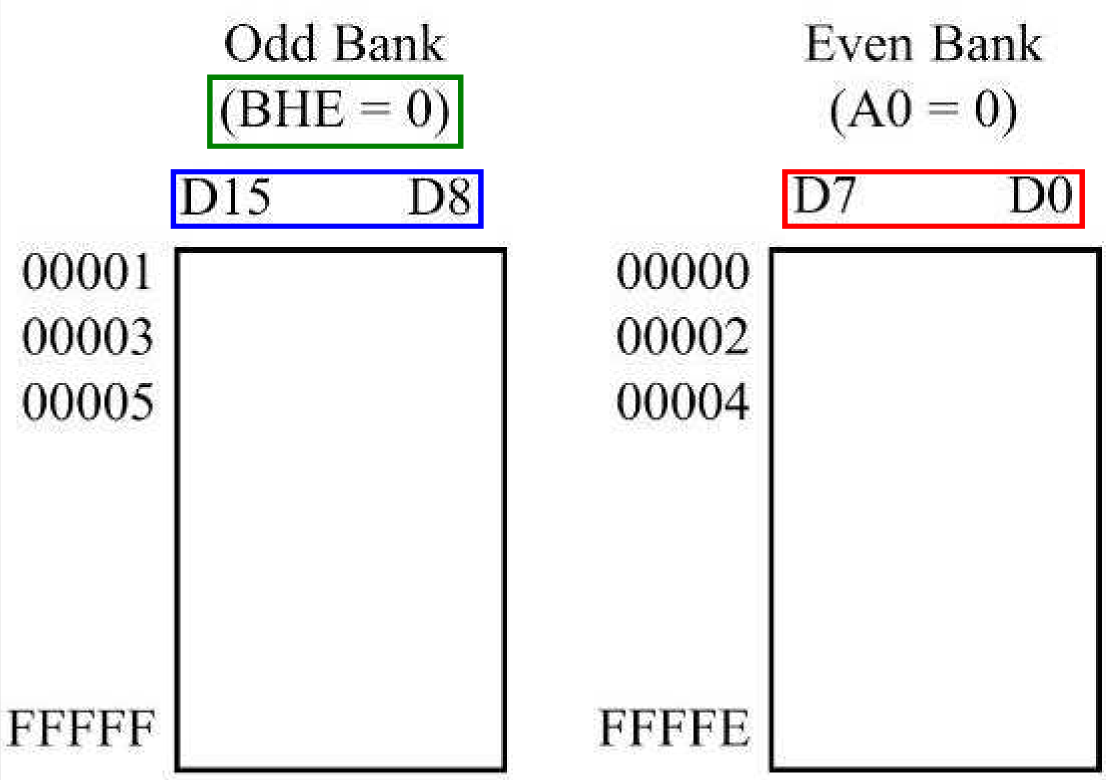


Fig. 9-20 Odd and Even Banks of Memory in 16-Bit CPUs (80286)

16-BIT ISA BUS
other control signals

BHE, in association with the **A0** pin, is used to select the odd or even byte.

Table 9-9: Distinguishing Between Odd and Even Bytes

BHE	A0		
0	0	Even word	D0–D15
0	1	Odd byte	D8–D15
1	0	Even byte	D0–D7
1	1	None	

16-BIT ISA BUS
A20 gate and the case of high memory area (HMA)

- In the 8088, when the segment register added to the offset is more than FFFFFH, it automatically wraps around and starts at 00000H.
  - In 80286 and higher processors in real mode, such a wrap-around will *not* occur.
    - The result will be 100000H, making A20 = 1.
- The problem is that A20–A23 is supposed to be activated *only* when the CPU is in protected mode.
  - To control activation of A20, IBM used a latch controlled by the keyboard in the original PC/AT.
  - With the introduction of PS computers, control of A20 can also be handled by port 92H.

16-BIT ISA BUS
A20 gate and the case of high memory area (HMA)

This diagram appears on page 246 of your textbook.

The process of enabling/disabling the **A20** gate in is handled by a piece of software called the *A20 handler*, provided with MS-DOS® and Windows® operating systems.

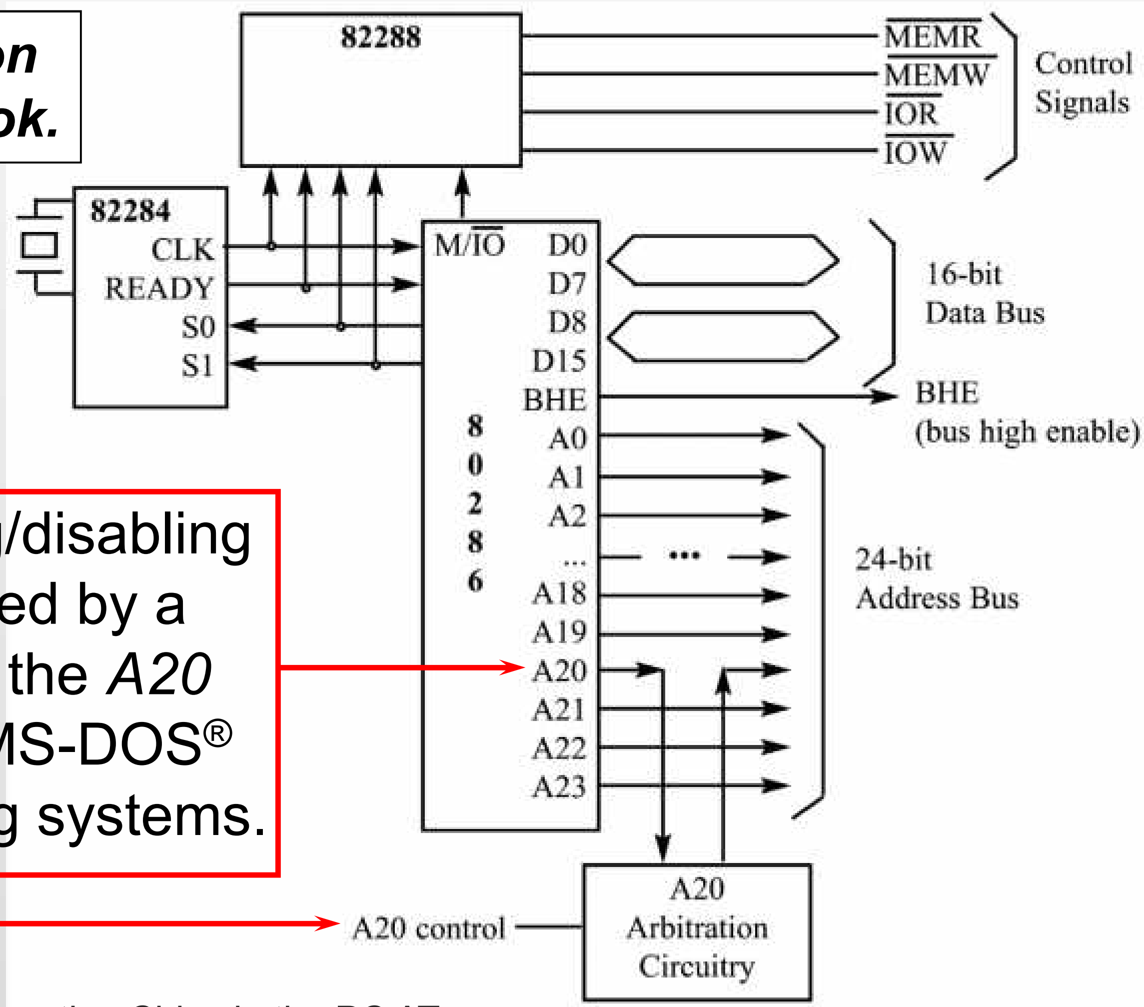


Fig. 9-17 80286 Block Diagram and Supporting Chips in the PC AT

9.5: 16-BIT ISA BUS
A20 gate and the case of high memory area (HMA)

- One can use the A20 gate (as it is commonly called) to create a high memory area (HMA).
  - Important for understanding HMA memory in x86 PCs.
    - Examples 9-1 and 9-2 for clarifiy this issue.

Example 9-2

Assume that CS = FF25H. Find the lowest and highest physical addresses for
(a) the 8088 (b) the 80286
Specify the bit on A20.

Solution:

(a) The lowest physical address is FF250H and the highest is 0F24FH (FF250H + FFFFH); since there are only lines A0–A19 in the 8088, the 1 is dropped.

(b) In the 286 the lowest address is the same as in the 8088, but the highest physical address is 10F24F; therefore, A20 = 1.

16-BIT ISA BUS
A20 gate and the case of high memory area (HMA)

Example 9-1

(a) If the A20 gate is enabled, show the highest address that 286 (and higher processors) can access while still in real mode.

(b) How far high above 1M is this address?

Solution:

(a) To access the highest physical location in real mode, we must have CS = FFFFH and IP = FFFFH. We shift left the segment register CS and add the offset IP = FFFF:

CS shifted left one hex digit	FFFF0H
adding the offset IP	+ FFFFH
	10FFEFH

Therefore, the addresses FFFF0H–10FFEFH are the range that the CPU can access while it is in real mode. This is a total of 64K bytes.

(b) If the A20 gate is enabled, accessible memory locations above 1M are 100000 to 10FFEF. This is a total of 65,520 bytes, or 16 locations short of 1M + 64K.

386 Protection Mode

- **Protection**
  - Protect the OS
  - Protect one user from the other
- 386 uses privilege level for protection
- **Virtual memory**
  - Segmentation: variable size
  - Paging: fixed size

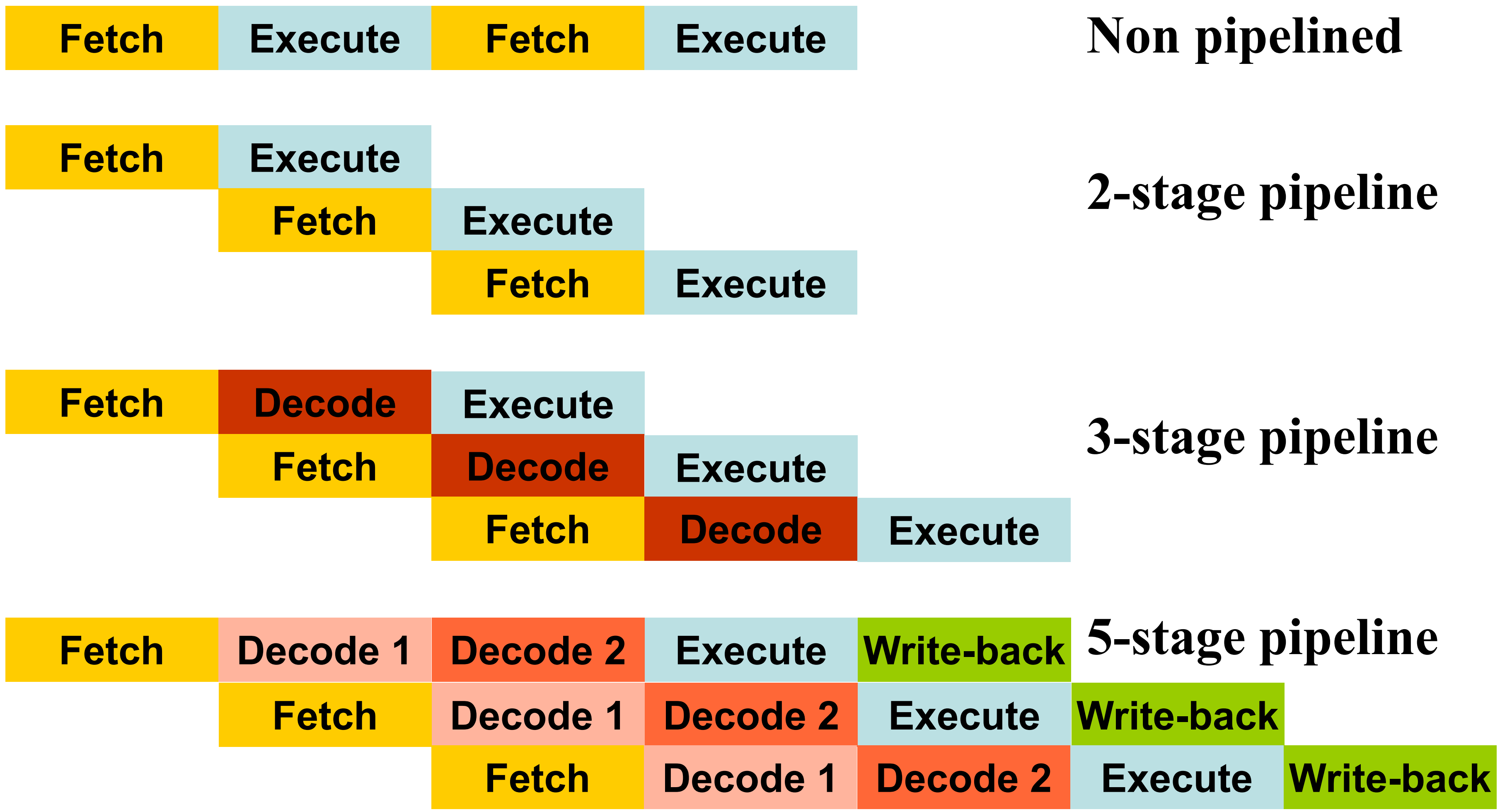
The 80486 Microprocessor

- The first **1-million** transistor microprocessor (actually 1.2 million)
- 168-pin PGA packaging (Pin Grid Array)
- 32-bit processor
- 486 has a 32-bit data bus (D0 – D31)
  - Data type: 8-bit, 16-bit, and 32-bit
- 486 has a 32-bit address bus (A2 – A31 plus BE0 – BE3)
  - Physical memory: 4G byte

Enhancements of the 486

- The pipeline stages is broken into **5 stages**
  - Fetch
  - Decode 1
  - Decode 2
  - Execute
  - Register write-back
- Many 486 instructions are executed in only **one** clock cycle because of using a deeper pipeline
- **On-chip cache** (8K byte) in microprocessor
  - eliminates the interchip delay of external cache.
- Math coprocessor on the **same chip** as the CPU
  - Faster execution of FP instructions
  - 486SX without math coprocessor

Pipeline vs. Nonpipelined Execution



Enhancements of the 486

- The use of 4 pins for **data parity** (bidirectional pins: DP0, DP1, DP2, and DP3)
- The 486 involves the **burst cycle**
  - Nonburst mode: it takes a minimum of 2 clocks to read from or write to external memory
  - Burst mode: 486 can perform 4 memory cycles in 5 clocks (2-1-1-1) for reading 4 double words (16 bytes).
- Supports new instructions
  - XADD EAX, EBX ; Exchange and add
  - BSWAP EAX ;change little endian to big endian
- The input frequency to the 486 is the same as the system frequency.

Three Ways to Increase the Processing Power of a CPU

- **Increase the clock frequency** of the chip
  - The higher frequency, the more power dissipation
  - The higher frequency, the more difficult the design of microprocessor and motherboard
  - The higher frequency, the more expensive
- Increase the number of data buses
- Change the internal architecture to exploit parallelism
  - Superpipeline: deeper pipeline
  - superscalar: issuing multiple instructions per clock cycle

Features of the Pentium

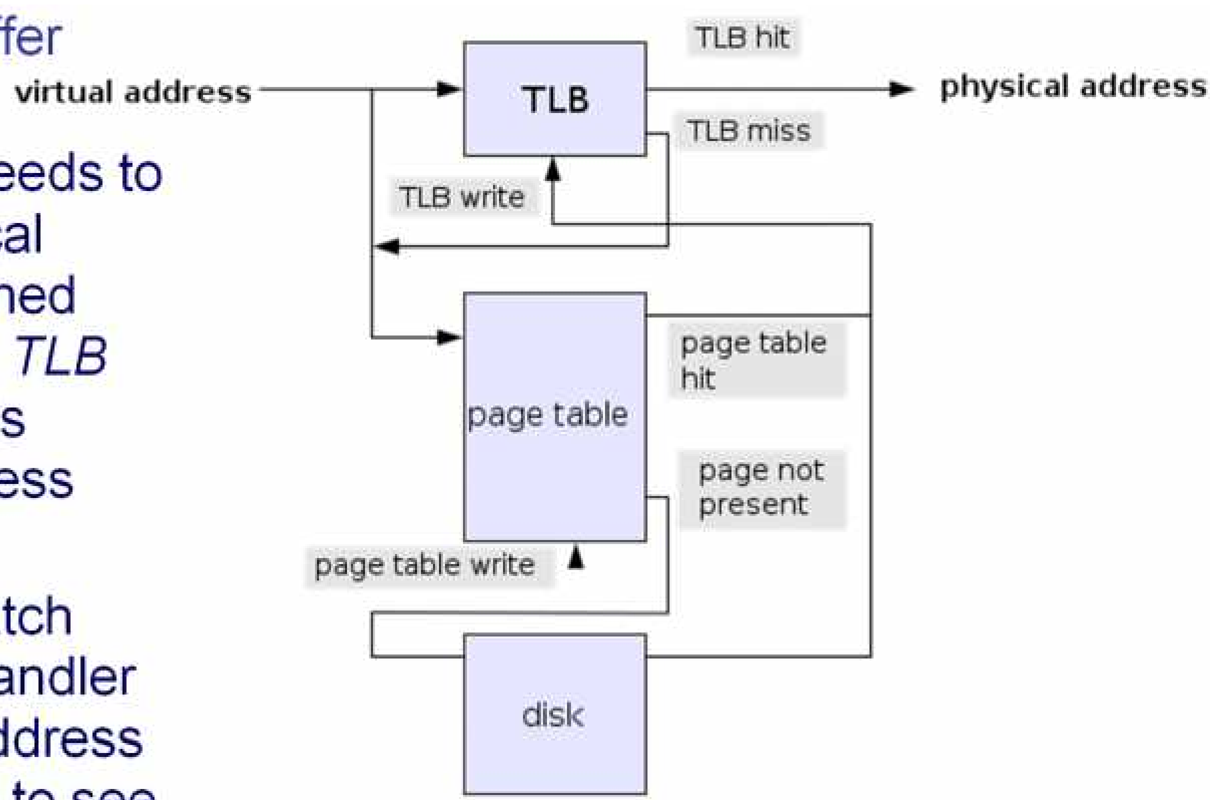
(3.1 million transistors and 273-pins)

- The external data bus is 64-bit
  - Pentium registers are 32-bit
  - 8 bytes external bus requires 8 byte enable (BE) pins
  - The data parity (DP) pins are 8 in Pentium
- The Pentium has 16K bytes of on chip cache (8K for code and 8K for data)
  - Internally, it has 4 buses:
    address code, code, address data, and data buses
- The on-chip math coprocessor of the Pentium (FPU) has been redesigned to be faster (8-stage pipeline).

Features of the Pentium

TLB

- Translation Lookaside Buffer (TLB):
- When a virtual address needs to be translated into a physical address, the TLB is searched first. If a match is found (a *TLB hit*), the physical address is returned and memory access can continue.
- However, if there is no match (called a *TLB miss*), the handler will typically look up the address mapping in the page table to see whether a mapping exists (a *Page Walk*).



Features of the Pentium

- The Pentium is a superscalar architecture
  - It has two execution unites (V: simple, U: complex)
- Includes branch prediction
- Provides the option of 4K and 4M for the page size
- The TLB for data: 64 entries for 4K pages and The TLB for code: 32 entries for 4K pages
- The Pentium has both burst read and burst write cycles.

RISC vs. CISC Architecture

RISC: Reduced Instruction Set Computer

CISC: Complex (Complete) Instruction Set Computer

- Small instruction set
- Fixed instruction size
- Load/store architecture
- Large number of registers
- Small task per instruction
- Simple instruction → simple decoder

Pentium Pro Processor

- 5.5 million transistors on 150 MHz
- Single package with two separate dies
- L2 cache (256K bytes) on a separate die to reduces the interchip delay.
- L1 cache (16K) on the same die with the CPU
- Internally RISC: translate 80x86 into micro-operations
- 12-stage pipeline: increase the clock rate
- It has multiple execution unites working in parallel
- Out-of-order execution: increase performance

Advanced Topics

- Pentium II: 7 million transistors, 266 MHz
- MMX: Multi Media eXtension
- Pentium III: 8.2 million transistors, 500 MHz
- SSE: Streaming SIMD Extension
- Pentium 4: 55 million transistors, 1.5 GHz

Little endian

- Little endian machine: Stores data **little-end first**. When looking at multiple bytes, the first byte is **smallest**.

- "Little Endian" means that the lower-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. For example, a 4 byte Integer

  Byte3 Byte2 Byte1 Byte0

  will be arranged in memory as follows:
  Base Address+0 Byte0
  Base Address+1 Byte1
  Base Address+2 Byte2
  Base Address+3 Byte3

  Intel processors (those used in PC's) use "Little Endian" byte order.

Big endian

- Big endian machine: Stores data **big-end first**. When looking at multiple bytes, the first byte (lowest address) is the biggest.

- "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address. The same 4 byte integer would be stored as:

  Base Address+0 Byte3
  Base Address+1 Byte2
  Base Address+2 Byte1
  Base Address+3 Byte0

  Motorola processors (those used in Mac's) use "Big Endian" byte order.