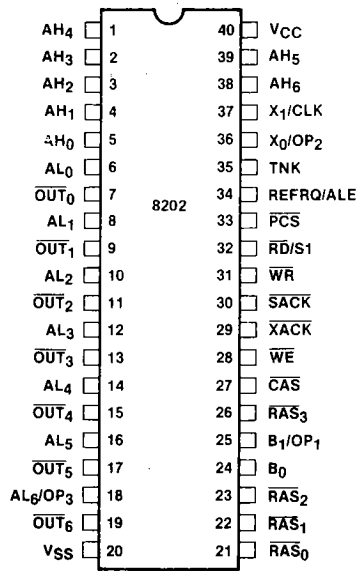
8202
DYNAMIC RAM CONTROLLER

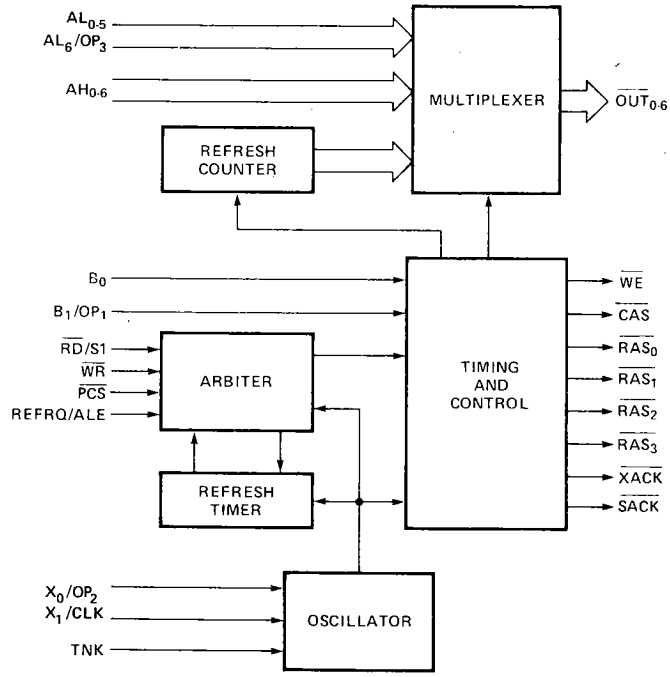
- **Provides All Signals Necessary to Control 2104A, 2117, or 2118 Dynamic Memories**
- **Directly Addresses and Drives Up to 128K Bytes Without External Drivers**
- **Provides Address Multiplexing and Strobes**
- **Provides a Refresh Timer and a Refresh Counter**
- **Refresh Cycles May be Internally or Externally Requested**
- **Provides Transparent Refresh Capability**
- **Fully Compatible with Intel® 8080A, 8085A and 8086 Microprocessors**
- **Decodes 8085A Status for Advanced Read Capability**
- **Provides System Acknowledge and Transfer Acknowledge Signals**
- **Internal or External Clock Capability**

The 8202 is a Dynamic RAM System Controller designed to provide all signals necessary to use 2104A, 2117, or 2118 Dynamic RAMs in microcomputer systems. The 8202 provides multiplexed addresses and address strobes, as well as refresh/access arbitration. Refresh cycles can be started internally or externally.

PIN CONFIGURATION



8202 BLOCK DIAGRAM



PIN DESCRIPTIONS

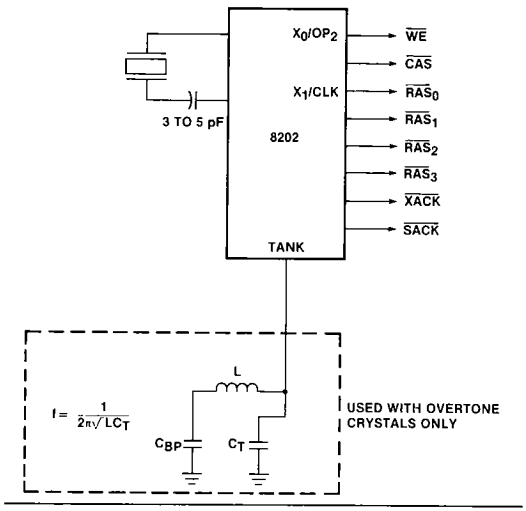
Pin Name	#	I/O	Pin Description
AL_0	6	I	Low-Order Address. These Address inputs are used to generate the Row Address for the Multiplexer. If the AL_6/OP_3 input is pulled to +12V through a 5KΩ resistor, the 8202 configures itself for 4K RAMs. If AL_6/OP_3 is driven with TTL levels, the 8202 configures itself for 16K RAMs.
AL_1	8	I	
AL_2	10	I	
AL_3	12	I	
AL_4	14	I	
AL_5	16	I	
AL_6/OP_3	18	I	
AH_0	5	I	High-Order Address. These Address inputs are used to generate the Column Address for the Multiplexer. If the 8202 is configured for 4K RAMs, AH_6 can be used as an active high Chip select for the memory controlled by 8202. For 16K RAM operation, AH_6 becomes the most significant column address bit.
AH_1	4	I	
AH_2	3	I	
AH_3	2	I	
AH_4	1	I	
AH_5	39	I	
AH_6	38	I	
$\overline{OUT_0}$	7	O	Output of the Multiplexer. These outputs are designed to drive the addresses of the Dynamic RAM array. For 4K RAM operation, $\overline{OUT_6}$ is designed to drive the 2104A $\overline{CS}$ input. (Note that the $\overline{OUT_{0-6}}$ pins do not require inverters or drivers for proper operation.
$\overline{OUT_1}$	9	O	
$\overline{OUT_2}$	11	O	
$\overline{OUT_3}$	13	O	
$\overline{OUT_4}$	15	O	
$\overline{OUT_5}$	17	O	
$\overline{OUT_6}$	19	O	
$\overline{WE}$	28	O	Write Enable. This output is designed to drive the Write Enable inputs of the Dynamic RAM array.
$\overline{CAS}$	27	O	Column Address Strobe. This output is used to latch the Column Address into the Dynamic RAM array.
$\overline{RAS_0}$	21	O	Row Address Strobe. These outputs are used to latch the Row Address into the bank of dynamic RAMs, selected by the 8202 Bank Address pins (B_0, B_1/OP_1)
$\overline{RAS_1}$	22	O	
$\overline{RAS_2}$	23	O	
$\overline{RAS_3}$	26	O	
B_0	24	I	Bank Address. These inputs are used to select one of four banks of dynamic RAM via the $\overline{RAS_{0-3}}$ outputs. If the B_1/OP_1 input is pulled to +12V through a 1KΩ resistor, the 8202 configures itself to the Advanced Read mode. This mode changes the function of the 8202 $\overline{RD}/S_1$ and REFRQ/ALE inputs and disables the $\overline{RAS_0}$ and $\overline{RAS_1}$ outputs.
B_1/OP_1	25	I	
$\overline{RD}/S_1$	32	I	Read/S_1 input. This input is used to request a read cycle. In normal operation, a low on this input informs the arbiter that a read cycle is requested. In the Advanced Read Mode, this input is designed to accept the S1 status signal from the 8085A (fully decoded for a read). The trailing edge of ALE informs the arbiter that a read cycle is requested by latching S_1.
$\overline{WR}$	31	I	Write Input. This input is used to request a write cycle. A low on this input informs the arbiter that a write cycle is desired.
$\overline{PCS}$	33	I	Protected Chip Select. A low on this input enables the $\overline{WR}$ and $\overline{RD}/S_1$ inputs. $\overline{PCS}$ is protected against terminating a cycle in progress.
REFRQ/ ALE	34	I	Refresh Request/Address Latch Enable. During normal operation, a high on this input indicates to the arbiter that a refresh cycle is being requested. In the Advanced Read Mode, this input is used to latch the state of the 8085 S1 signal into the $\overline{RD}/S_1$ input. If S_1 is high at this time, a Read Cycle is requested. In this mode, transparent refresh is not possible.
$\overline{XACK}$	29	O	Transfer acknowledge. This output is a strobe indicating valid data during a read cycle or data written during a write cycle. $\overline{XACK}$ can be used to latch valid data from the RAM array.
$\overline{SACK}$	30	O	System Acknowledge. This output indicates the beginning of a memory access cycle. It can be used as an advanced transfer acknowledge to eliminate wait states. (Note: If a memory access request is made during a refresh cycle, $\overline{SACK}$ is delayed until $\overline{XACK}$ in the memory access cycle).
X_0/OP_2	36	I	Crystal Inputs. These inputs are designed for a quartz crystal to control the frequency of the oscillator. If X_0/OP_2 is pulled to +12V through a 1KΩ resistor, X_1/CLK becomes a TTL input for an external clock.
X_1/CLK	37	I	
TNK	35		Tank. This pin is used for a tank circuit connection.
V_{CC}	40		+5V ± 10%
V_{SS}	20		Ground.

BASIC FUNCTIONAL DESCRIPTION

The 8202 consists of six basic blocks; the oscillator, the arbiter, the refresh timer, the refresh counter, the multiplexer, and the timing and control block.

Oscillator

The oscillator provides the basic timing for all 8202 operations. The oscillator circuit is designed primarily for use with an external series resonant fundamental mode crystal. Overtone crystals may be used with the tank circuit shown in Figure 1. A small capacitor (3-5) pF should be placed in series with any crystal to block D.C. stress and assure oscillation at the proper frequency.



The tank input to the oscillator allows the use of overtone mode crystals. The tank circuit shunts the crystal's fundamental and high overtone frequencies and allows the third harmonic to oscillate. The external LC network is connected to the TANK input and is AC coupled to ground.

If the X_0/OP_2 pin is pulled to +12V, through a 1KΩ resistor, the 8202 can be driven by a TTL clock on the X_1/CLK input. No tank circuit is required in this mode.

Arbiter

The 8202 provides 3 different operational cycles:

1. Read Cycle
2. Write Cycle
3. Refresh Cycle

The read and write cycles are initiated by external requests (RD/S_1 and PCS or WR and PCS). A refresh cycle may be initiated by the internal refresh timer, or by an external request (REFRQ/ALE). The arbiter resolves conflicts between cycle requests and cycles in execution.

If the B_1/OP_1 input is pulled to +12V through a 1KΩ resistor (Advanced Read mode), RD/S_1 becomes an input for the S_1 status signal of the 8085A (fully decoded for read). REFRQ/ALE becomes an input for the ALE signal of the 8085 (used to latch S_1. If S_1 is "high" at the falling edge of ALE, a read cycle will be requested. Transparent refresh is not possible in this mode.

Refresh Timer

The refresh timer is a simple timer that indicates to the arbiter that it is time for a refresh cycle. The refresh timer is reset when a refresh cycle is requested.

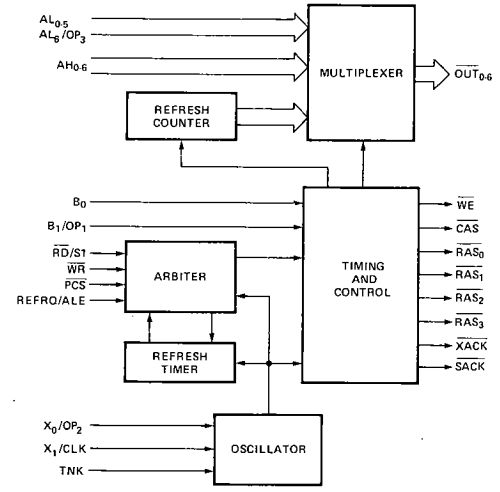
Refresh Counter

The refresh counter contains the address of the row to be refreshed. This counter is incremented after every refresh cycle.

Multiplexer

The multiplexer is designed to provide the dynamic RAM array with row addresses, column addresses and refresh addresses at the proper times. Its inputs consist of AL_{0-5}, AL_6/OP_3, AH_{0-6}, and the refresh counter.

If AL_6/OP_3 is pulled to +12V through a 5KΩ resistor, the 8202 configures itself for 4K RAMs. In this mode, AL_{0-5} provides the multiplexer with the six bit row address. AH_{0-5} provides the multiplexer with the six bit column address.



$\overline{OUT}_{0-5}$ provide the RAM array with twelve bits of multiplexed address. AH_6 can be used as an active high chip select for the RAM array if $\overline{OUT}_6$ drives $\overline{CS}$. Note that the $\overline{OUT}_{0-6}$ signals do not require inverters or drivers.

If the 8202 is configured for 16K RAMs, AL_{0-5} and AL_6/OP_3 provide the multiplexer with seven bits of row

address. AH_{0-6} provides it with seven bits of column address. $\overline{OUT}_{0-6}$ provides the RAM array with fourteen bits of multiplexed address.

Timing and Control Block

The timing and control block executes one of three operational cycles at the request of the arbiter (Read, Write, and Refresh cycles). It provides the RAM array with $\overline{WE}$, $\overline{CAS}$, and $\overline{RAS}$ signals. It provides the CPU with transfer and system acknowledge ($\overline{XACK}$ and $\overline{SACK}$) signals. It controls the multiplexer during all cycles. It resets the refresh timer and increments the refresh counter during refresh cycles.

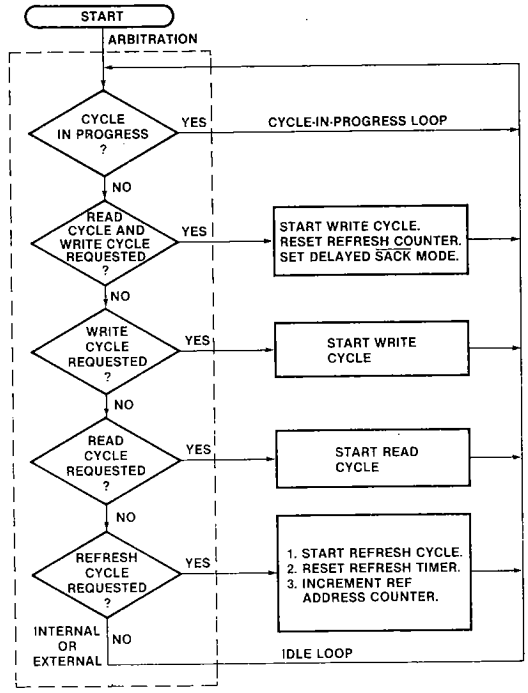
Inputs B_0 and B_1/OP_1 are used to select one of four banks of dynamic RAM via the $\overline{RAS}_{0-3}$ outputs.

If B_1/OP_1 is pulled to +12V through a 1KΩ resistor, the 8202 configures itself to the Advanced Read Mode. This mode changes the function of the $\overline{RD}/S_1$ and REFRQ/ALE inputs and disables the $\overline{RAS}_0$ and $\overline{RAS}_1$ outputs.

SYSTEM OPERATION

The 8202 is always in one of the following states:

1. Idle.
2. Performing a Test Cycle.
3. Performing a Write Cycle.
4. Performing a Read Cycle.
5. Performing a Refresh Cycle.



Idle

When the 8202 is idle, no cycle is in progress, the arbiter monitors internal and external cycle requests, and the refresh timer counts towards an internal refresh cycle request. (Fig. X.1)

While the 8202 is idle, the arbiter samples access cycle requests and refresh cycle requests, internal or external, on the rising edge of clock. If both Read and Write cycle requests are active when sampled, a test cycle is started. If a write-cycle request is active when sampled, a write cycle is started. If a read cycle request is active when sampled, a read cycle is started. If a refresh cycle request was previously pulsed or is active when sampled, a refresh cycle is started. Due to internal delays, if an access cycle request and a refresh cycle request occur simultaneously, the access cycle will be executed before the refresh cycle is executed.

Test Cycle

When a test cycle is started, (Read and Write Cycle Requests both active when sampled) the refresh counter is set to zero and the delayed $\overline{SACK}$ mode is reset, while the 8202 executes a write cycle. This cycle is used for testing only and is not recommended for normal system operation.

Write Cycle (Fig. X.2)

When a write cycle is started, (Write-Cycle Request active when sampled) the Multiplexer drives the $\overline{OUT}$ 0-6 pins with the low order address. Then, if the delayed $\overline{SACK}$ Mode is not set, $\overline{SACK}$ is activated. The row address is strobed into the selected bank of RAMs. The multiplexer then drives the $\overline{OUT}$ 0-6 pins with the high order address and the write enable ($\overline{WE}$) pin is activated. The column address is then strobed into the RAM array.

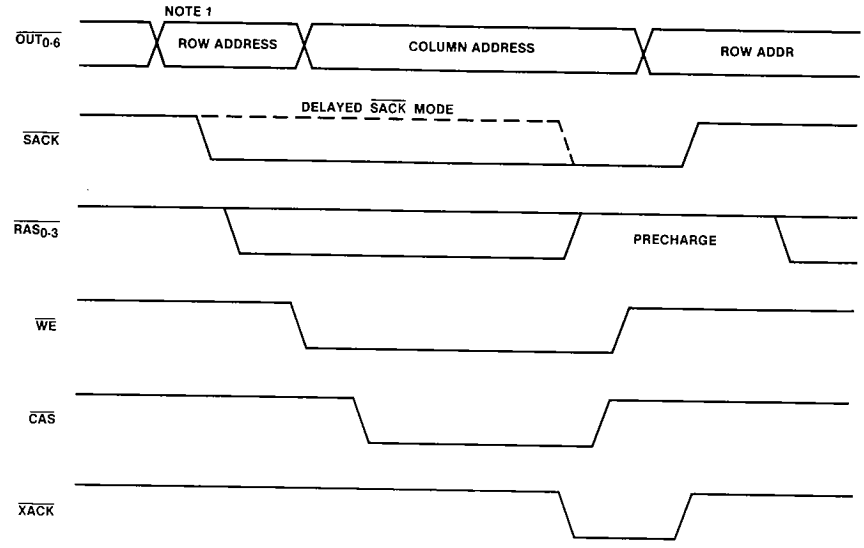
Near the end of the cycle, the $\overline{XACK}$ output is activated. If the Delayed $\overline{SACK}$ Mode is set, $\overline{SACK}$ had the same timing as $\overline{XACK}$. At the end of the cycle, all signals are deactivated, the Delayed $\overline{SACK}$ Mode is exited, and the precharge time begins. After the precharge time, the 8202 re-enters the idle state. The refresh timer continues to count during access cycles.

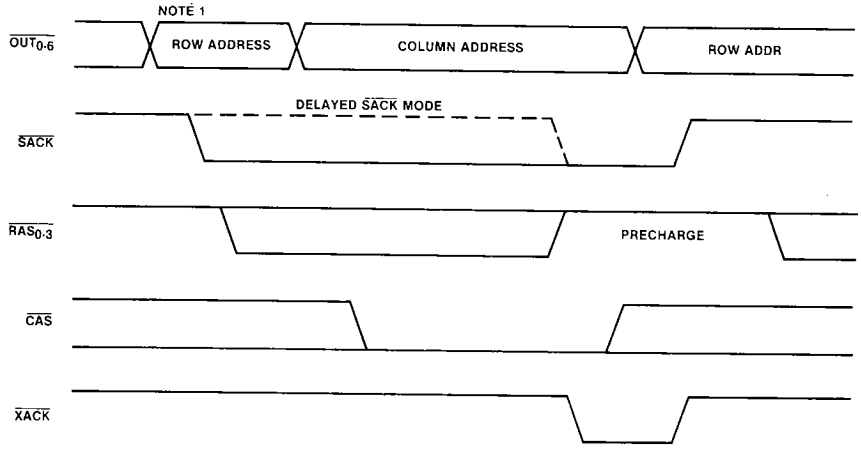
If the REFRQ pin is pulsed or held active while a write cycle is in progress, a refresh cycle will occur immediately following the write cycle, if the Advanced Read Mode is not selected.

Read Cycle (Fig. X.3)

Read cycle operation is the same as write cycle operation, except the write enable ($\overline{WE}$) signal is not activated.

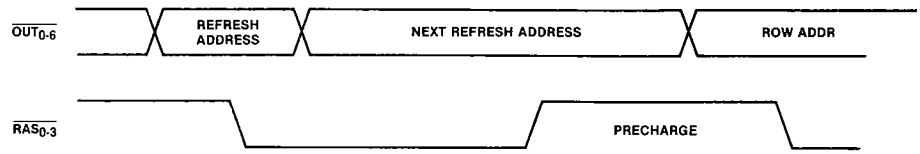
If the REFRQ pin is pulsed or held active while a read cycle is in progress, a refresh cycle will occur immediately following the read cycle, if the Advanced Read Mode is not selected.





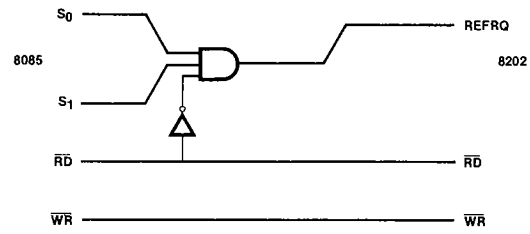
Refresh Cycle (Fig. X.4)

When a refresh cycle is started, (refresh-cycle request previously pulsed or active when sampled) the 8202 resets the Refresh Timer. The Multiplexer drives the OUT 0-6 pins with the refresh address contained in the Refresh Counter. The 8202 then activates the Row Address Strobe (RAS 0-3) signals. At the end of the refresh cycle, all signals are deactivated, the refresh counter is incremented, and the precharge time begins. After the precharge time, the 8202 re-enters the Idle State.



Hidden Refresh Cycle

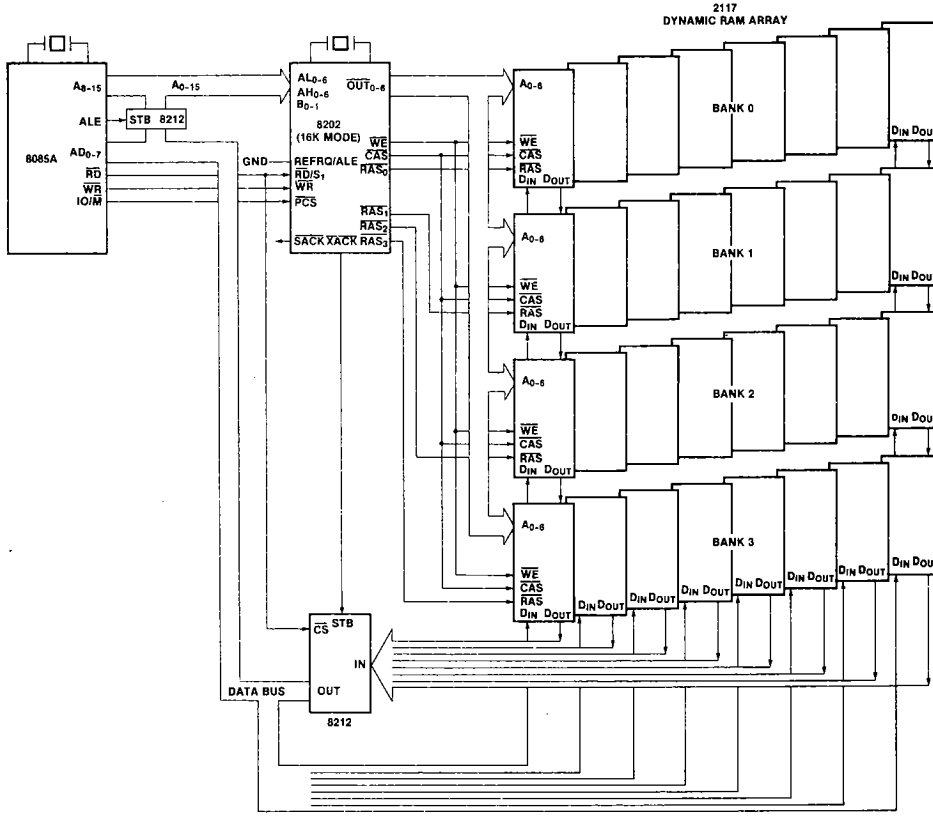
Distributed hidden refresh operation is most efficient if REFRQ is strobed during a command cycle such as fetch, where it is intended for the refresh cycle to follow. This is illustrated for 8085 in the following diagram.



System Configurations

Currently, there exists a wide range of processor bus structures, processor speeds, and memory speeds. As a result, the 8202 offers many possible system configurations with equally many cost-performance tradeoffs.

The following system block diagram illustrates just one of the possible system configurations supported by the 8202:



Other system configurations are described in the Intel, Application Note AP45, "Using the 8202 Dynamic RAM Controller." Other related documents are:

- "Intel Memory Design Handbook" (Dynamic Ram sections).
- AR-1, "Simplify Your Dynamic RAM/Microprocessor Interface."
- AP-38, "Application Techniques for the Intel 8085A Bus."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V[1]
Power Dissipation ..... 1.4 Watts

[1] −0.5V to +10.0 volts for pins 18, 25, 36.

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to 70°C; $V_{CC} = 5.0V \pm 10\%$; GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
V_C	Input Clamp Voltage		−1.0	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		250	mA	
I_F	Forward Input Current				
	X_1/CLK		−2.0	mA	$V_F = 0.45V$
	All Other Inputs		−320	μA	$V_F = 0.45V$
I_R	Reverse Input Current		40	μA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage				
	$\overline{SACK}$, $\overline{XACK}$		0.45	V	$I_{OL} = 5$ mA
	All Other Outputs		0.45	V	$I_{OL} = 3$ mA
V_{OH}	Output High Voltage				
	$\overline{SACK}$, $\overline{XACK}$	2.4		V	$I_{OH} = -1$ mA
	All Other Outputs	2.6		V	$I_{OH} = -1$ mA
V_{IL}	Input Low Voltage		0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input High Voltage	2.0		V	$V_{CC} = 5.0V$

CAPACITANCE

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		30	pF	F = 1 MHz $V_{BIAS} = 2.5V$, $V_{CC} = 5V$ $T_A = 25°C$

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Loading:
32 devices

$\overline{SACK}$, $\overline{XACK}$	CL = 30 pF
$\overline{OUT_0} - \overline{OUT_6}$	CL = 160 pF
$\overline{RAS_1} - \overline{RAS_4}$	CL = 115 pF
$\overline{WE}$	CL = 224 pF
$\overline{CAS}$	CL = 320 pF

Measurements made with respect to $RAS_1 - RAS_4$, CAS, WE, $OUT_0 - OUT_6$ are at 2.4V and 0.8V. All other pins are measured at 1.5V.

Symbol	Parameter	Min	Max	Units
t_P	Clock (Internal/External) Period (See Note 1)	40	DC	ns
t_{RC}	Memory Cycle Time	$10\ t_P - 30$	$12\ t_P$	ns
t_{RAH}	Row Address Hold Time	$t_P - 10$		ns
t_{ASR}	Row Address Setup Time	t_{PH}		ns
t_{CAH}	Column Address Hold Time	$5\ t_P$		ns
t_{ASC}	Column Address Setup Time	$t_P - 35$		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$2\ t_P - 10$	$2\ t_P + 30$	ns
t_{WCS}	$\overline{WE}$ Setup to $\overline{CAS}$	$t_P - 40$		ns
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$	$5\ t_P - 30$		ns
t_{CAS}	$\overline{CAS}$ Pulse Width	$5\ t_P$		ns
t_{RP}	$\overline{RAS}$ Precharge Time (See Note 2)	$4\ t_P - 30$		ns
t_{WCH}	$\overline{WE}$ Hold Time to $\overline{CAS}$	$5\ t_P - 20$		ns
t_{REF}	Internally Generated Refresh to Refresh Time 64 Cycle 128 Cycle	 $548\ t_P$ $264\ t_P$	 $576\ t_P$ $288\ t_P$	ns ns ns
t_{CR}	$\overline{RD}$, $\overline{WR}$ to $\overline{RAS}$ Delay	$t_{PH} + 30$	$t_{PH} + t_P + 75$	ns
t_{CC}	$\overline{RD}$, $\overline{WR}$ to $\overline{CAS}$ Delay	$t_{PH} + 2\ t_P + 25$	$t_{PH} + 3\ t_P + 85$	ns
t_{RFR}	REFRQ to $\overline{RAS}$ Delay	$1.5\ t_P + 30$	$2.5\ t_P + 100$	ns
t_{AS}	$A_0 - A_{15}$ to $\overline{RD}$, $\overline{WR}$ Setup Time (See Note 4)	0		ns
t_{CA}	$\overline{RD}$, $\overline{WR}$ to $\overline{SACK}$ Leading Edge		$t_P + 40$	ns
t_{CK}	$\overline{RD}$, $\overline{WR}$ to $\overline{XACK}$, $\overline{SACK}$ Trailing Edge Delay		30	ns
t_{KCH}	$\overline{RD}$, $\overline{WR}$ Inactive Hold to $\overline{SACK}$ Trailing Edge	10		ns
t_{SC}	$\overline{RD}$, $\overline{WR}$, $\overline{PCS}$ to X/CLK Setup Time (See Note 3)	15		ns
t_{CX}	$\overline{CAS}$ to $\overline{XACK}$ Time	$5\ t_P - 25$	$5\ t_P + 20$	ns
t_{ACK}	$\overline{XACK}$ Leading Edge to $\overline{CAS}$ Trailing Edge Time	10		ns
t_{XW}	$\overline{XACK}$ Pulse Width	$2\ t_P - 25$		ns
t_{LL}	REFRQ Pulse Width	20		ns
t_{CHS}	$\overline{RD}$, $\overline{WR}$, $\overline{PCS}$ Active Hold to $\overline{RAS}$	0		ns
t_{WW}	$\overline{WR}$ to $\overline{WE}$ Propagation Delay	8	50	ns
t_{AL}	S_1 to ALE Setup Time	40		ns
t_{LA}	S_1 to ALE Hold Time	$2\ t_P + 40$		ns
t_{PL}	External Clock Low Time	15		ns
t_{PH}	External Clock High Time	20		ns
t_{PH}	External Clock High Time for $V_{CC} = 5V \pm 5\%$	17		ns

Notes:
1. t_P minimum determines maximum oscillator frequency.
   t_P should not exceed 54 nsec for RAM's with 2 msec refresh rate.
2. To achieve the minimum time between the $\overline{RAS}$ of a memory cycle and the $\overline{RAS}$ of a refresh cycle, such as a transparent refresh, REFRQ should be pulsed in the previous memory cycle.
3. t_{SC} is not required for proper operation which is in agreement with the other specs, but can be used to synchronize external signals with X/CLK if it is desired.
4. If t_{AS} is less than 0 then the only impact is that t_{ASR} decreases by a corresponding amount.

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Loading:
64 Devices

$\overline{SACK}$, $\overline{XACK}$	CL = 30 pF
$\overline{OUT_0} - \overline{OUT_6}$	CL = 320 pF
$\overline{RAS_1} - \overline{RAS_4}$	CL = 230 pF
$\overline{WE}$	CL = 450 pF
$\overline{CAS}$	CL = 640 pF

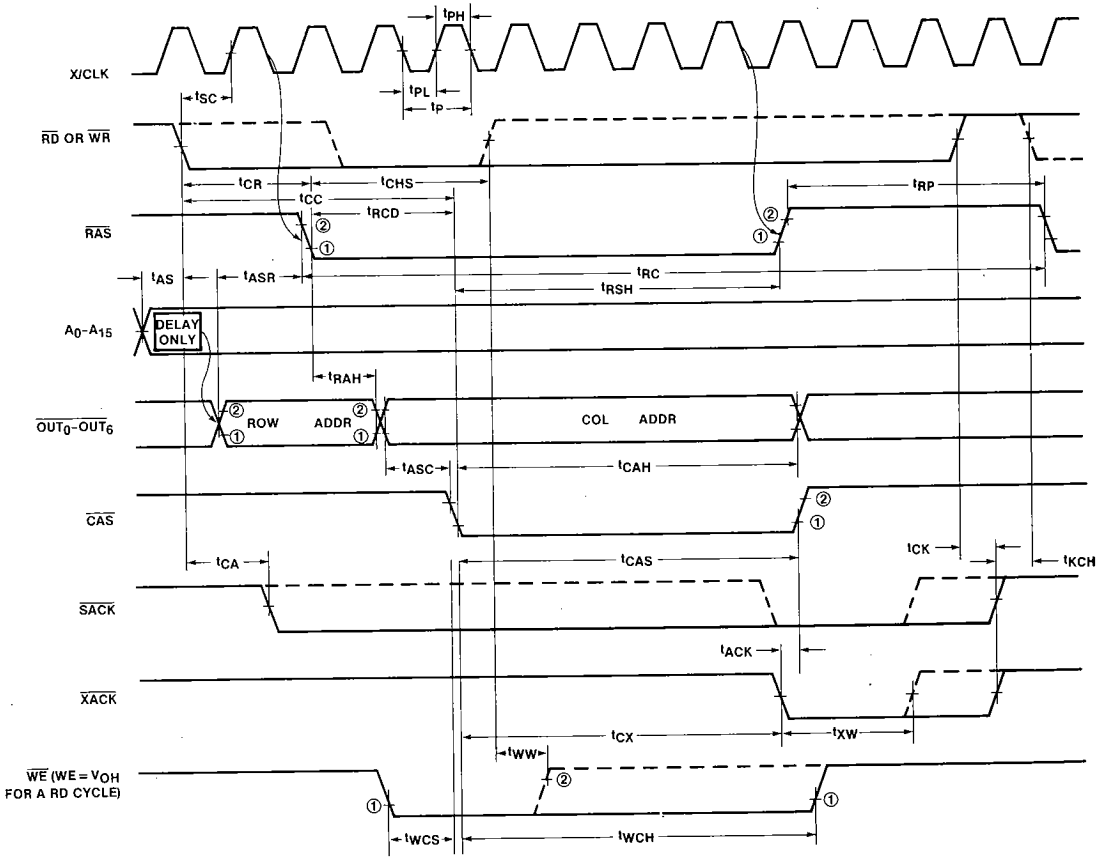
Measurements made with respect to $RAS_1 - RAS_4$, CAS, WE, $OUT_0 - OUT_6$ are at 2.4V and 0.8V. All other pins are measured at 1.5V.

Symbol	Parameter	Min	Max	Units
t_P	Clock (Internal/External) Period (See Note 1)	40	54	ns
t_{RC}	Memory Cycle Time	$10\ t_P - 30$	$12\ t_P$	ns
t_{RAH}	Row Address Hold Time	$t_P - 10$		ns
t_{ASR}	Row Address Setup Time	t_{PH}		ns
t_{CAH}	Column Address Hold Time	$5\ t_P$		ns
t_{ASC}	Column Address Setup Time	$t_P - 35$		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$2\ t_P - 10$	$2\ t_P + 45$	ns
t_{WCS}	$\overline{WE}$ Setup to $\overline{CAS}$	$t_P - 40$		ns
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$	$5\ t_P - 30$		ns
t_{CAS}	$\overline{CAS}$ Pulse Width	$5\ t_P - 30$		ns
t_{RP}	$\overline{RAS}$ Precharge Time (See Note 2)	$4\ t_P - 30$		ns
t_{WCH}	$\overline{WE}$ Hold Time to $\overline{CAS}$	$5\ t_P - 35$		ns
t_{REF}	Internally Generated Refresh to Refresh Time 64 Cycle 128 Cycle	 $548\ t_P$ $264\ t_P$	 $576\ t_P$ $288\ t_P$	 ns ns
t_{CR}	$\overline{RD}$, $\overline{WR}$ to $\overline{RAS}$ Delay	$t_{PH} + 30$	$t_{PH} + t_P + 75$	ns
t_{CC}	$\overline{RD}$, $\overline{WR}$ to $\overline{CAS}$ Delay	$t_{PH} + 2\ t_P + 25$	$t_{PH} + 3\ t_P + 100$	ns
t_{RFR}	REFRQ to $\overline{RAS}$ Delay	$1.5\ t_P + 30$	$2.5\ t_P + 100$	ns
t_{AS}	$A_0 - A_{15}$ to $\overline{RD}$, $\overline{WR}$ Setup Time (See Note 4)	0		ns
t_{CA}	$\overline{RD}$, $\overline{WR}$ to $\overline{SACK}$ Leading Edge		$t_P + 40$	ns
t_{CK}	$\overline{RD}$, $\overline{WR}$ to $\overline{XACK}$, $\overline{SACK}$ Trailing Edge Delay		30	ns
t_{KCH}	$\overline{RD}$, $\overline{WR}$ Inactive Hold to $\overline{SACK}$ Trailing Edge	10		ns
t_{SC}	$\overline{RD}$, $\overline{WR}$, $\overline{PCS}$ to X/CLK Setup Time (See Note 3)	15		ns
t_{CX}	$\overline{CAS}$ to $\overline{XACK}$ Time	$5\ t_P - 40$	$5\ t_P + 20$	ns
t_{ACK}	$\overline{XACK}$ Leading Edge to $\overline{CAS}$ Trailing Edge Time	10		ns
t_{XW}	$\overline{XACK}$ Pulse Width	$2\ t_P - 25$		ns
t_{LL}	REFRQ Pulse Width	20		ns
t_{CHS}	$\overline{RD}$, $\overline{WR}$, $\overline{PCS}$ Active Hold to $\overline{RAS}$	0		ns
t_{WW}	$\overline{WR}$ to $\overline{WE}$ Propagation Delay	8	50	ns
t_{AL}	S_1 to ALE Setup Time	40		ns
t_{LA}	S_1 to ALE Hold Time	$2\ t_P + 40$		ns
t_{PL}	External Clock Low Time	15		ns
t_{PH}	External Clock High Time	22		ns
t_{PH}	External Clock High Time for $V_{CC} = 5V \pm 5\%$	18		ns

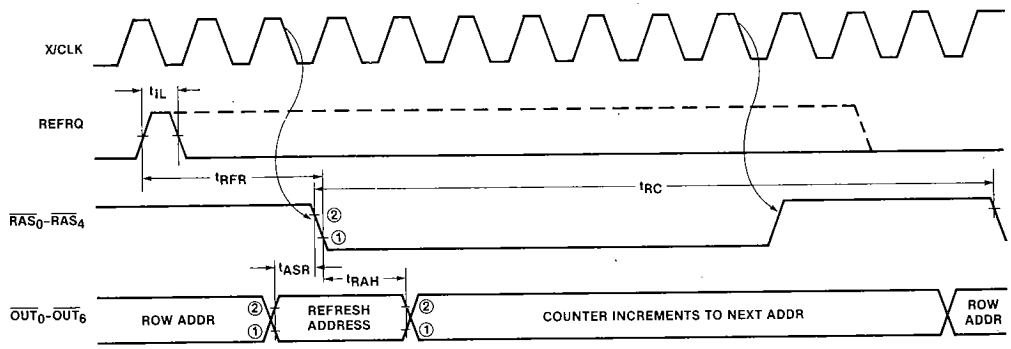
Notes:
1. t_P minimum determines maximum oscillator frequency.
   t_P maximum determines minimum frequency to maintain 2 ms refresh rate and t_{RP} minimum.
2. To achieve the minimum time between the $\overline{RAS}$ of a memory cycle and the $\overline{RAS}$ of a refresh cycle, such as a transparent refresh, REFRQ should be pulsed in the previous memory cycle.
3. t_{SC} is not required for proper operation which is in agreement with the other specs, but can be used to synchronize external signals with X/CLK if it is desired.
4. If t_{AS} is less than 0 then the only impact is that t_{ASR} decreases by a corresponding amount.

8202 TIMING

NORMAL READ OR WRITE CYCLE

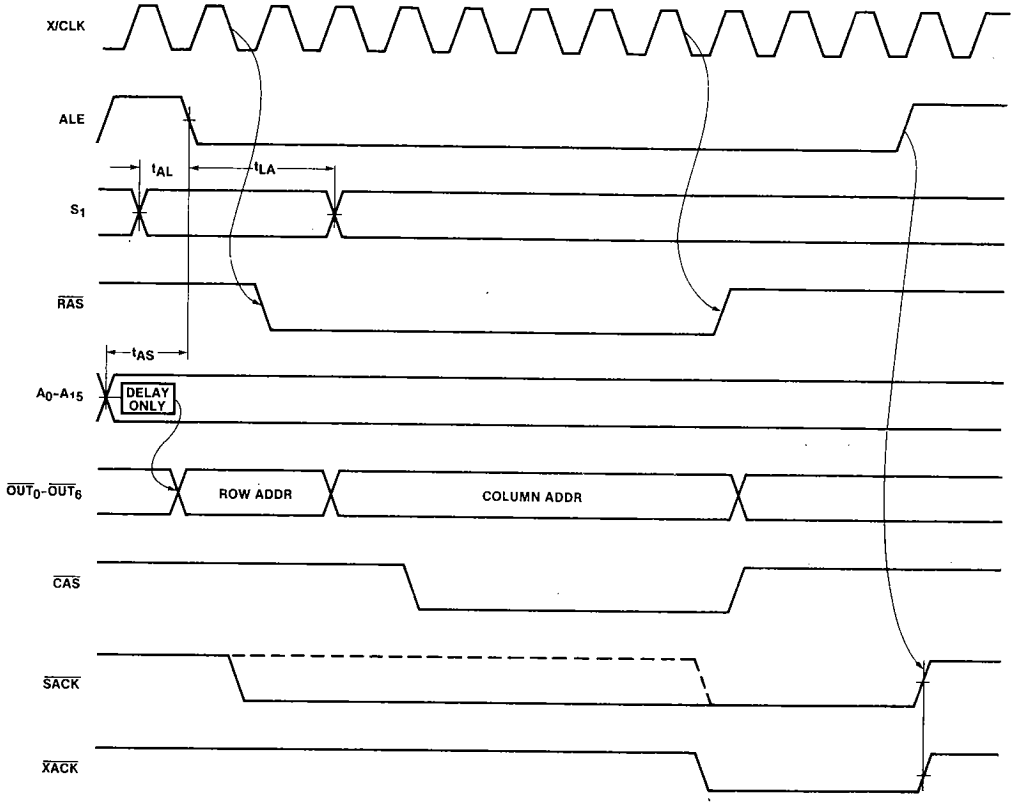


REFRESH CYCLE



(CAS = VOH) IF THE REFRESH CYCLE IS INTERNALLY TRIGGERED THEN IGNORE REFRQ.

ADVANCED READ MODE USING THE SIMPLIFIED 8085 INTERFACE OPTION



OTHER TIMING PARAMETERS ARE THE SAME AS NORMAL MODE
WRITE CYCLE IS THE SAME AS NORMAL MODE EXCEPT THAT $\overline{XACK}$ AND $\overline{SACK}$ GO INACTIVE ON THE RISING EDGE OF ALE

MPO PERIPHERALS

OUTPUT TEST LOAD CIRCUIT