

# Schematics For Lunzn r68s

## RK3568

### Main Functions Introduction

- 1) PMIC: RK809-5+DiscretePower
- 2) RAM: LPDDR4 1x32Bit 16Gb
- 3) ROM: eMMC5.1 64Gb
- 4) Support: 1 x USB3.0 OTG + 1 x USB3.0 HOST
- 5) Support: 2 x 1Lanes PCIe - 2.5G Ethernet
- 6) Support: 2 x 10/100/1000 Ethernet(RGMII)
- 7) Support: 1 x IR Receiver
- 8) Support: 1 x Power LED, 1 x Sytem LED RJ45^LED
- 9) Support: 1 x Recovery Key
- 10) Support: Debug UART



深圳市岚正科技有限公司

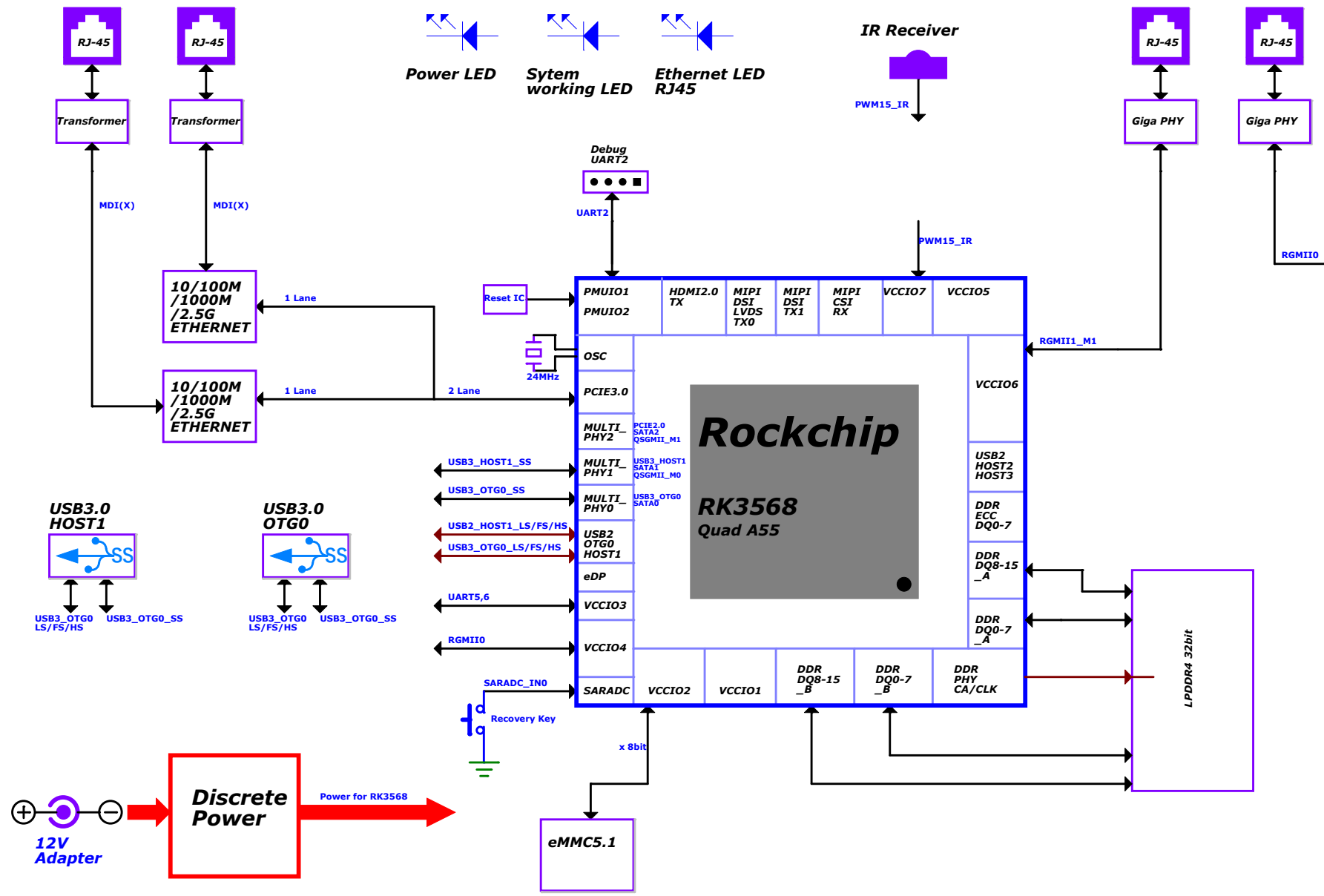
Project **Lunzn\_r68s**

Size A4 Document Number  
**01.Cover Page**

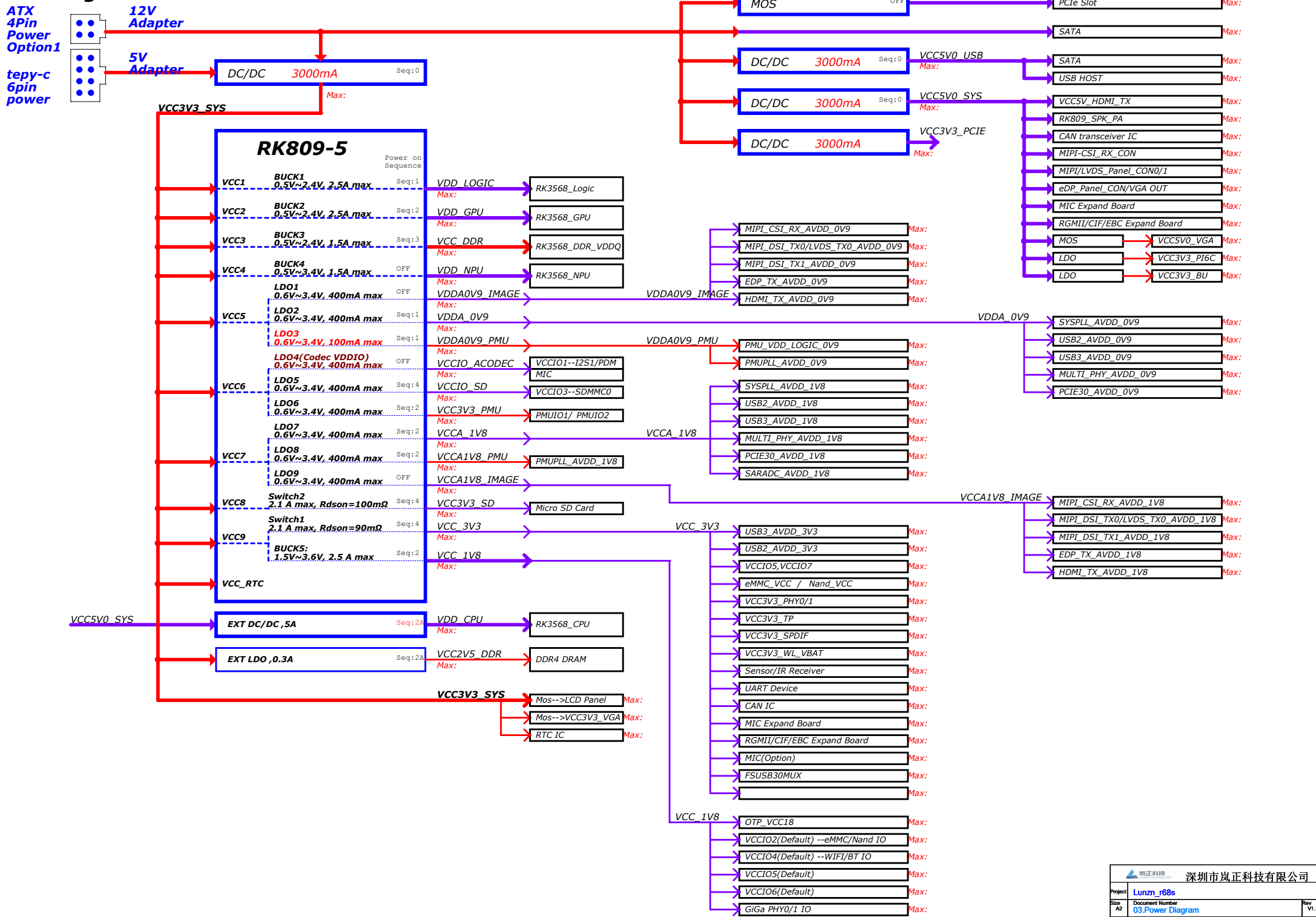
Rev  
V1.1

Date: Friday, May 06, 2022 Sheet 1 of 29

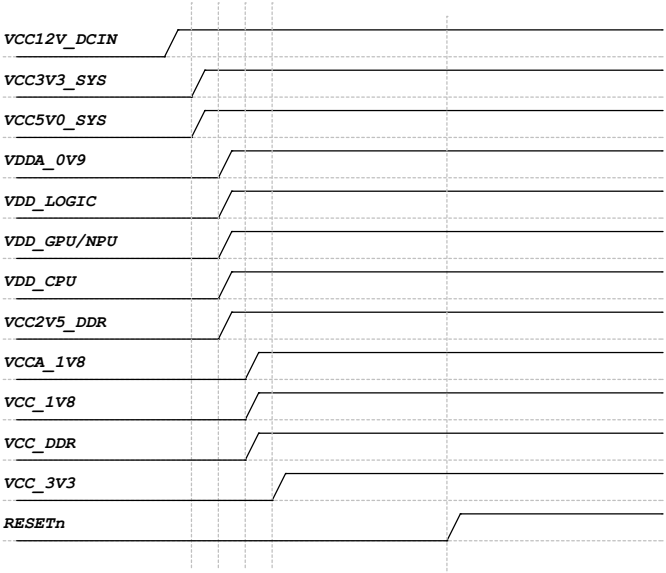
Lunzn r68s Block Diagram



### ***Power Diagram***



# Power Sequence



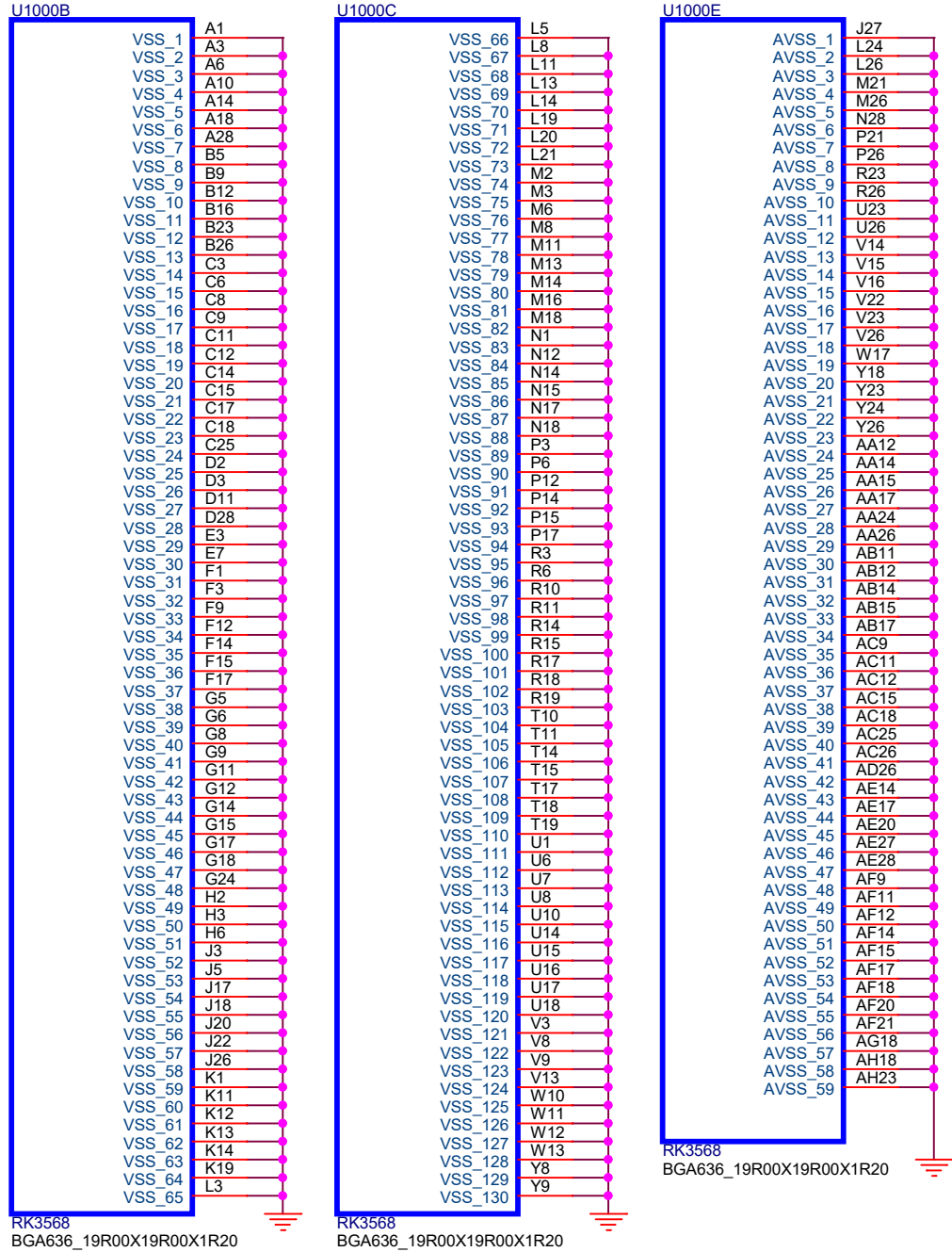
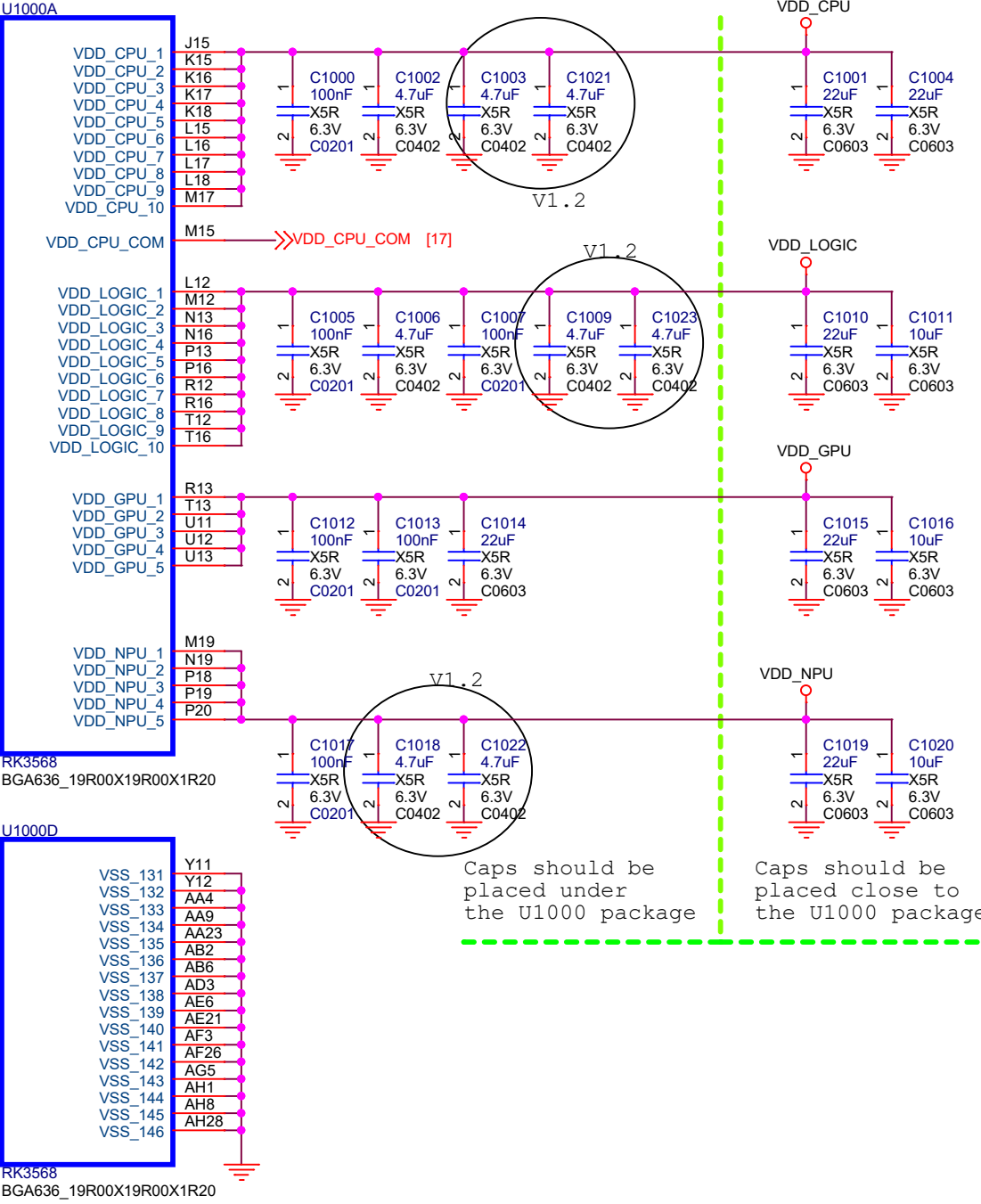
Power Supply	Channel	Supply Limit	Power Name	Time Slot	Default Voltage
VCC12V_DCIN	BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V
VCC12V_DCIN	BUCK	3.0A	VCC5V0_SYS	Slot:0	5.2V
VCC3V3_SYS			VCC3V3_PMUIO	Slot:0	3.3V
VCC3V3_SYS	LDO	0.3A	VDDA_0V9	Slot:1	0.9V
VCC3V3_SYS	BUCK	1.5A	VDD_LOGIC	Slot:1	0.9V
VCC3V3_SYS	BUCK	3.0A	VDD_GPU/NPU	Slot:1	0.9V
VCC3V3_SYS	BUCK	5.0A	VDD_CPU	Slot:1	0.9V
VCC3V3_SYS	LDO	0.3A	VCC2V5_DDR	Slot:1	2.5V
VCC3V3_SYS	LDO	0.5A	VCC_1V8	Slot:2	1.8V
VCC3V3_SYS	LDO	0.5A	VCCA_1V8	Slot:2	1.8V
VCC3V3_SYS	BUCK	1.5A	VCC_DDR	Slot:2	1.2V
VCC3V3_SYS	MOS	2A	VCC_3V3	Slot:3	DDR4 3.3V
VCC3V3_PMUIO	RESETn				

## IO Power Domain Map

Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC_3V3	VCC_3V3	3.3V	
PMUIO2	Pin W19	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO1	Pin H17	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO4	Pin J21	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCC_3V3	VCC_3V3	3.3V	

# RK3568\_ABCDE (Power&Gnd)



# RK3568\_F (DDR PHY)

U1000F

	DDR4	LPDDR4	DDR3	LPDDR3	
[20] LPDDR4_DQ0<X>	DDR DQ0 A	F2	DDR DQ0 A / DDR4 DQ0 A / LPDDR4 DQ0 A / DDR3 DQ0 / LPDDR3 DQ0		
[20] LPDDR4_DQ1<X>	DDR DQ1 A	E1	DDR DQ1 A / DDR4 DQ1 A / LPDDR4 DQ1 A / DDR3 DQ1 / LPDDR3 DQ1		
[20] LPDDR4_DQ2<X>	DDR DQ2 A	E2	DDR DQ2 A / DDR4 DQ2 A / LPDDR4 DQ2 A / DDR3 DQ2 / LPDDR3 DQ2		
[20] LPDDR4_DQ3<X>	DDR DQ3 A	D1	DDR DQ3 A / DDR4 DQ3 A / LPDDR4 DQ3 A / DDR3 DQ3 / LPDDR3 DQ3		
[20] LPDDR4_DQ4<X>	DDR DQ4 A	J1	DDR DQ4 A / DDR4 DQ4 A / LPDDR4 DQ4 A / DDR3 DQ4 / LPDDR3 DQ4		
[20] LPDDR4_DQ5<X>	DDR DQ5 A	J2	DDR DQ5 A / DDR4 DQ5 A / LPDDR4 DQ5 A / DDR3 DQ5 / LPDDR3 DQ5		
[20] LPDDR4_DQ6<X>	DDR DQ6 A	H1	DDR DQ6 A / DDR4 DQ6 A / LPDDR4 DQ6 A / DDR3 DQ6 / LPDDR3 DQ6		
[20] LPDDR4_DQ7<X>	DDR DQ7 A	H4	DDR DQ7 A / DDR4 DQ7 A / LPDDR4 DQ7 A / DDR3 DQ7 / LPDDR3 DQ7		
[20] LPDDR4_DM0<X>	DDR DM0 A	H5	DDR DM0 A / DDR4 DM0 A / LPDDR4 DM0 A / DDR3 DM0 / LPDDR3 DM0		
[20] LPDDR4_DQS0P<X>	DDR DQS0P A	G1	DDR DQS0P A / DDR4 DQS0P A / LPDDR4 DQS0P A / DDR3 DQS0P / LPDDR3 DQS0P		
[20] LPDDR4_DQS0N<X>	DDR DQS0N A	G2	DDR DQS0N A / DDR4 DQS0N A / LPDDR4 DQS0N A / DDR3 DQS0N / LPDDR3 DQS0N		
[20] LPDDR4_DQ8<X>	DDR DQ8 A	M1	DDR DQ8 A / DDR4 DQ8 A / LPDDR4 DQ8 A / DDR3 DQ8 / LPDDR3 DQ8		
[20] LPDDR4_DQ9<X>	DDR DQ9 A	N2	DDR DQ9 A / DDR4 DQ9 A / LPDDR4 DQ9 A / DDR3 DQ9 / LPDDR3 DQ9		
[20] LPDDR4_DQ10<X>	DDR DQ10 A	L7	DDR DQ10 A / DDR4 DQ10 A / LPDDR4 DQ10 A / DDR3 DQ10 / LPDDR3 DQ10		
[20] LPDDR4_DQ11<X>	DDR DQ11 A	L6	DDR DQ11 A / DDR4 DQ11 A / LPDDR4 DQ11 A / DDR3 DQ11 / LPDDR3 DQ11		
[20] LPDDR4_DQ12<X>	DDR DQ12 A	K2	DDR DQ12 A / DDR4 DQ12 A / LPDDR4 DQ12 A / DDR3 DQ12 / LPDDR3 DQ12		
[20] LPDDR4_DQ13<X>	DDR DQ13 A	J6	DDR DQ13 A / DDR4 DQ13 A / LPDDR4 DQ13 A / DDR3 DQ13 / LPDDR3 DQ13		
[20] LPDDR4_DQ14<X>	DDR DQ14 A	J7	DDR DQ14 A / DDR4 DQ14 A / LPDDR4 DQ14 A / DDR3 DQ14 / LPDDR3 DQ14		
[20] LPDDR4_DQ15<X>	DDR DQ15 A	L4	DDR DQ15 A / DDR4 DQ15 A / LPDDR4 DQ15 A / DDR3 DQ15 / LPDDR3 DQ15		
[20] LPDDR4_DM1<X>	DDR DM1 A	J4	DDR DM1 A / DDR4 DM1 A / LPDDR4 DM1 A / DDR3 DM1 / LPDDR3 DM1		
[20] LPDDR4_DQS1P<X>	DDR DQS1P A	L2	DDR DQS1P A / DDR4 DQS1P A / LPDDR4 DQS1P A / DDR3 DQS1P / LPDDR3 DQS1P		
[20] LPDDR4_DQS1N<X>	DDR DQS1N A	L1	DDR DQS1N A / DDR4 DQS1N A / LPDDR4 DQS1N A / DDR3 DQS1N / LPDDR3 DQS1N		
[20] LPDDR4_DQ0<X>	DDR DQ0 B	B10	DDR DQ0 B / DDR4 DQ0 B / LPDDR4 DQ0 B / DDR3 DQ0 / LPDDR3 DQ0		
[20] LPDDR4_DQ1<X>	DDR DQ1 B	A9	DDR DQ1 B / DDR4 DQ1 B / LPDDR4 DQ1 B / DDR3 DQ1 / LPDDR3 DQ1		
[20] LPDDR4_DQ2<X>	DDR DQ2 B	D12	DDR DQ2 B / DDR4 DQ2 B / LPDDR4 DQ2 B / DDR3 DQ2 / LPDDR3 DQ2		
[20] LPDDR4_DQ3<X>	DDR DQ3 B	E12	DDR DQ3 B / DDR4 DQ3 B / LPDDR4 DQ3 B / DDR3 DQ3 / LPDDR3 DQ3		
[20] LPDDR4_DQ4<X>	DDR DQ4 B	A12	DDR DQ4 B / DDR4 DQ4 B / LPDDR4 DQ4 B / DDR3 DQ4 / LPDDR3 DQ4		
[20] LPDDR4_DQ5<X>	DDR DQ5 B	D15	DDR DQ5 B / DDR4 DQ5 B / LPDDR4 DQ5 B / DDR3 DQ5 / LPDDR3 DQ5		
[20] LPDDR4_DQ6<X>	DDR DQ6 B	E15	DDR DQ6 B / DDR4 DQ6 B / LPDDR4 DQ6 B / DDR3 DQ6 / LPDDR3 DQ6		
[20] LPDDR4_DQ7<X>	DDR DQ7 B	E14	DDR DQ7 B / DDR4 DQ7 B / LPDDR4 DQ7 B / DDR3 DQ7 / LPDDR3 DQ7		
[20] LPDDR4_DM0<X>	DDR DM0 B	D14	DDR DM0 B / DDR4 DM0 B / LPDDR4 DM0 B / DDR3 DM0 / LPDDR3 DM0		
[20] LPDDR4_DQS0P<X>	DDR DQS0P B	BA11	DDR DQS0P B / DDR4 DQS0P B / LPDDR4 DQS0P B / DDR3 DQS0P / LPDDR3 DQS0P		
[20] LPDDR4_DQS0N<X>	DDR DQS0N B	BB11	DDR DQS0N B / DDR4 DQS0N B / LPDDR4 DQS0N B / DDR3 DQS0N / LPDDR3 DQS0N		
[20] LPDDR4_DQ8<X>	DDR DQ8 B	A16	DDR DQ8 B / DDR4 DQ8 B / LPDDR4 DQ8 B / DDR3 DQ8 / LPDDR3 DQ8		
[20] LPDDR4_DQ9<X>	DDR DQ9 B	B17	DDR DQ9 B / DDR4 DQ9 B / LPDDR4 DQ9 B / DDR3 DQ9 / LPDDR3 DQ9		
[20] LPDDR4_DQ10<X>	DDR DQ10 B	A17	DDR DQ10 B / DDR4 DQ10 B / LPDDR4 DQ10 B / DDR3 DQ10 / LPDDR3 DQ10		
[20] LPDDR4_DQ11<X>	DDR DQ11 B	B18	DDR DQ11 B / DDR4 DQ11 B / LPDDR4 DQ11 B / DDR3 DQ11 / LPDDR3 DQ11		
[20] LPDDR4_DQ12<X>	DDR DQ12 B	B19	DDR DQ12 B / DDR4 DQ12 B / LPDDR4 DQ12 B / DDR3 DQ12 / LPDDR3 DQ12		
[20] LPDDR4_DQ13<X>	DDR DQ13 B	A13	DDR DQ13 B / DDR4 DQ13 B / LPDDR4 DQ13 B / DDR3 DQ13 / LPDDR3 DQ13		
[20] LPDDR4_DQ14<X>	DDR DQ14 B	D17	DDR DQ14 B / DDR4 DQ14 B / LPDDR4 DQ14 B / DDR3 DQ14 / LPDDR3 DQ14		
[20] LPDDR4_DQ15<X>	DDR DQ15 B	B14	DDR DQ15 B / DDR4 DQ15 B / LPDDR4 DQ15 B / DDR3 DQ15 / LPDDR3 DQ15		
[20] LPDDR4_DM1<X>	DDR DM1 B	E17	DDR DM1 B / DDR4 DM1 B / LPDDR4 DM1 B / DDR3 DM1 / LPDDR3 DM1		
[20] LPDDR4_DQS1P<X>	DDR DQS1P B	BB15	DDR DQS1P B / DDR4 DQS1P B / LPDDR4 DQS1P B / DDR3 DQS1P / LPDDR3 DQS1P		
[20] LPDDR4_DQS1N<X>	DDR DQS1N B	BA15	DDR DQS1N B / DDR4 DQS1N B / LPDDR4 DQS1N B / DDR3 DQS1N / LPDDR3 DQS1N		
X	DDR ECC DQ0	DDR4 ECC DQ0	/	DDR3 ECC DQ0	
X	DDR ECC DQ1	DDR4 ECC DQ1	/	DDR3 ECC DQ1	
X	DDR ECC DQ2	DDR4 ECC DQ2	/	DDR3 ECC DQ2	
X	DDR ECC DQ3	DDR4 ECC DQ3	/	DDR3 ECC DQ3	
X	DDR ECC DQ4	DDR4 ECC DQ4	/	DDR3 ECC DQ4	
X	DDR ECC DQ5	DDR4 ECC DQ5	/	DDR3 ECC DQ5	
X	DDR ECC DQ6	DDR4 ECC DQ6	/	DDR3 ECC DQ6	
X	DDR ECC DQ7	DDR4 ECC DQ7	/	DDR3 ECC DQ7	
X	DDR ECC DM	DDR4 ECC DM	/	DDR3 ECC DM	
X	DDR ECC DQS	DDR4 ECC DQS	/	DDR3 ECC DQS	
X	DDR ECC DQS	DDR4 ECC DQS	/	DDR3 ECC DQS	

RR3568  
BGA636\_19R00X19R00X1R20

RK3568  
BGA636\_19R00X19R00X1R20

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	LPDDR3_DQ15
DDR4_A1	LPDDR4_CLKN_B	DDR3_A8	LPDDR3_DQ14
DDR4_A2	LPDDR4_CKE1_A	DDR3_A7	LPDDR3_DQ13
DDR4_A3	LPDDR4_CKE1_A	DDR3_A6	LPDDR3_DQ12
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3
DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2
DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	LPDDR3_A0
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9
DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	LPDDR3_A0
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	LPDDR3_A8
DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	LPDDR3_A0
DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0
DDR4_A14	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5
DDR4_A15	LPDDR4_A2_A	DDR3_A0	LPDDR3_A5
DDR4_A16	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7
DDR4_A17	LPDDR4_CKE1_B	DDR3_CASn	LPDDR3_A7
DDR4_BA0	LPDDR4_A2_B	DDR3_A1	LPDDR3_A7
DDR4_BA1	LPDDR4_A1_B	DDR3_A12	LPDDR3_A4
DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_Wen	LPDDR3_A0
DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	LPDDR3_A0
DDR4_CKE	LPDDR4_CKE0_A	DDR3_CASn	LPDDR3_CASn
DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP
DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_CS1n
DDR4_CS2n	LPDDR4_CS2n_B	DDR3_CS2n	LPDDR3_CS2n
DDR4_CS3n	LPDDR4_CS3n_B	DDR3_CS3n	LPDDR3_CS3n
DDR4_RESETh	LPDDR4_RESETh	DDR3_RESETh	LPDDR3_RESETh

Note: Sequences can not be swap

DDR\_RZQ

DDR\_VREFOUT

DDR3L	=1.35V	DDRRPHY_VDDQ_1
DDR3	=1.5V	DDRRPHY_VDDQ_2
DDR4	=1.2V	DDRRPHY_VDDQ_3
LPDDR3	=1.2V	DDRRPHY_VDDQ_4
LPDDR4	=1.1V	DDRRPHY_VDDQ_5
LPDDR4x	=1.1V	DDRRPHY_VDDQ_6
		DDRRPHY_VDDQ_7
		DDRRPHY_VDDQ_8

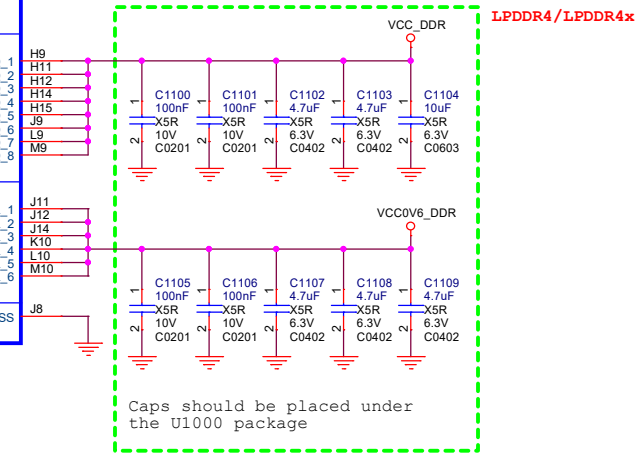
Note:  
Except DDR3, other DQ sequences  
can not be swap

DDR\_AVSS

B6	AC0	LPDDR4_CLKP_B [20]
F5	AC2	LPDDR4_A1_A [20]
B1	AC3	LPDDR4_CKE1_A [20]
D9	AC4	LPDDR4_A3_B [20]
B7	AC5	LPDDR4_A5_B [20]
A7	AC6	LPDDR4_A1_B [20]
A8	AC7	LPDDR4_ODT0_CA_B [20]
C1	AC8	LPDDR4_ODT0_CA_A [20]
A5	AC9	LPDDR4_CLKN_B [20]
D6	AC10	LPDDR4_CKE0_B [20]
C2	AC11	LPDDR4_A0_A [20]
C4	AC12	LPDDR4_A3_A [20]
B8	AC13	LPDDR4_A0_B [20]
C5	AC14	LPDDR4_A4_A [20]
E4	AC15	LPDDR4_A2_A [20]
D5	AC16	LPDDR4_A5_A [20]
E6	AC17	LPDDR4_CKE1_B [20]
E11	AC18	LPDDR4_A2_B [20]
E9	AC19	LPDDR4_A4_B [20]
F8	AC20	LPDDR4_CKE0_A [20]
F7	AC21	LPDDR4_CKE0_A [20]
B3	AC22	LPDDR4_CKE0_A [20]
B4	AC23	LPDDR4_CLKP_A [20]
A4	AC24	LPDDR4_CLKN_A [20]
A2	AC25	LPDDR4_CS0n_A [20]
B2	AC26	LPDDR4_CS1n_A [20]
E8	AC27	LPDDR4_CS1n_B [20]
D8	AC28	LPDDR4_CS0n_B [20]
F11	AC29	LPDDR4_RESETh [20]

For DDR4/DDR3/LPDDR3 mode,  
a 120 ohm +/-1% tolerance external  
resistor must be connected between  
the DDR\_RZQ pin and VSS pin

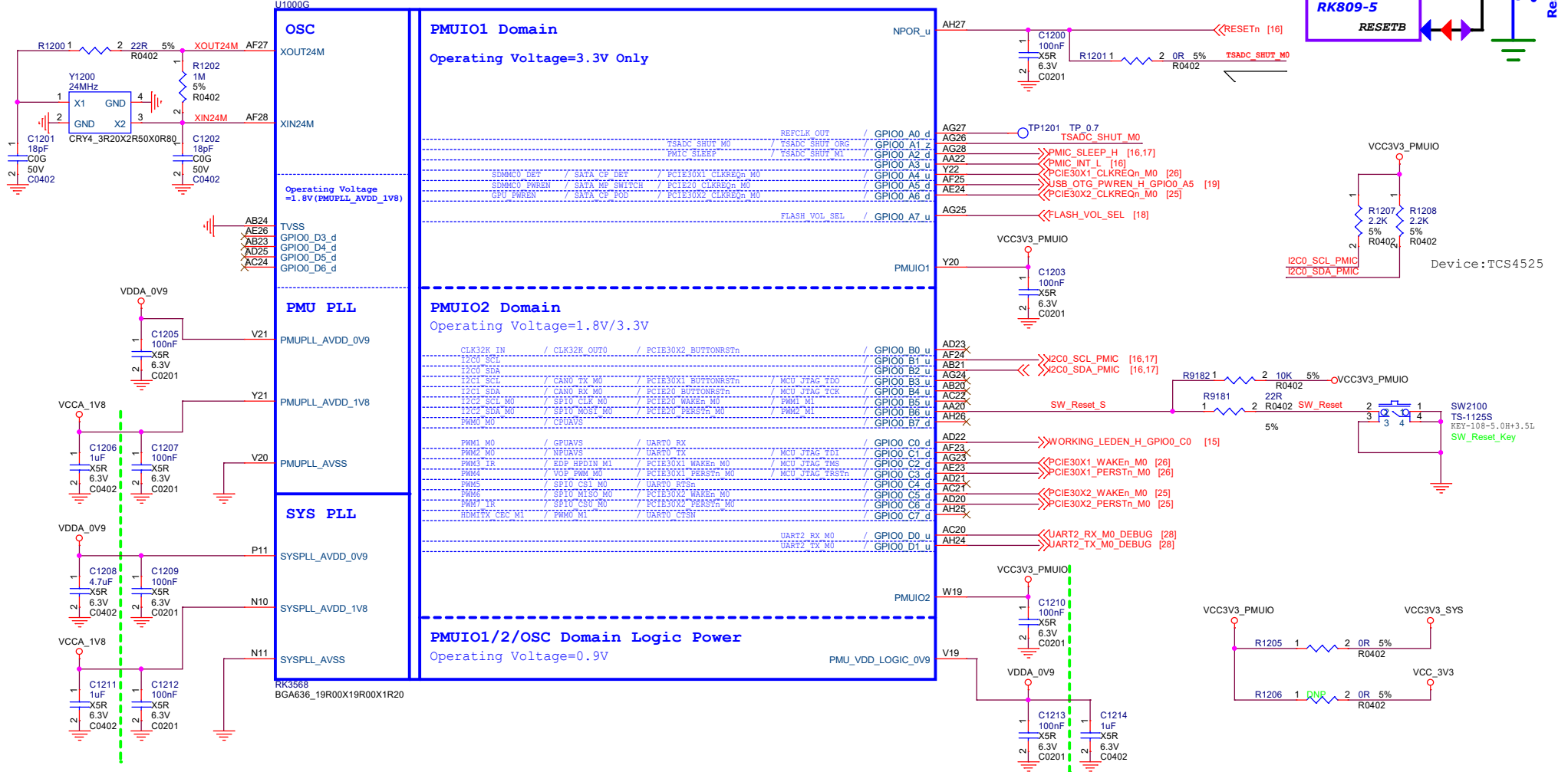
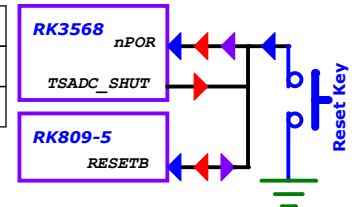
For LPDDR4/LPDDR4x mode,  
a 120 ohm +/-1% tolerance external  
resistor must be connected between  
the DDR\_RZQ pin and DDRPHY\_VDDQ pin



Caps should be placed under  
the U1000 package

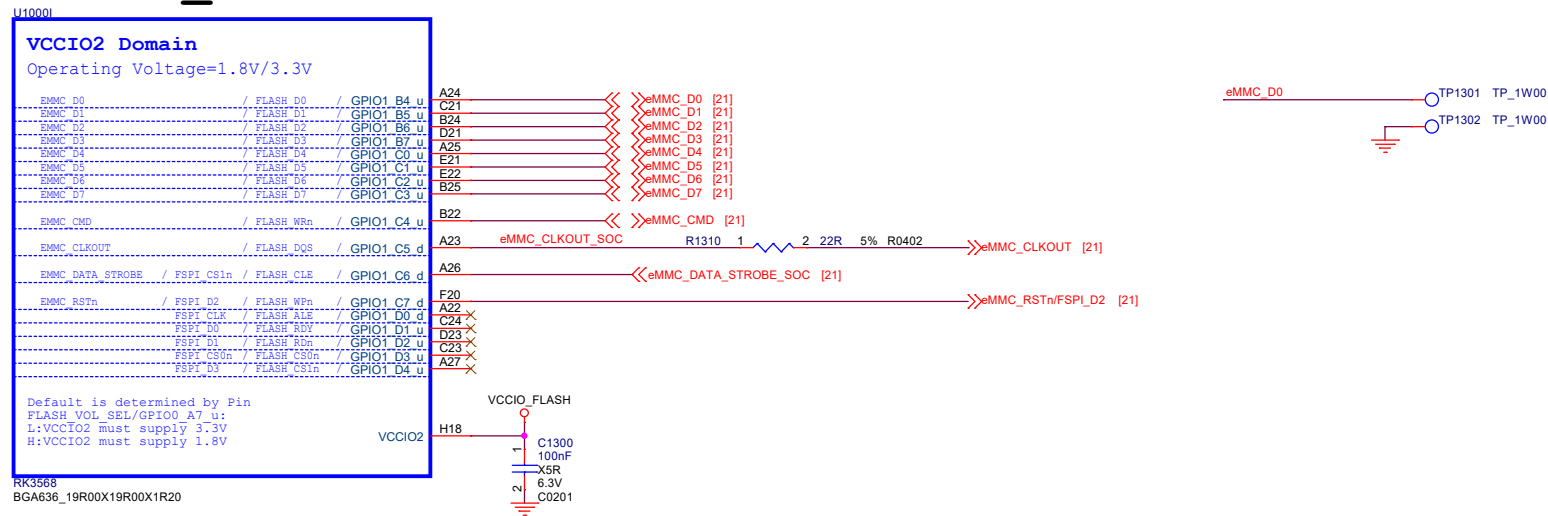
# RK3568\_G (OSC/PLL/PMUIO1/2)

- Reset Key Control Path
- TSADC\_SHUT Control Path
- RK809-5 Control Path

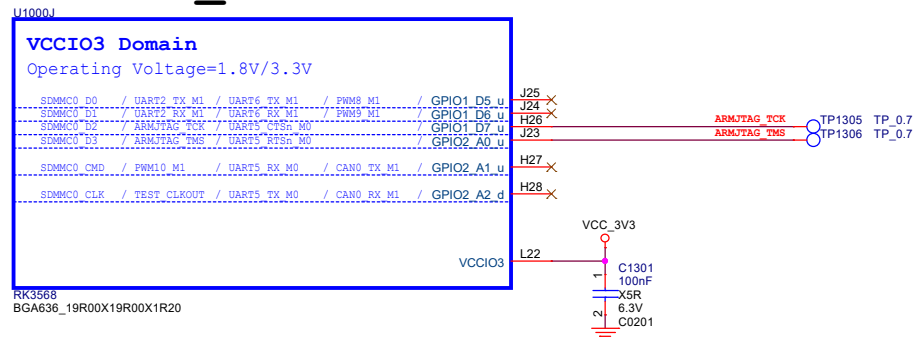


**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

# RK3568\_I (VCCIO2 Domain)



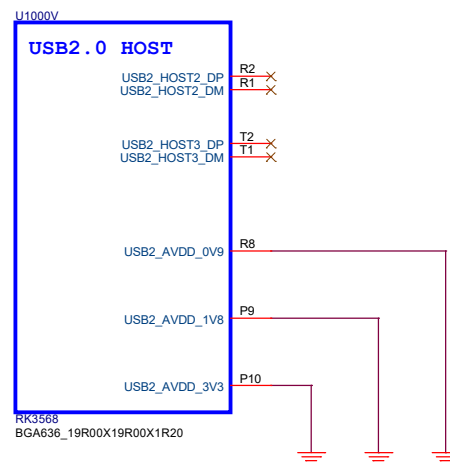
# RK3568\_J (VCCIO3 Domain)



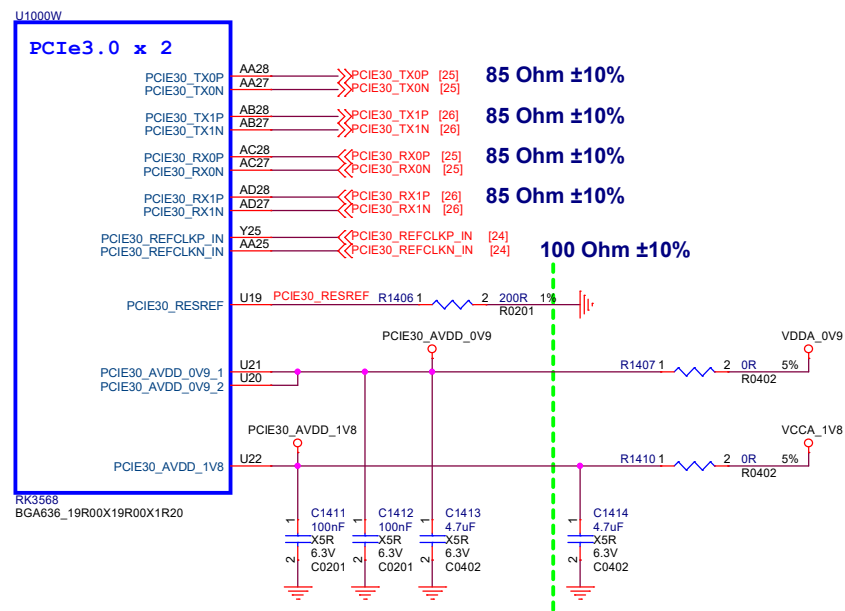
## Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

## RK3568 V (USB2.0 HOST)

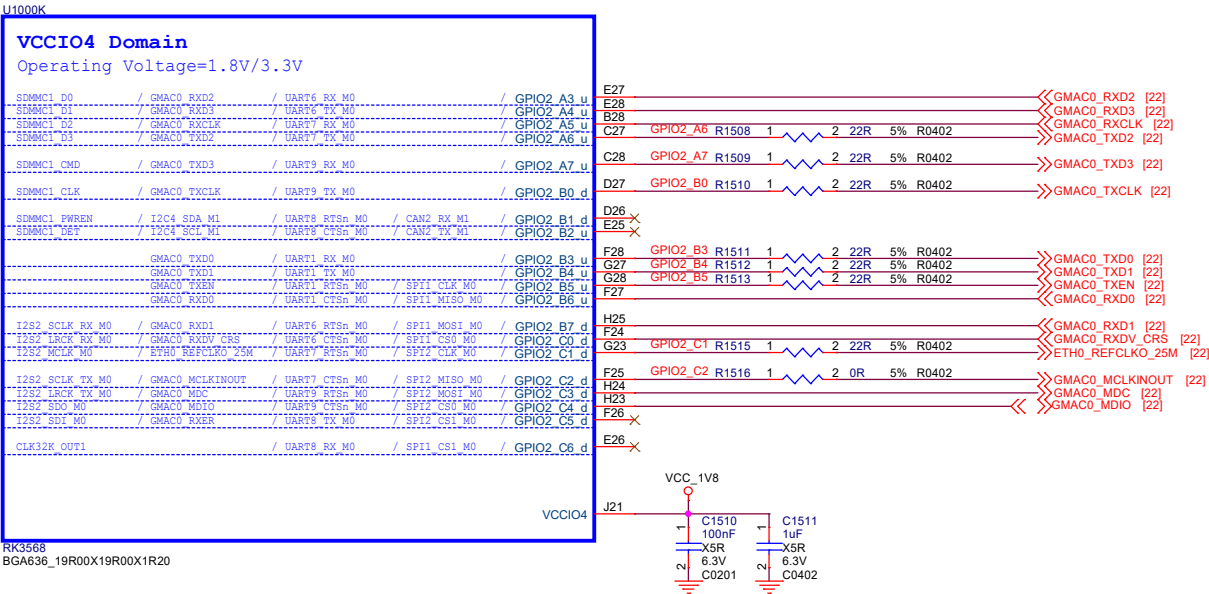


**RK3568 W (PCIe3.0 x2)**

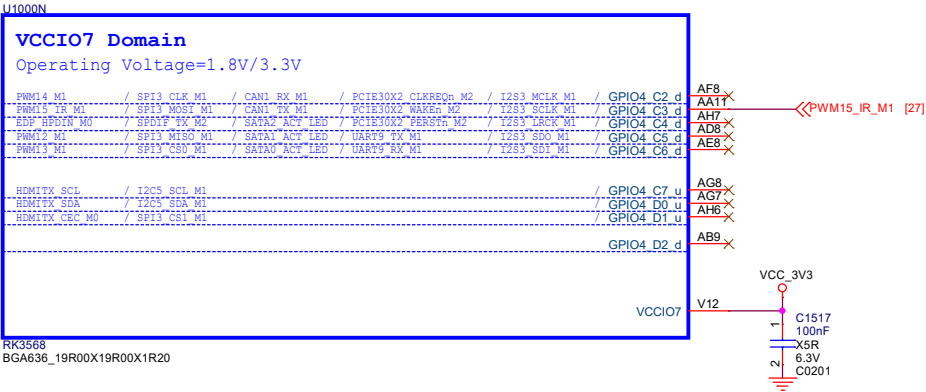


Caps of between dashed green lines and U1000  
should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

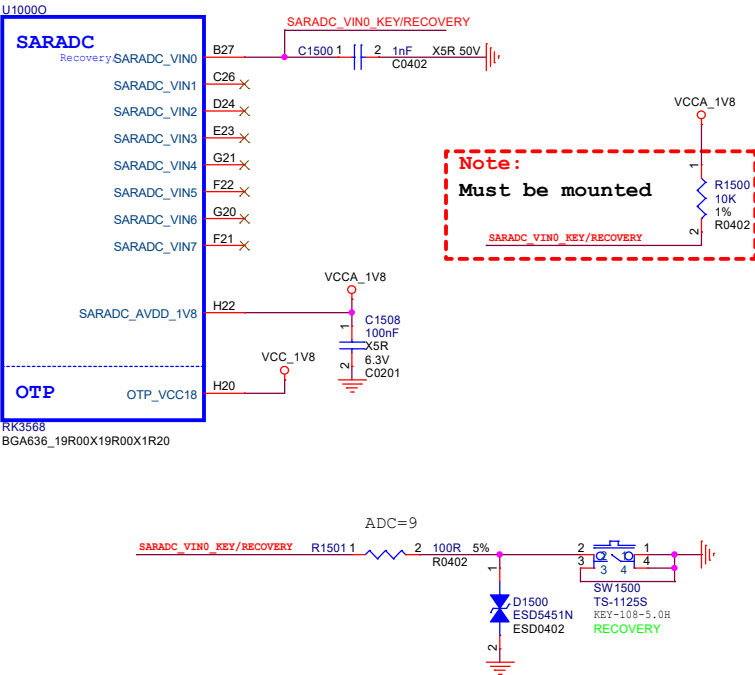
RK3568\_K (VCCIO4 Domain)



RK3568\_N (VCCIO7 Domain)

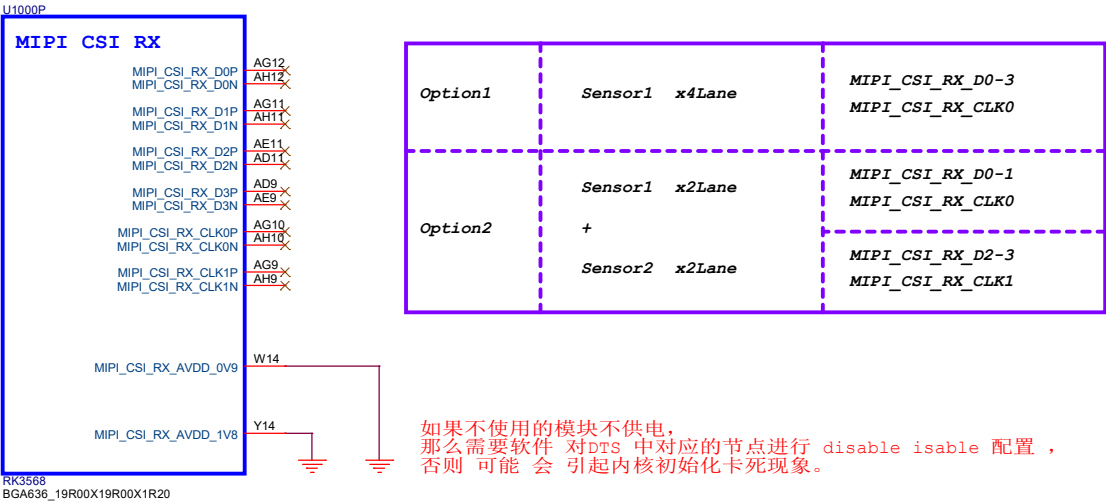


RK3568\_O (SARADC/OTP)



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3568\_P (MIPI\_CSI\_RX)

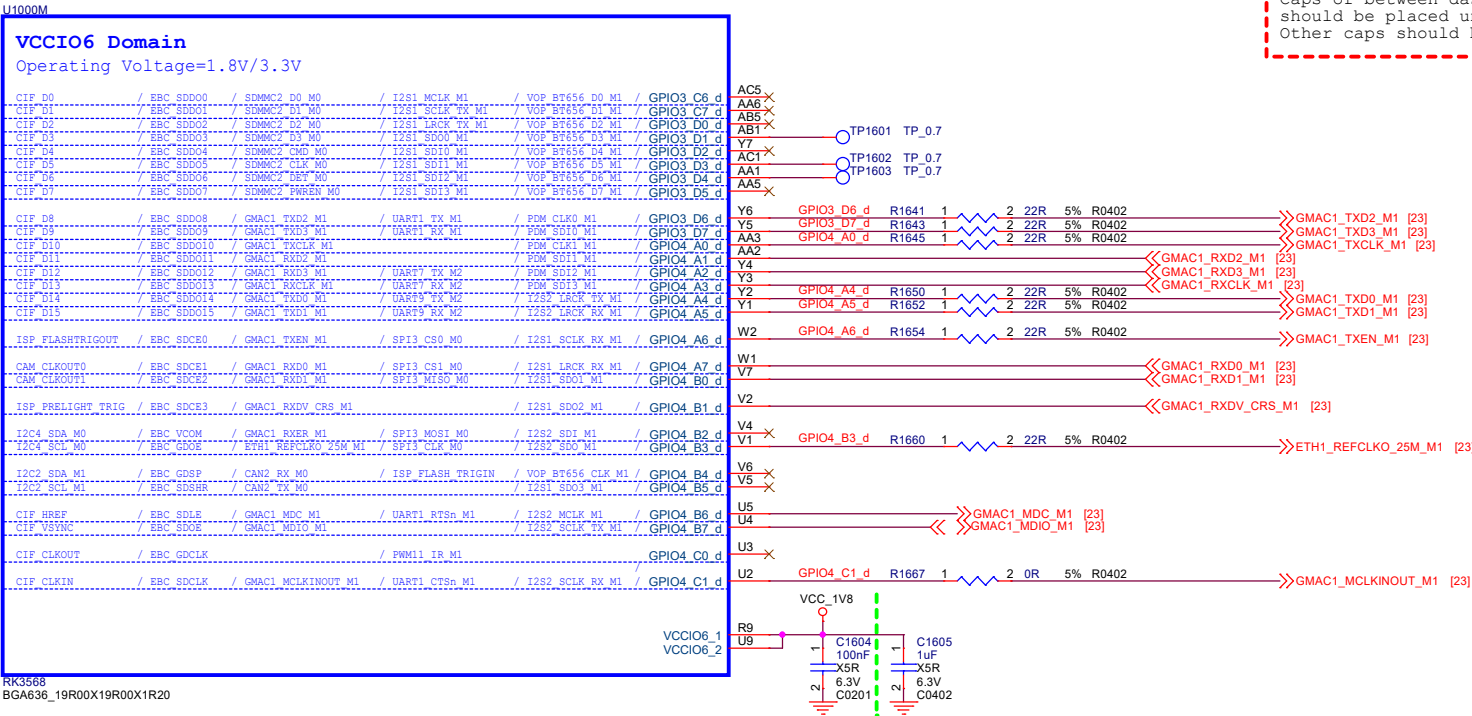


如果不使用的模块不供电，那么需要软件 对DTS 中对应的节点进行 disable isable 配置，否则 可能 会引起内核初始化卡死现象。

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

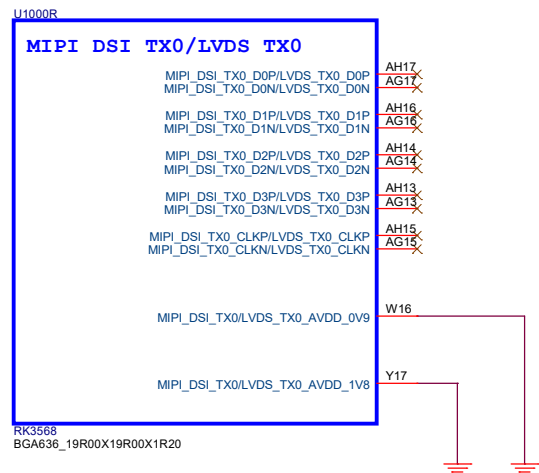
Support BT601 YCbCr 422 8bit input  
Support BT656 YCbCr 422 8bit input  
Support RAW 8/10/12bit input  
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling  
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

RK3568\_M (VCCIO6 Domain)



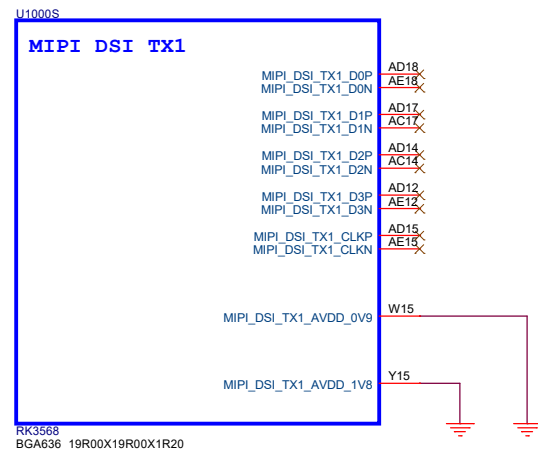
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

## RK3568\_R(MIPI\_DSI\_TX0/LVDS\_TX0)



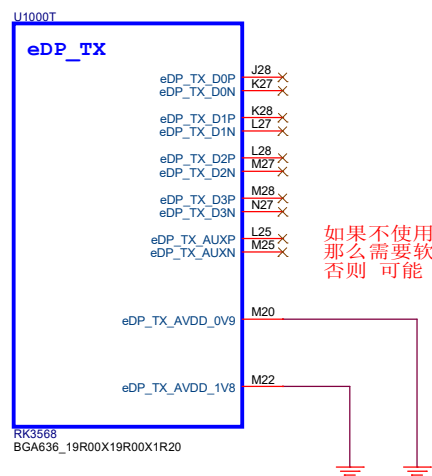
如果不使用的模块不供电，  
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，  
否则 可能 会 引起内核初始化卡死现象。

## RK3568\_S(MIPI\_DSI\_TX1)



如果不使用的模块不供电，  
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，  
否则 可能 会 引起内核初始化卡死现象。

## RK3568\_T(eDP TX)

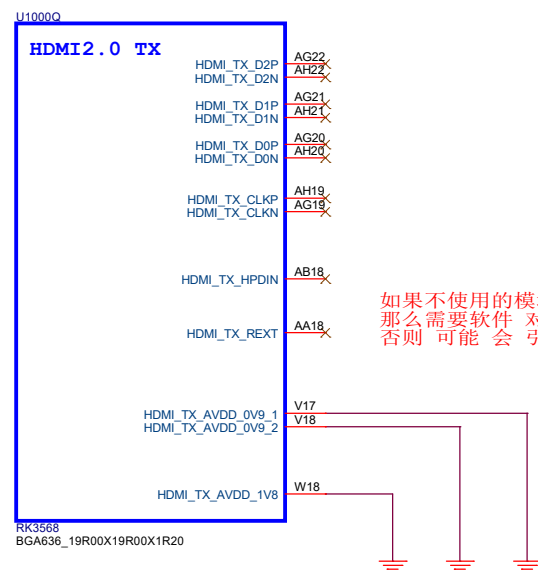


如果不使用的模块不供电，  
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，  
否则 可能 会 引起内核初始化卡死现象。

### Note:

Caps of between dashed green lines and U1000  
should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

## RK3568\_Q(HDMI2.0 TX)



如果不使用的模块不供电，  
那么需要软件 对DTS 中对应的节点进行 disable isable 配置 ，  
否则 可能 会 引起内核初始化卡死现象。

RK3568\_L (VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREQn M1	/ I2S1 LRCK TX M2	/ GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDI0 M2	/ GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0		/ SDMMC2 DET M1	/ GPIO3 A7 d
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLK0 25M M0		/ SDMMC2 PWREN M1	/ GPIO3 B0 d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDI0 M2	/ GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ I2C5 SDA M0	/ PDM SDI1 M2	/ GPIO3 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
LCDC B23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d

VCCIO5\_1  
VCCIO5\_2

AG6  
AD7  
AC8  
AC7  
AF5  
AF6  
AD6  
AH5  
  
AH4  
  
AB8  
AE5  
AG4  
AF4  
AH3  
AG3  
AH2  
AG2  
  
AG1  
AF2  
AF1  
AE1  
AE2  
AE3  
AD4  
AD2  
  
AD1  
AA7  
AC4  
  
AC3  
AC2  
  
V10  
V11

RK3568  
BGA636\_19R00X19R00X1R20

Note:  
Caps of between dashed green lines and U1000  
should be placed under the U1000 package

# RK3568\_H (VCCIO1 Domain)

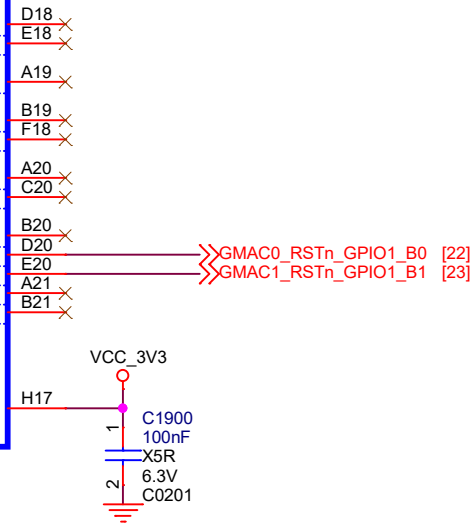
U1000H

## VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3 SDA M0	/ UART3 RX M0	/ CAN1 RX M0	/ AUDIOPWM LOUT P	/ ACODEC ADC DATA	/ GPIO1 A0 u
I2C3 SCL M0	/ UART3 TX M0	/ CAN1 TX M0	/ AUDIOPWM LOUT N	/ ACODEC ADC CLK	/ GPIO1 A1 u
I2S1 MCLK M0	/ UART3 RTSn M0	/ SCR CLK	/ PCIE30X1 PERSTn M2		/ GPIO1 A2 d
I2S1 SCLK TX M0	/ UART3 CTSn M0	/ SCR IO	/ PCIE30X1 WAKEn M2	/ ACODEC DAC CLK	/ GPIO1 A3 d
I2S1 SCLK RX M0	/ UART4 RX M0	/ PDM CLK1 M0	/ SPDIF TX M0		/ GPIO1 A4 d
I2S1 LRCK TX M0	/ UART4 RTSn M0	/ SCR RST	/ PCIE30X1 CLKREQn M2	/ ACODEC DAC SYNC	/ GPIO1 A5 d
I2S1 LRCK RX M0	/ UART4 TX M0	/ PDM CLK0 M0	/ AUDIOPWM ROUT P		/ GPIO1 A6 d
I2S1 SDO0 M0	/ UART4 CTSn M0	/ SCR DET	/ AUDIOPWM ROUT N	/ ACODEC DAC DATAL	/ GPIO1 A7 d
I2S1 SDO1 M0	/ I2S1 SDI3 M0	/ PDM SDI3 M0	/ PCIE20 CLKREQn M2	/ ACODEC DAC DATAR	/ GPIO1 B0 d
I2S1 SDO2 M0	/ I2S1 SDI2 M0	/ PDM SDI2 M0	/ PCIE20 WAKEn M2	/ ACODEC ADC SYNC	/ GPIO1 B1 d
I2S1 SDO3 M0	/ I2S1 SDI1 M0	/ PDM SDI1 M0	/ PCIE20 PERSTn M2		/ GPIO1 B2 d
	/ I2S1 SDI0 M0	/ PDM SDI0 M0			/ GPIO1 B3 d

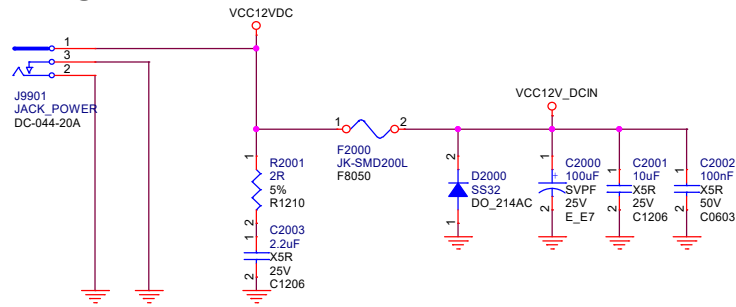
RK3568  
BGA636\_19R00X19R00X1R20



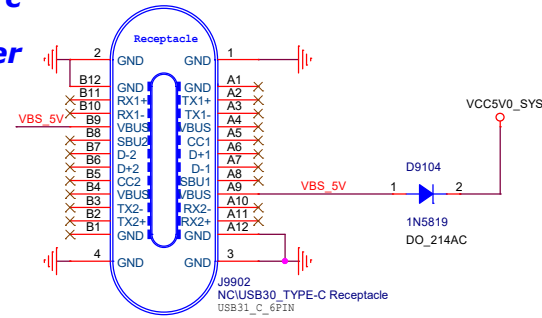
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

## 12V/3A DCIN

DC044B  
Power  
Option1

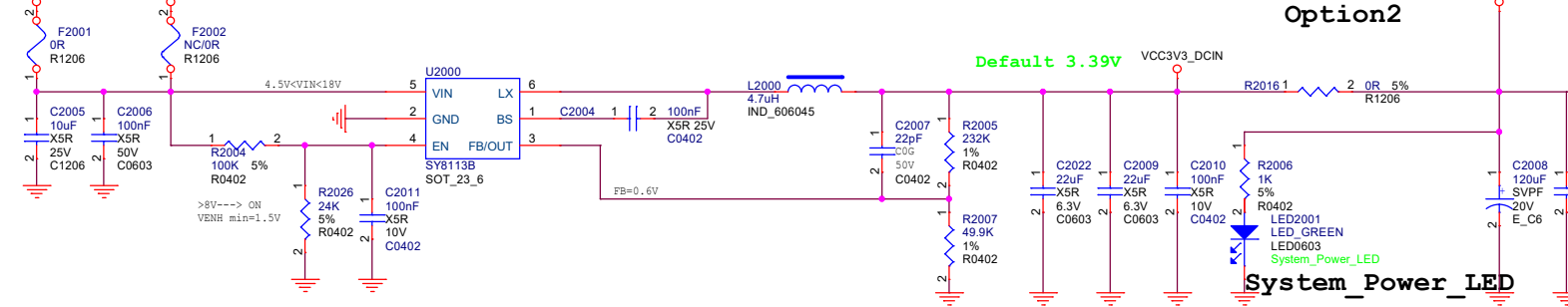


tepy-c  
6pin  
power



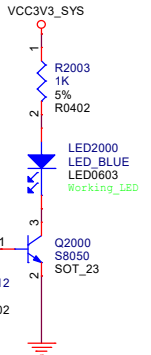
## VCC3V3\_SYS

VCC12V\_DCIN VCC5V0\_SYS

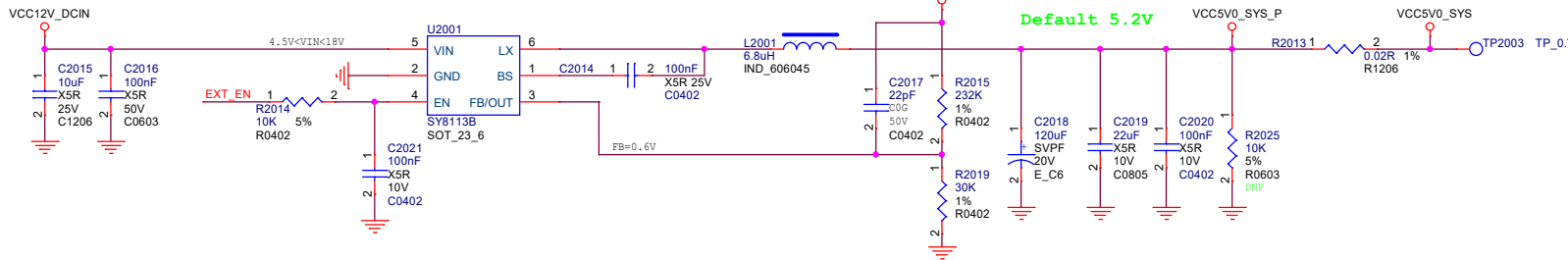


Option2

Working LED

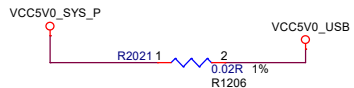


## VCC5V0\_SYS



WORKING\_LEDEN\_H\_GPIO0\_C0 [7]  
EXT\_EN [16]

## VCC5V0\_USB

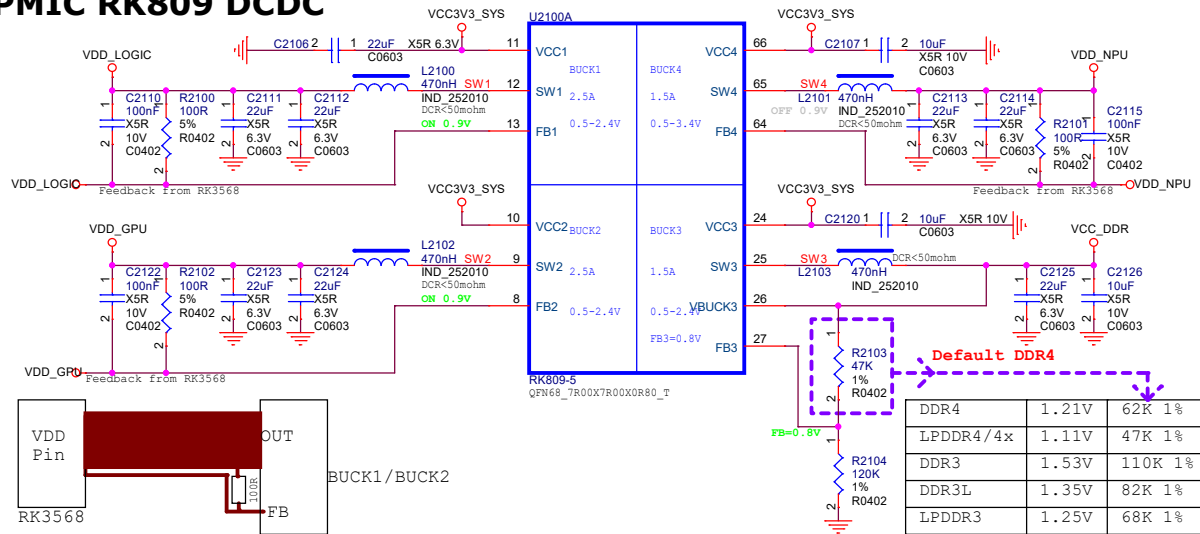


Project		Lunzn_r68s	
Size		Document Number	
A3		15.Power_DC IN	
Date:		Friday, May 06, 2022	
Sheet		15 of 29	
Rev		V1.1	

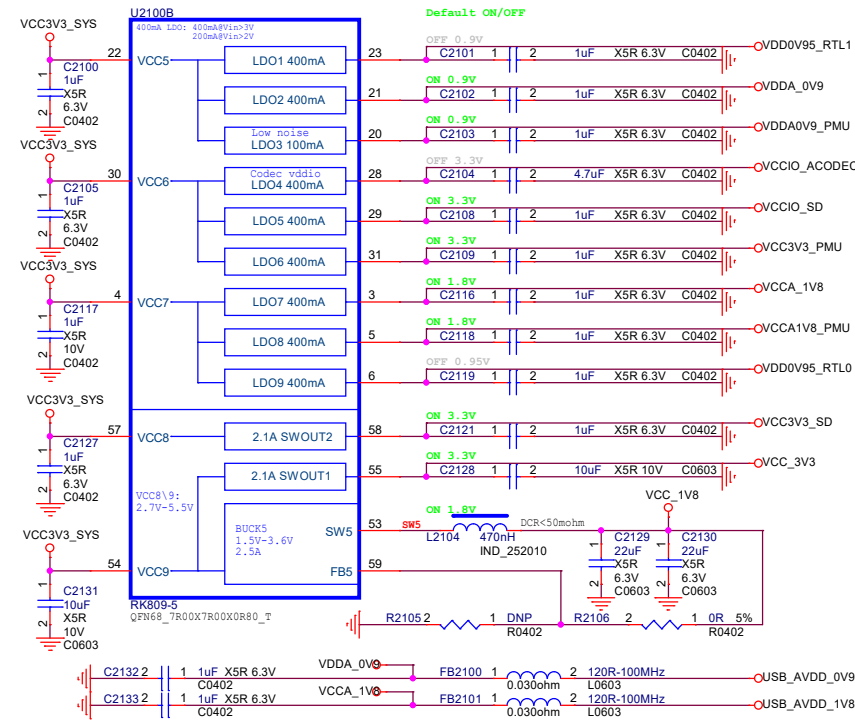
>>>I2C0\_SCL\_PMIC [7,17]  
>>>I2C0\_SDA\_PMIC [7,17]  
>>>PMIC\_INT\_L [7]  
>>>PMIC\_SLEEP\_H [7,17]  
  
>>>RESETn [7]  
  
>>>RK809\_PWRON

>>>EXT\_EN [15]

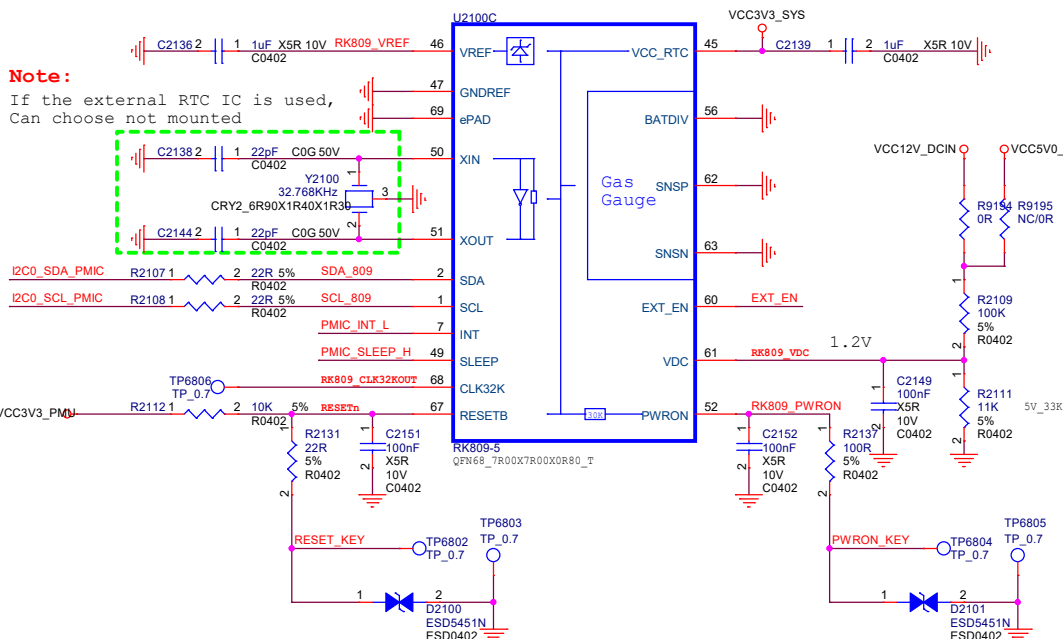
## PMIC RK809 DCDC



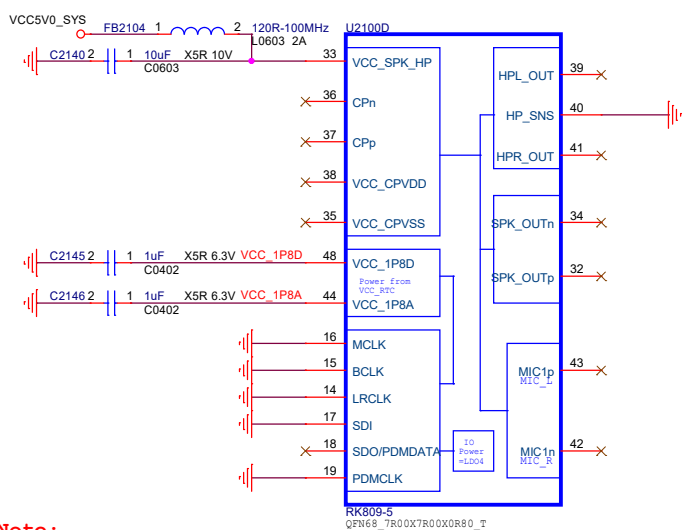
## PMIC RK809 LDO



## PMIC RK809 Managerment



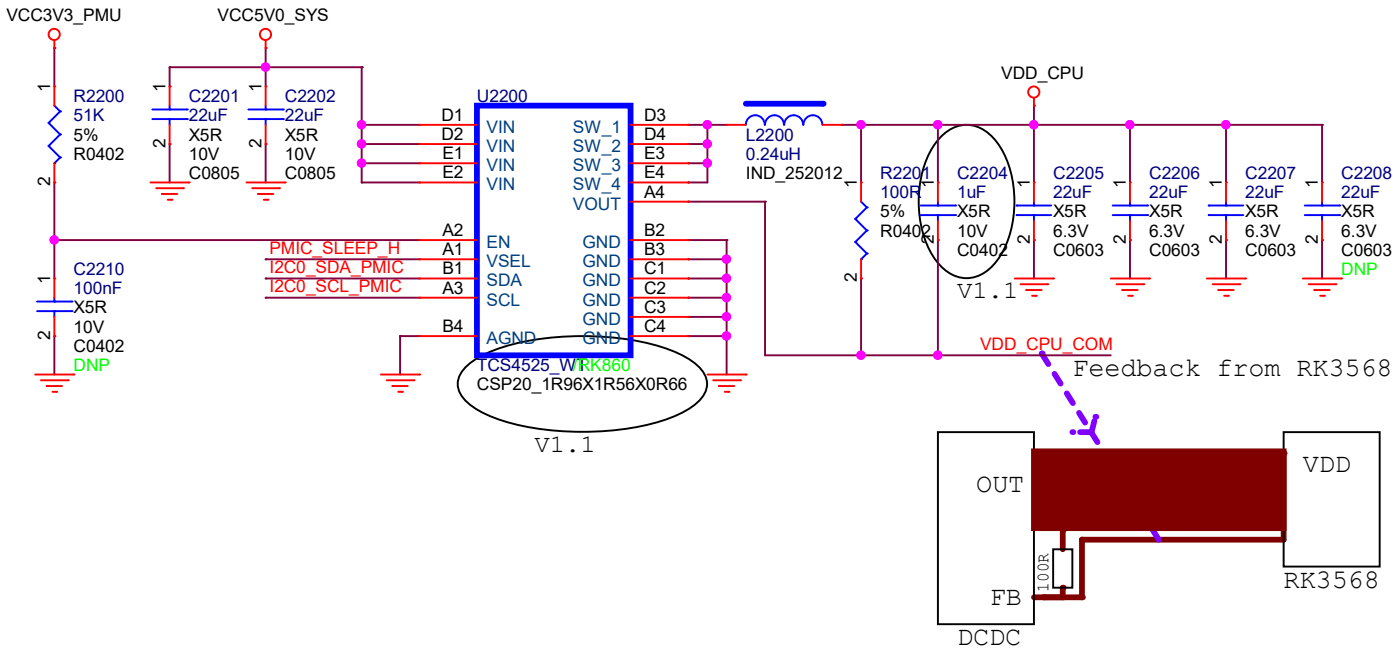
## PMIC RK809 CODEC



**Note:**

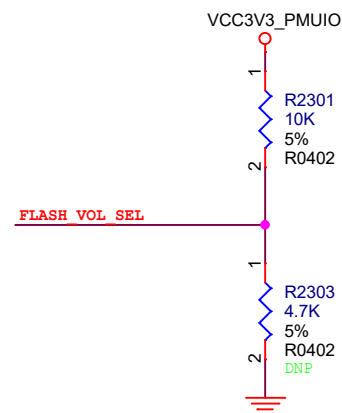
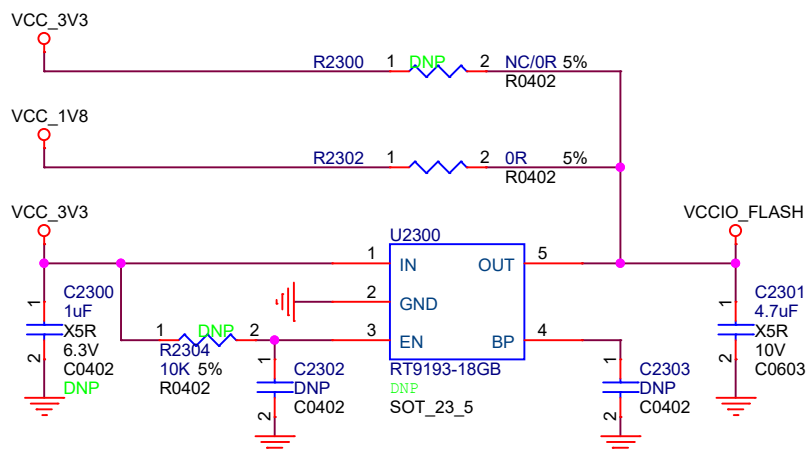
If RK809-5 codec is not used,  
then Pin 14,15,16,17,19,40 Tie VSS  
Pin 18,36,37,38,39,41,34,32,43,42  
Leave floating

# VDD\_CPU

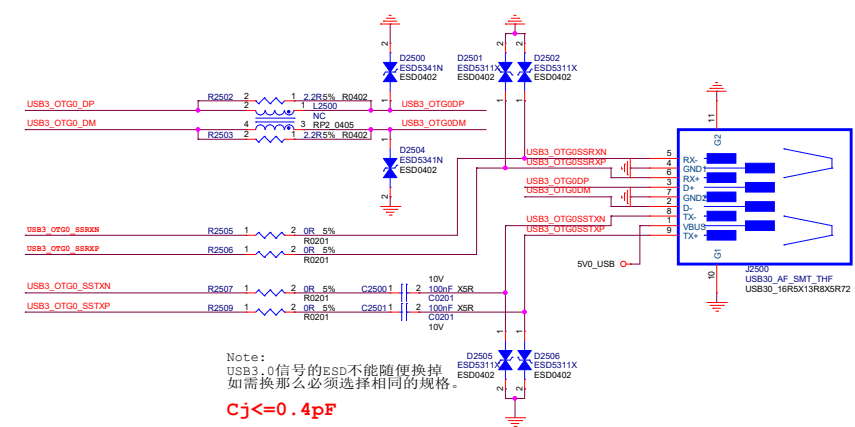


# Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



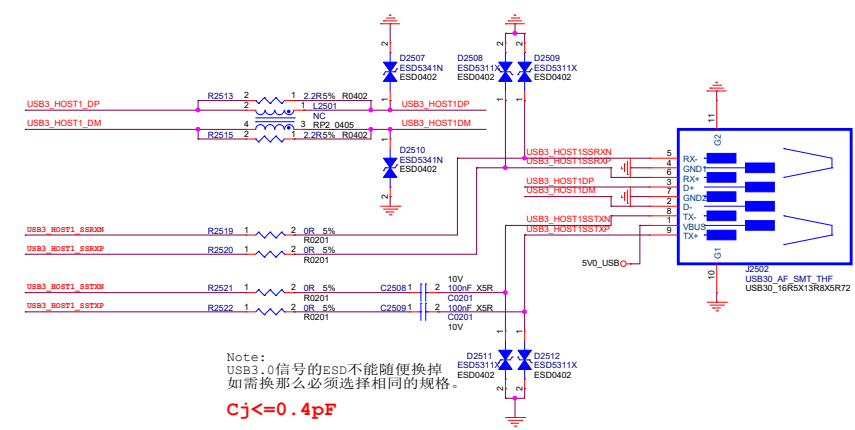
Note:  
FLASH\_VOL\_SEL state decided  
to VCCIO2-domain IO driven by default  
Logic=L: 3.3V IO driven  
Logic=H: 1.8V IO driven



Note:  
USB3.0信号的ESD不能随便换掉  
如需换那么必须选择相同的规格

$$C_j \leq 0.4 \text{ pF}$$

## USB3.0 OTG

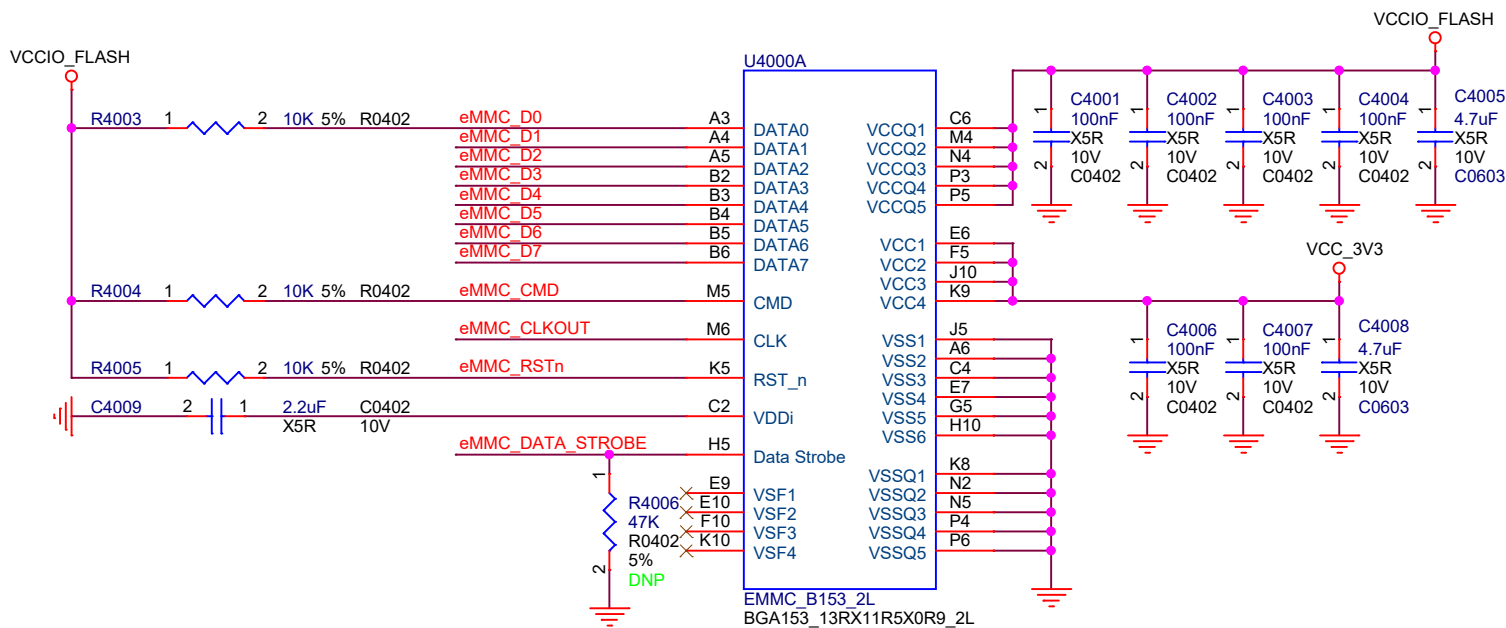


Note:  
USB3.0信号的ESD不能随便换掉  
如需换那么必须选择相同的规格

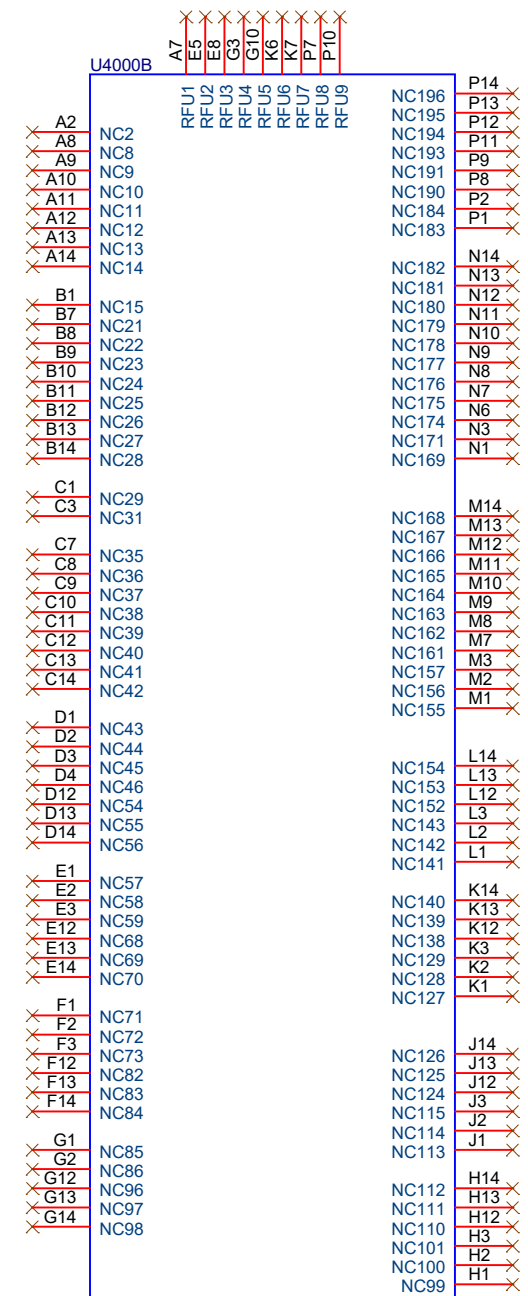
$$C_j \leq 0.4 \text{ pF}$$

## USB3.0 HOST1





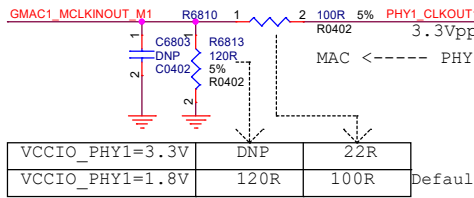
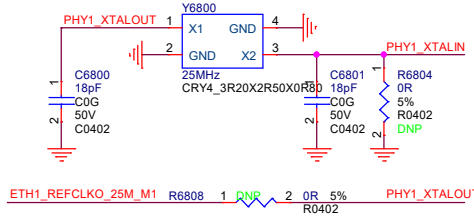
KLMBG2JETD-B041  
SDINBDA6-32G-XI1



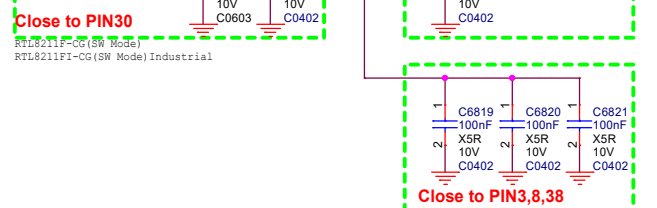
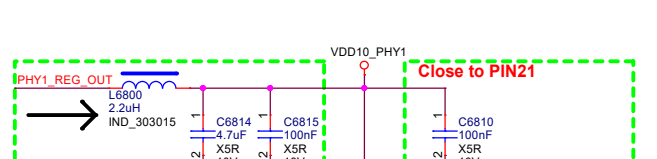
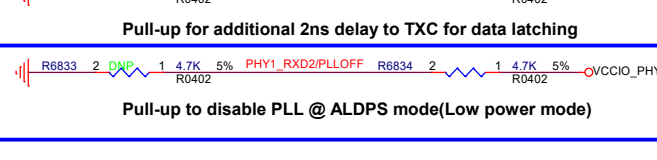
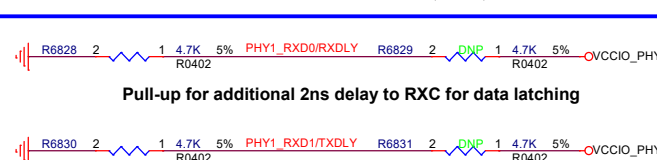
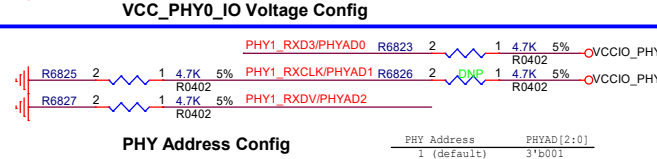
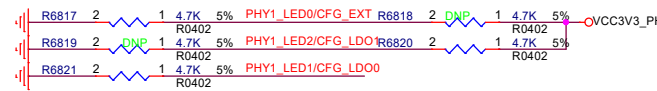
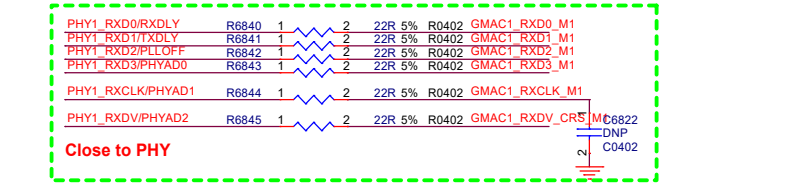
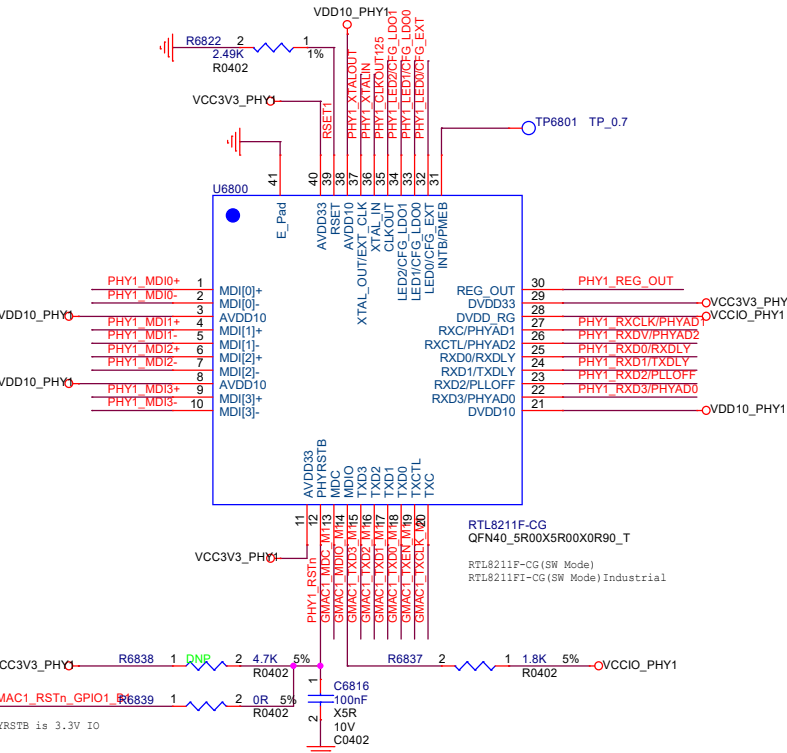
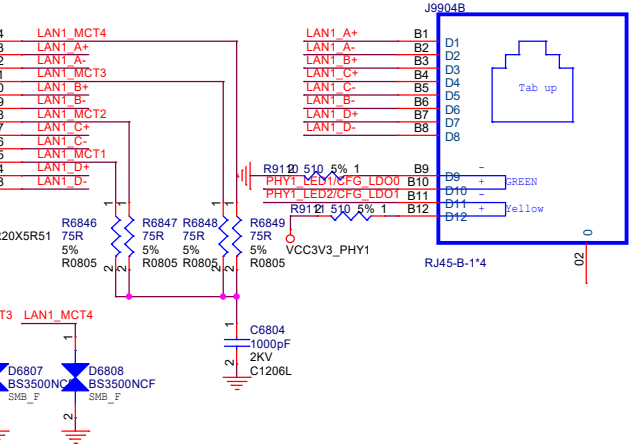
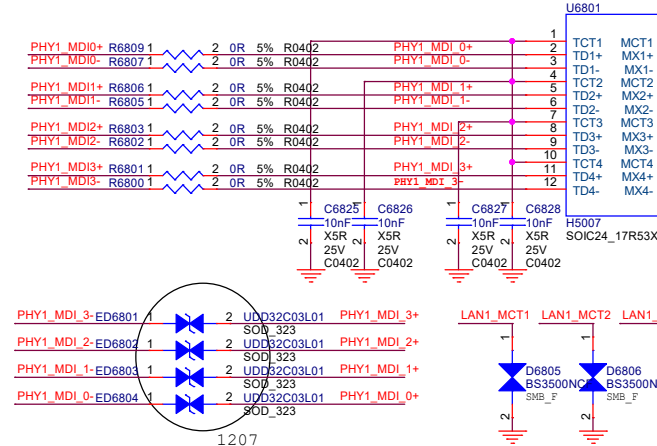
EMMC B153\_2L  
BGA153\_13RX11R5X0R9\_2L



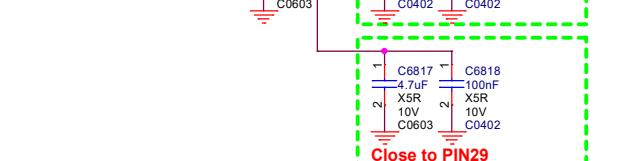
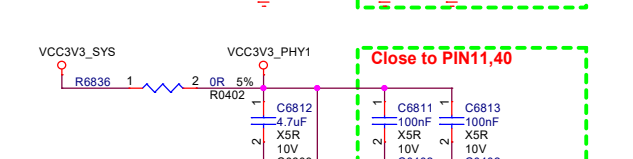
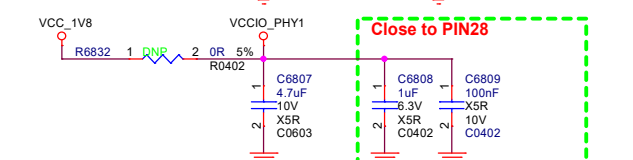
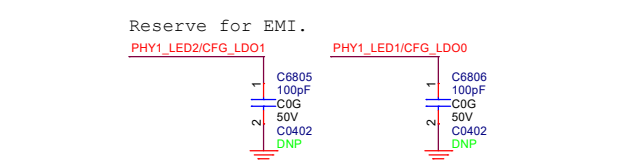
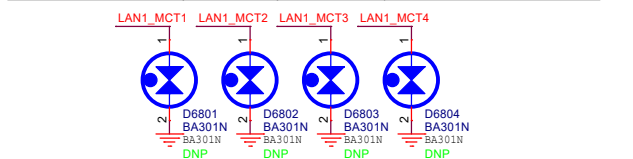
GMAC1\_TXD0\_M1 [11]  
GMAC1\_TXD1\_M1 [11]  
GMAC1\_TXD2\_M1 [11]  
GMAC1\_TXD3\_M1 [11]  
GMAC1\_TXEN\_M1 [11]  
GMAC1\_TXCLK\_M1 [11]  
GMAC1\_RXD0\_M1 [11]  
GMAC1\_RXD1\_M1 [11]  
GMAC1\_RXD2\_M1 [11]  
GMAC1\_RXD3\_M1 [11]  
GMAC1\_RXDV\_CRS\_M1 [11]  
GMAC1\_RXCLK\_M1 [11]  
ETH1\_REFCLKO\_25M\_M1 [11]  
GMAC1\_MCLKINOUT\_M1 [11]  
GMAC1\_MDC\_M1 [11]  
GMAC1\_MDIO\_M1 [11]  
GMAC1\_RSTn\_GPIO1\_B1 [14]



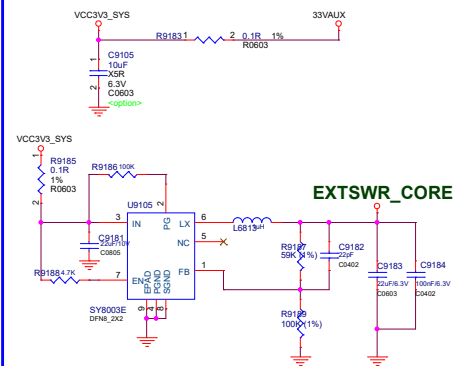
VCCIO_PHY1=3.3V	DNP	22R	Default
VCCIO_PHY1=1.8V	120R	100R	



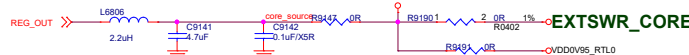
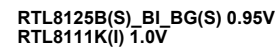
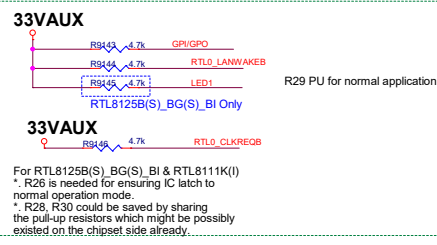
RGMI Power Source	CFG EXT	CFG LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	

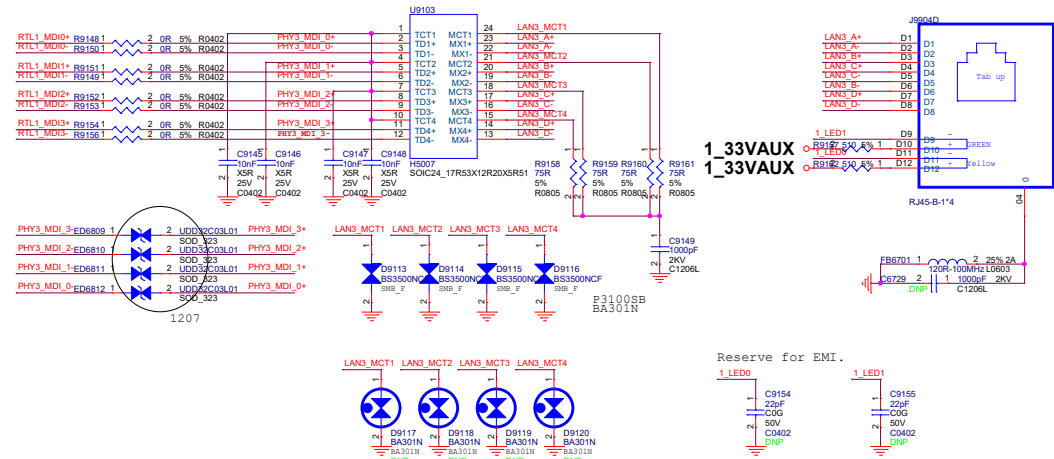
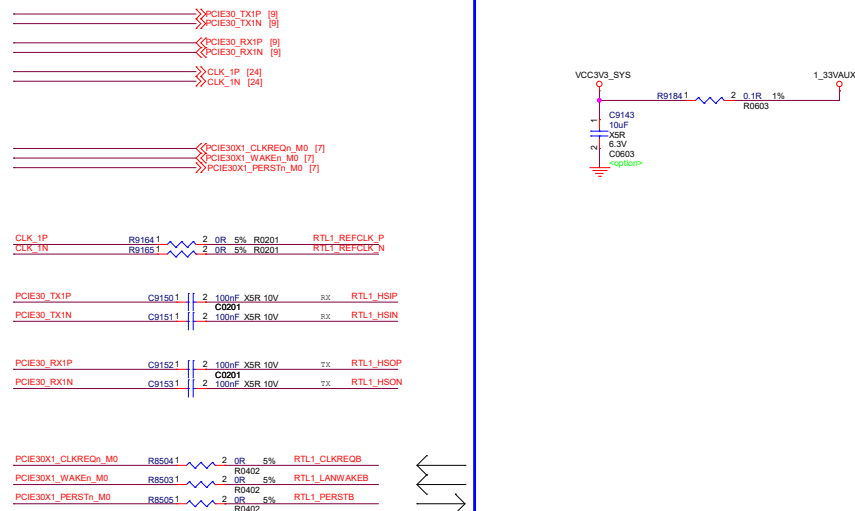




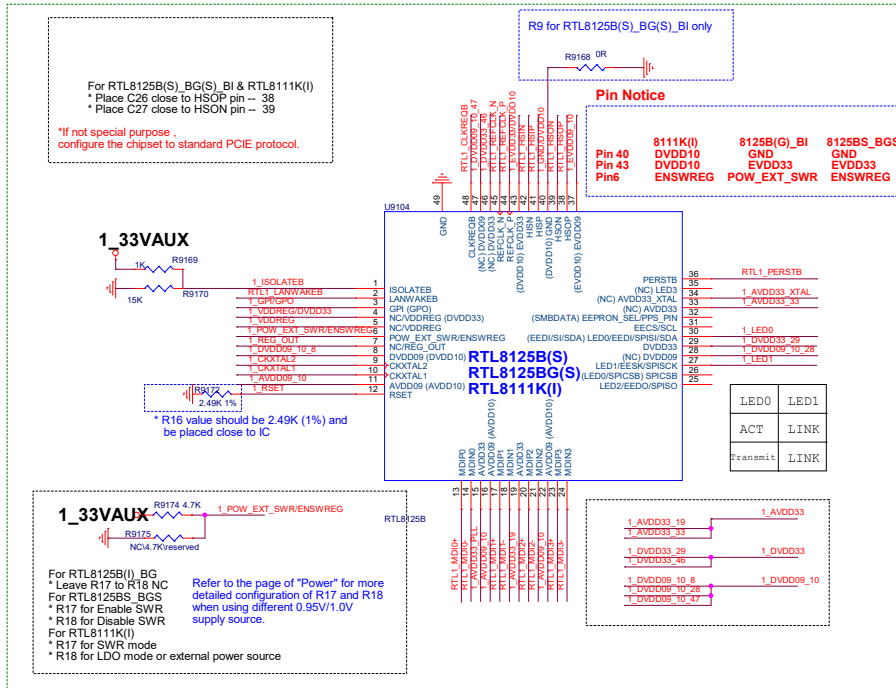


\* If not special purpose ,  
configure the chipset to standard PCIE protocol.

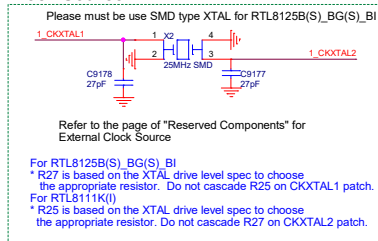




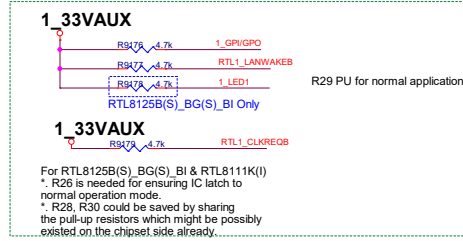
## Ethernet PHY



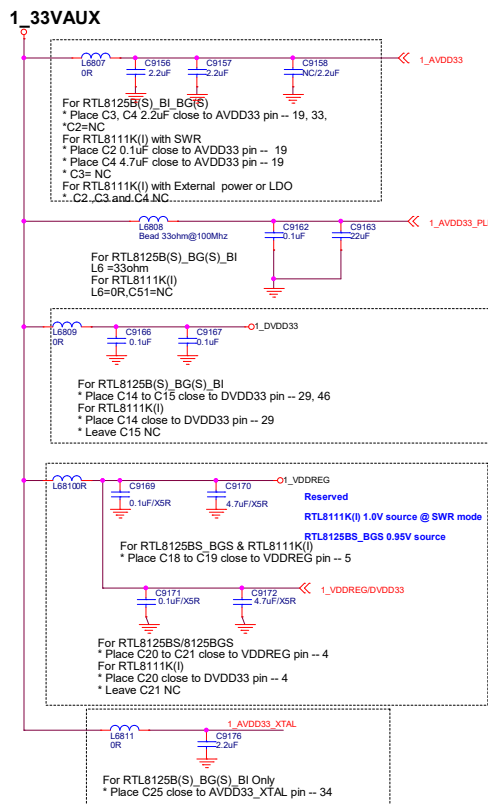
## Clock Source



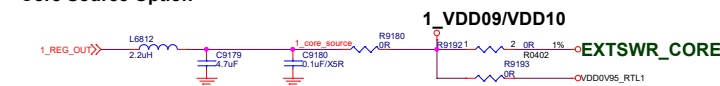
## External Resistor



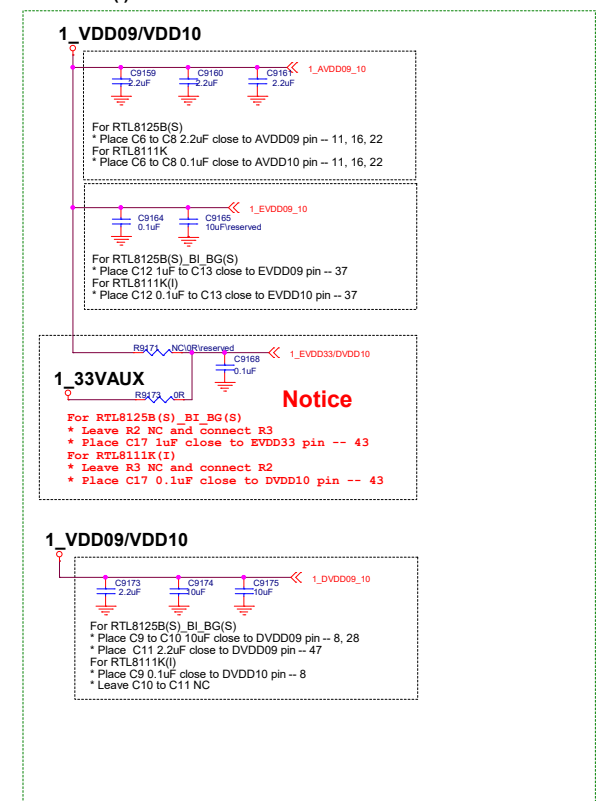
## 3.3V

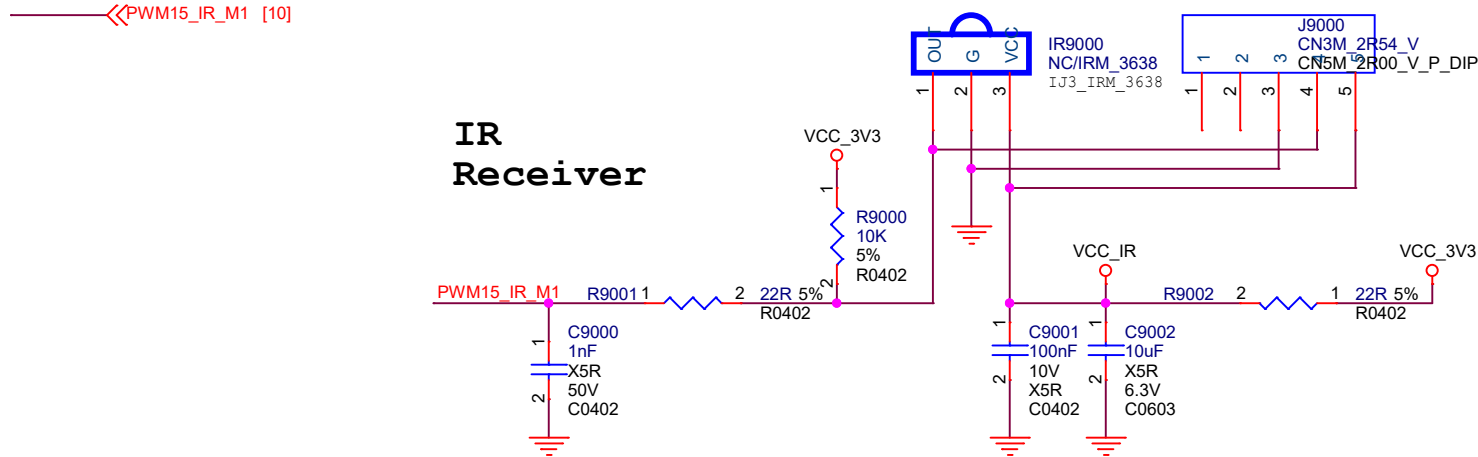


## Core Source Option



## RTL8125B(S)\_BI\_BG(S) 0.95V RTL8111K(I) 1.0V



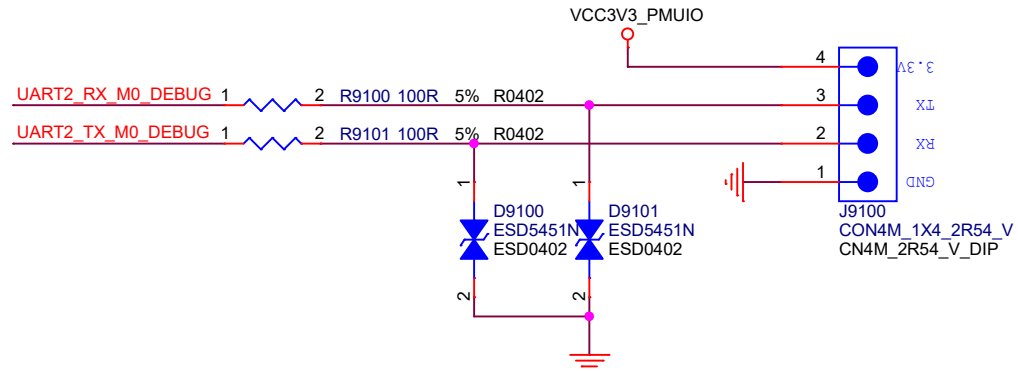


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<<UART2\_RX\_M0\_DEBUG [7]  
>>UART2\_TX\_M0\_DEBUG [7]

## Debug UART2



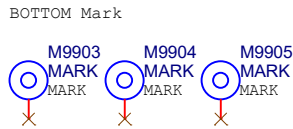
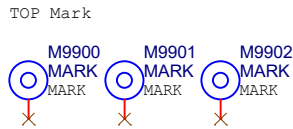
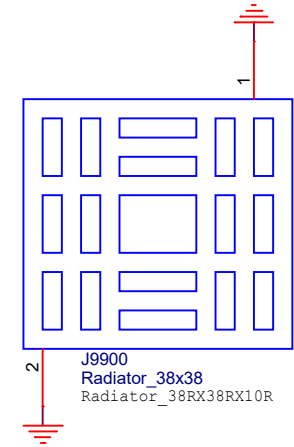
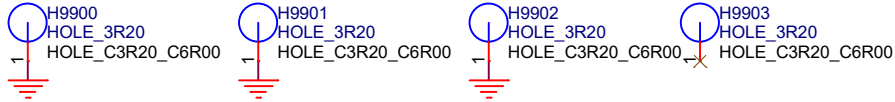
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