

Schematics For Lunzn r68s

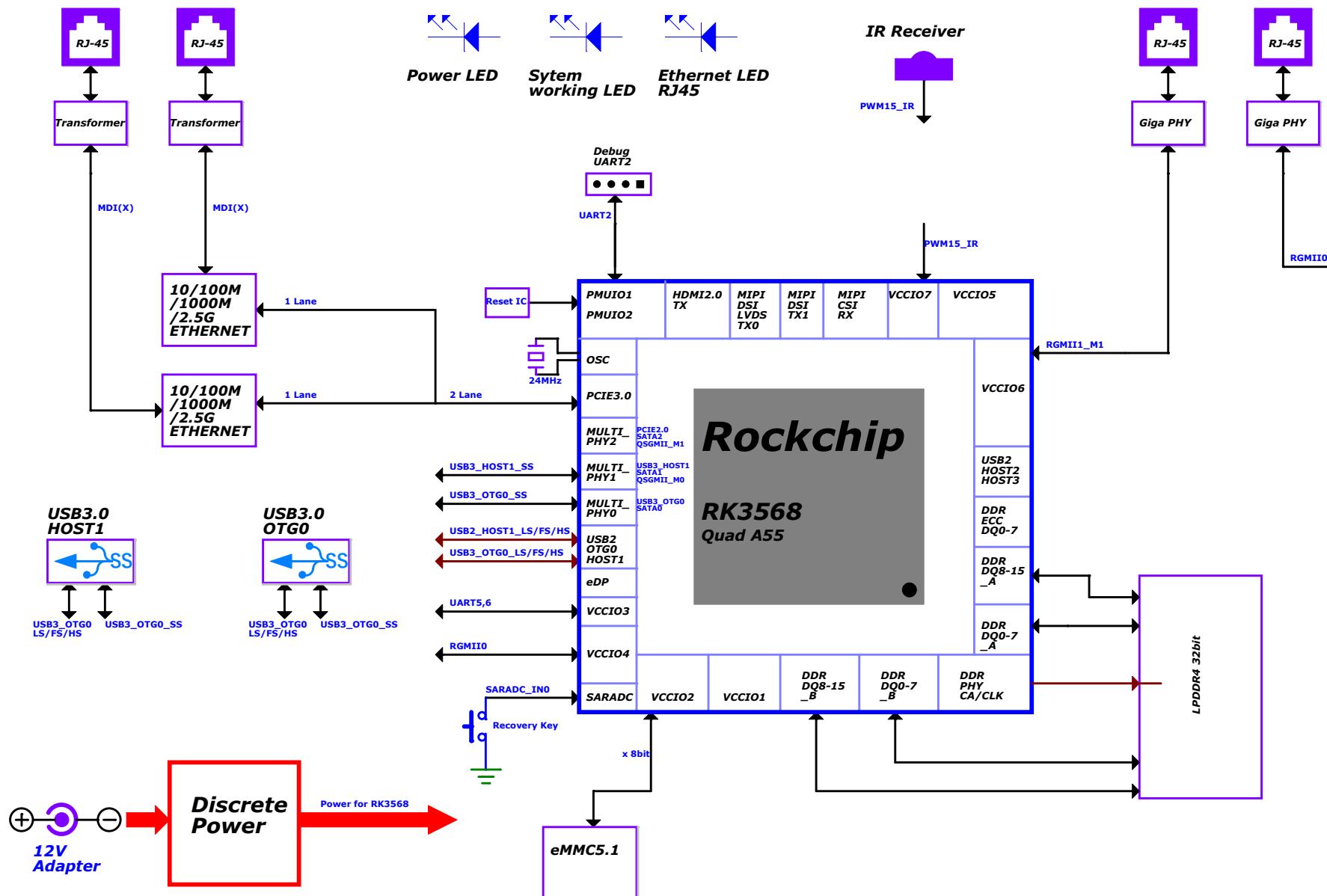
RK3568

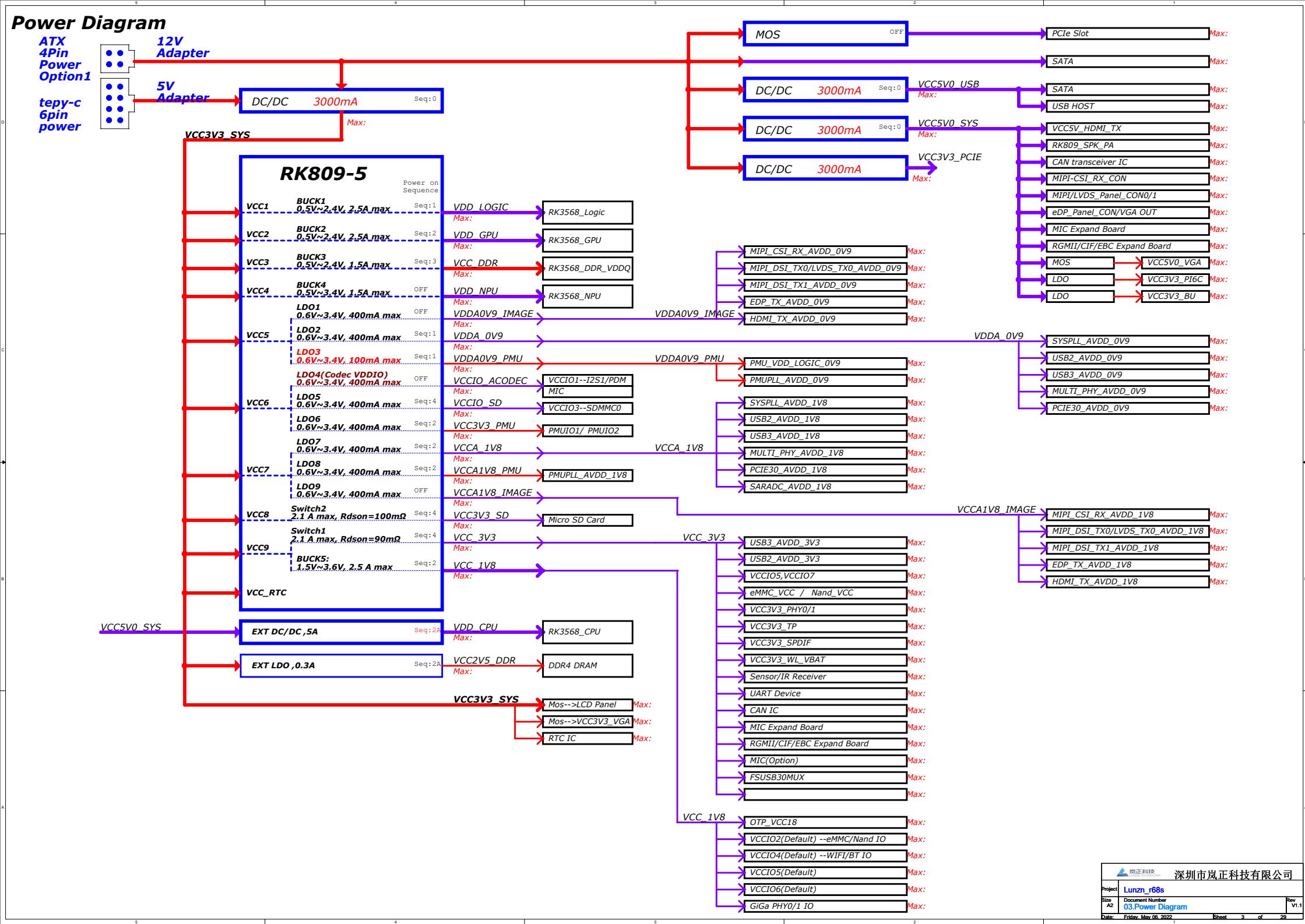
Main Functions Introduction

- 1) PMIC: RK809-5+DiscretePower
- 2) RAM: LPDDR4 1x32Bit 16Gb
- 3) ROM: eMMC5.1 64Gb
- 4) Support: 1 x USB3.0 OTG + 1 x USB3.0 HOST
- 5) Support: 2 x 1Lanes PCIe - 2.5G Ethernet
- 6) Support: 2 x 10/100/1000 Ethernet(RGMII)
- 7) Support: 1 x IR Receiver
- 8) Support: 1 x Power LED,1 x System LED RJ45^LED
- 9) Support: 1 x Recovery Key
- 10) Support: Debug UART

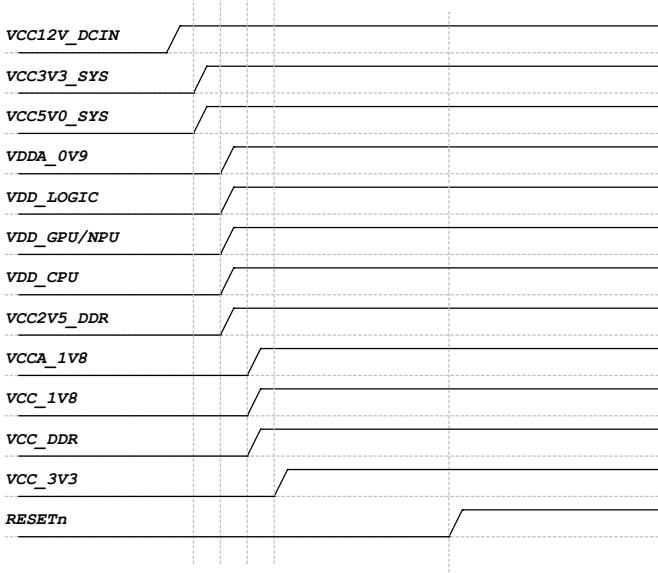
 岚正科技 LUNZN TECHNOLOGY	深圳市岚正科技有限公司		
Project	Lunzn_r68s		
Size A4	Document Number 01.Cover Page	Rev V1.1	
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Lunzn r68s Block Diagram





Power Sequence

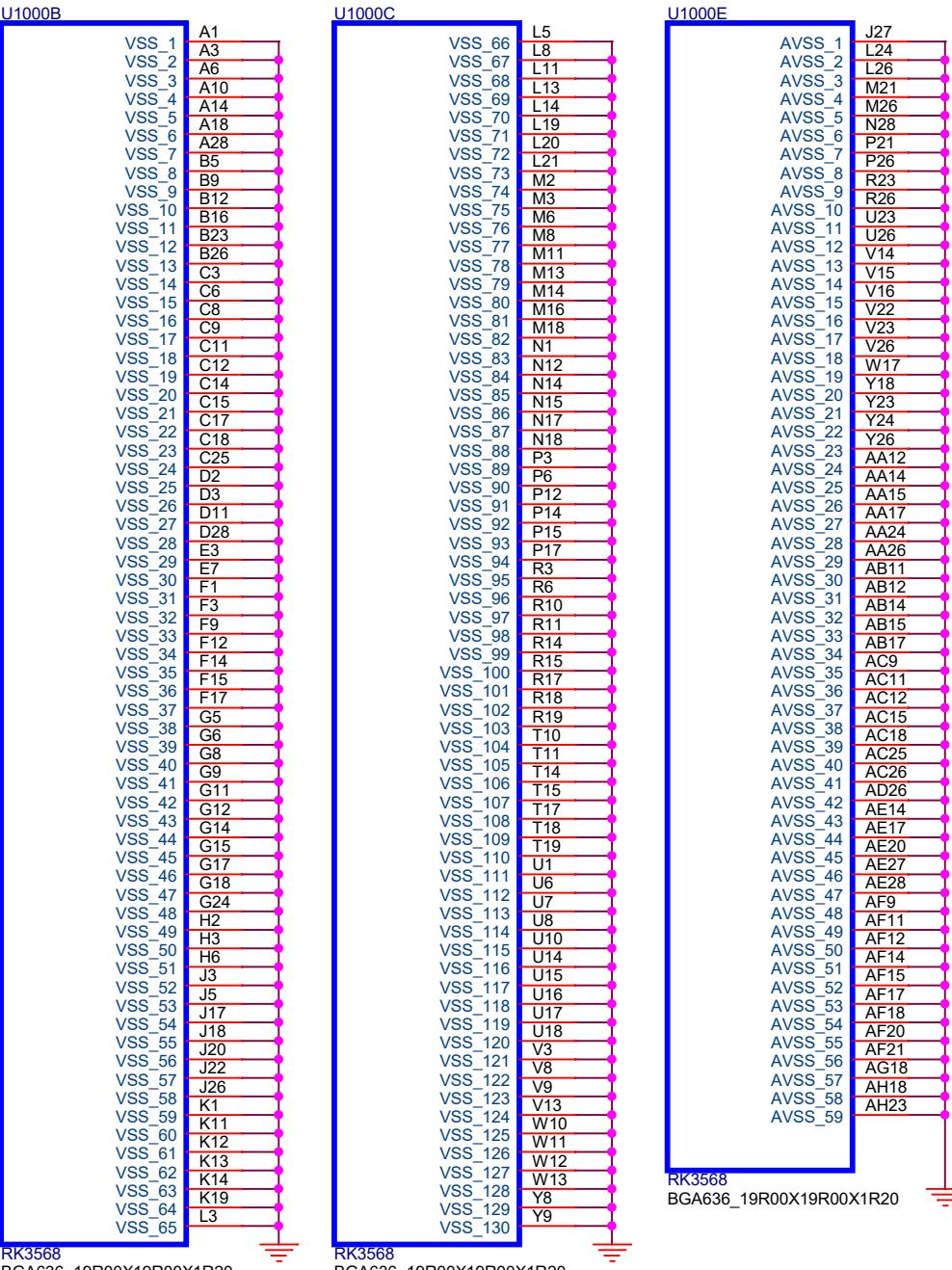
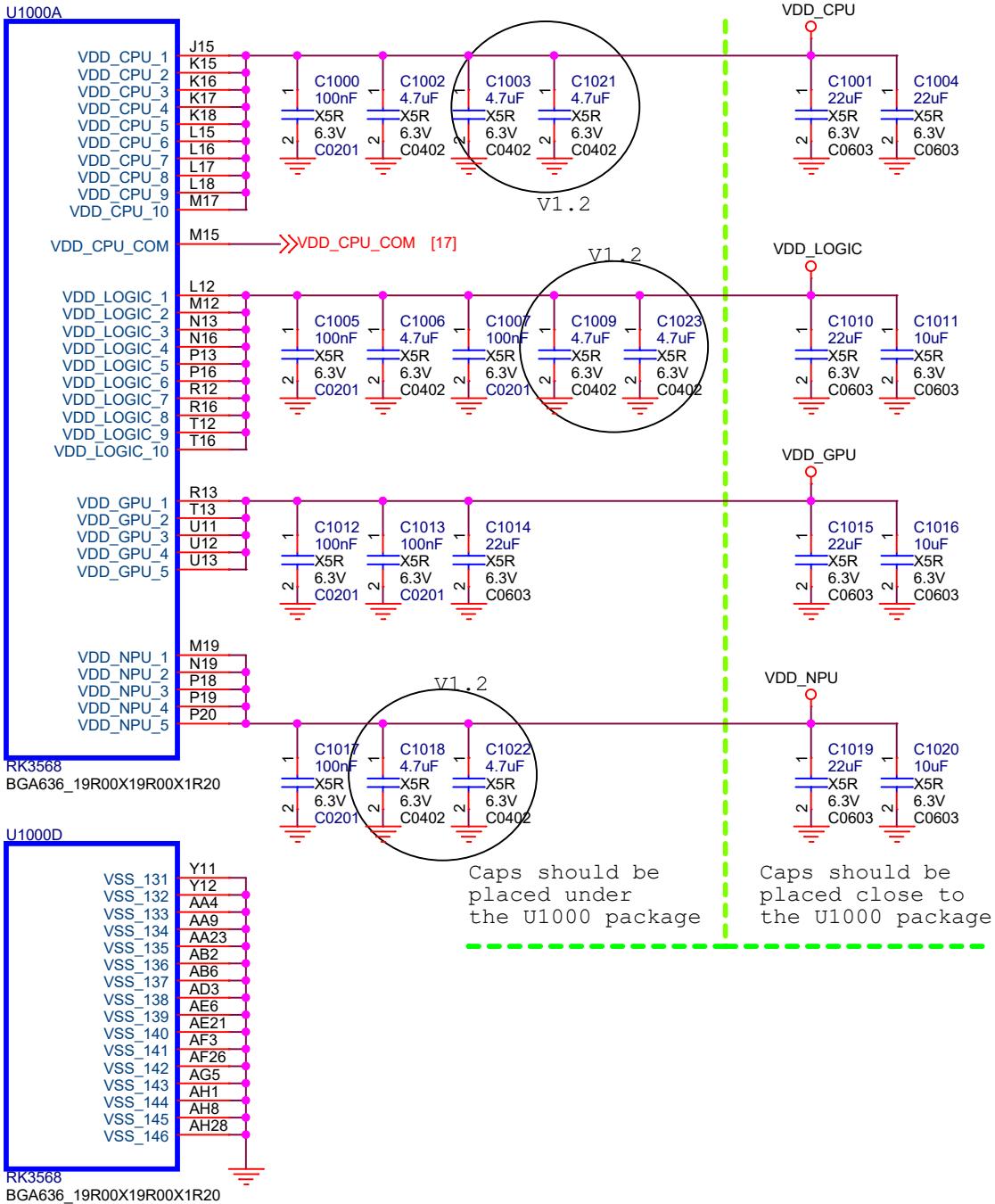


Power Supply	Channel	Supply Limit	Power Name	Time Slot	Default Voltage
VCC12V_DCIN	BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V
VCC12V_DCIN	BUCK	3.0A	VCC5V0_SYS	Slot:0	5.2V
VCC3V3_SYS			VCC3V3_PMUIO	Slot:0	3.3V
VCC3V3_SYS	LDO	0.3A	VDDA_0V9	Slot:1	0.9V
VCC3V3_SYS	BUCK	1.5A	VDD_LOGIC	Slot:1	0.9V
VCC3V3_SYS	BUCK	3.0A	VDD_GPU/NPU	Slot:1	0.9V
VCC3V3_SYS	BUCK	5.0A	VDD_CPU	Slot:1	0.9V
VCC3V3_SYS	LDO	0.3A	VCC2V5_DDR	Slot:1	2.5V
VCC3V3_SYS	LDO	0.5A	VCC_1V8	Slot:2	1.8V
VCC3V3_SYS	LDO	0.5A	VCCA_1V8	Slot:2	1.8V
VCC3V3_SYS	BUCK	1.5A	VCC_DDR	Slot:2	1.2V DDR4
VCC3V3_SYS	MOS	2A	VCC_3V3	Slot:3	3.3V
VCC3V3_PMUIO	RESETn				

IO Power Domain Map
Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC_3V3	VCC_3V3	3.3V	
PMUIO2	Pin W19	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO1	Pin H17	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO4	Pin J21	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCC_3V3	VCC_3V3	3.3V	

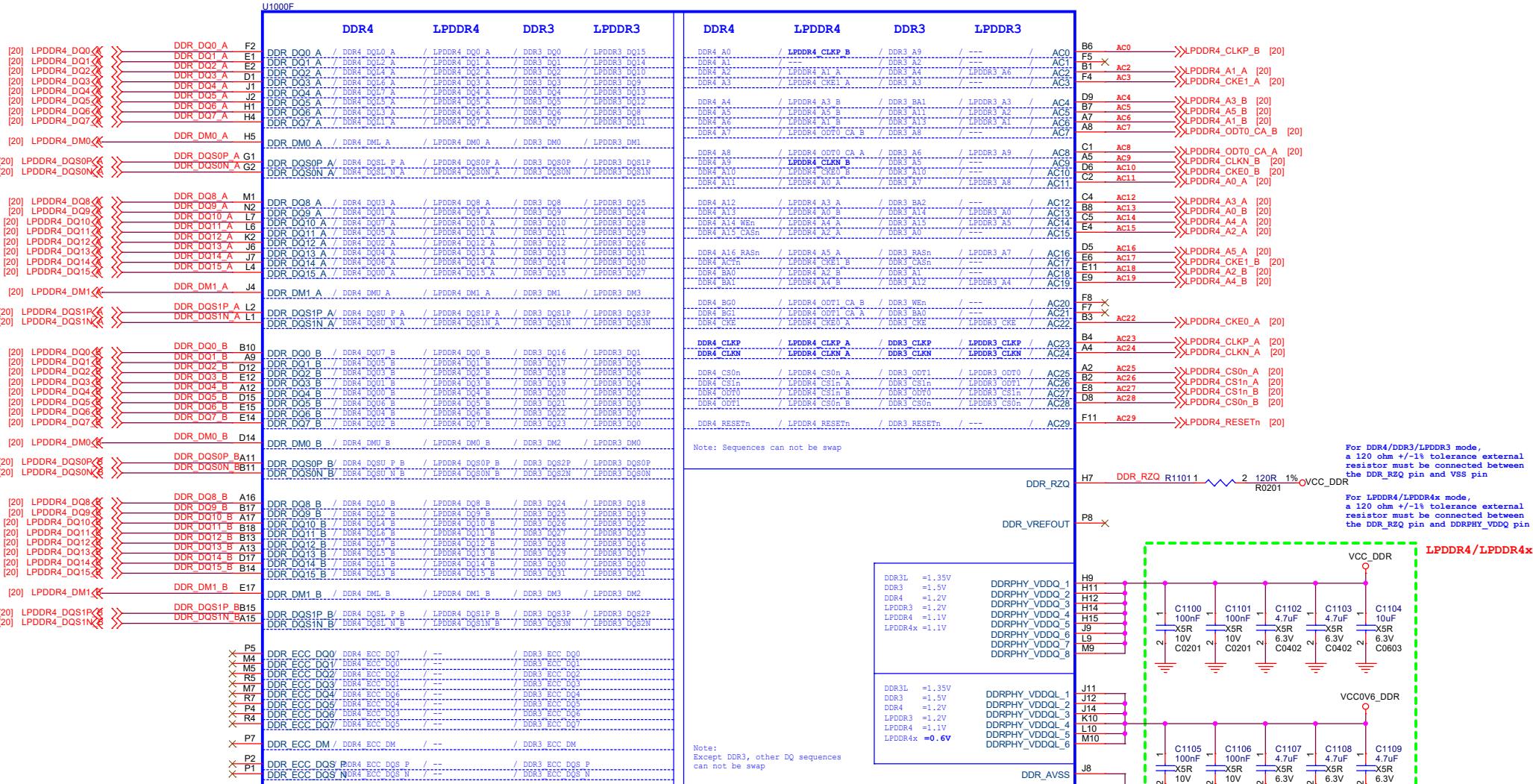
RK3568 ABCDE (Power&Gnd)



Caps should be placed under the U1000 package	 Caps should be placed close to the U1000 package
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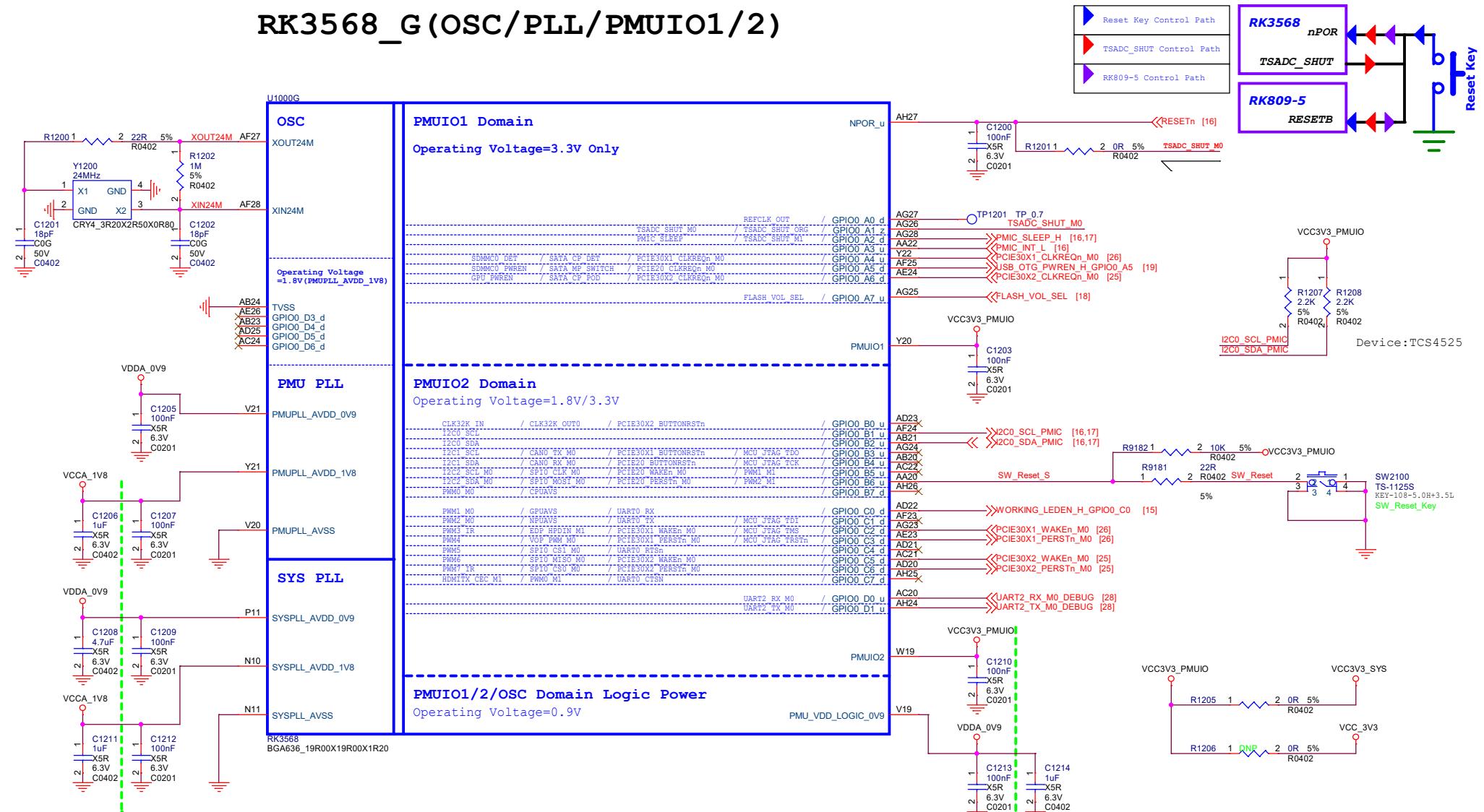
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Project	Lunzn_68s
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RK3568 F (DDR PHY)



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RK3568 G (OSC/PLL/PMUIO1/2)

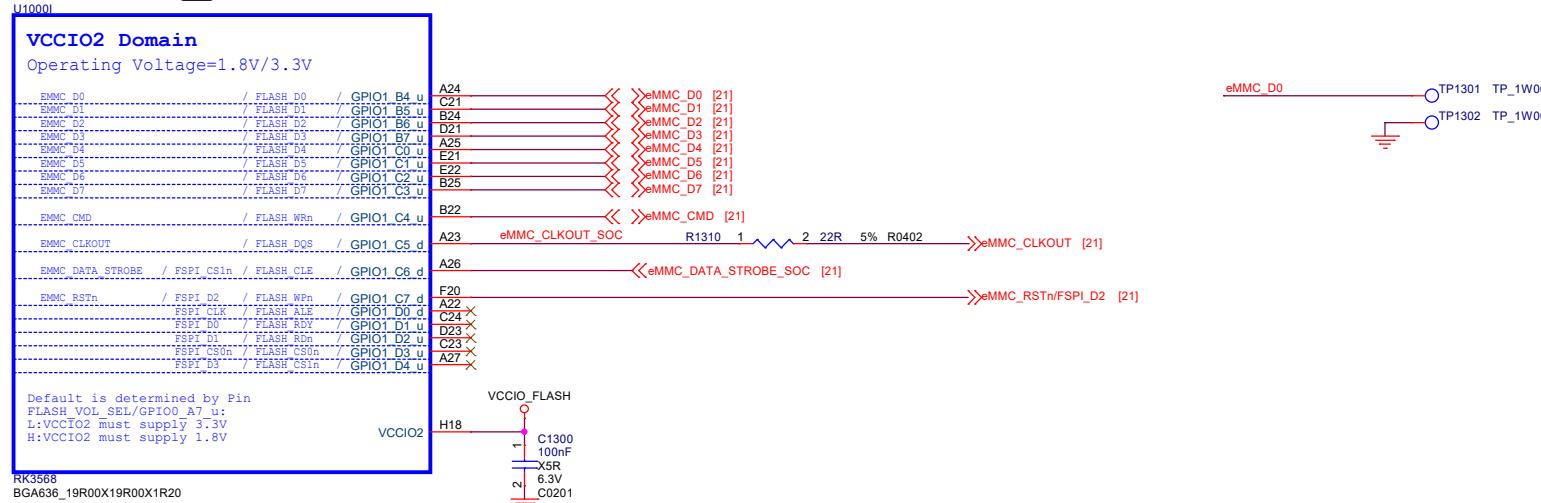


Note:

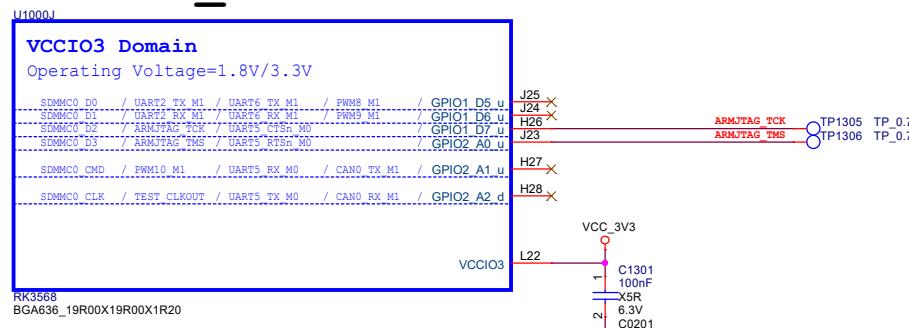
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



RK3568 I (VCCIO2 Domain)

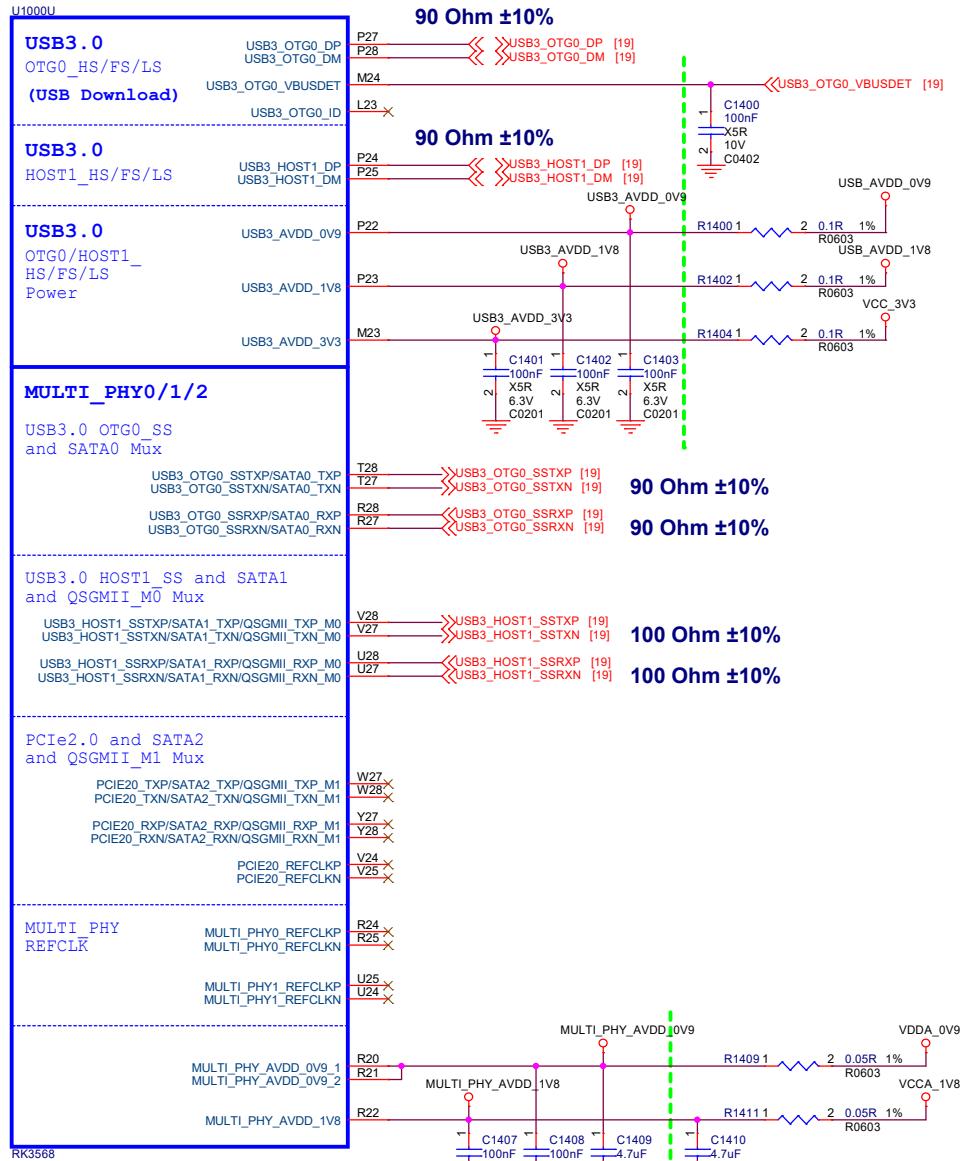


RK3568 J(vccio3 Domain)



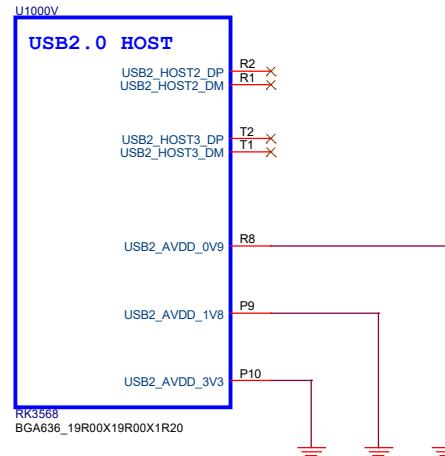
Note: Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3568_U (USB3.0/SATA/QSGMII/PCIe2.0 x1)



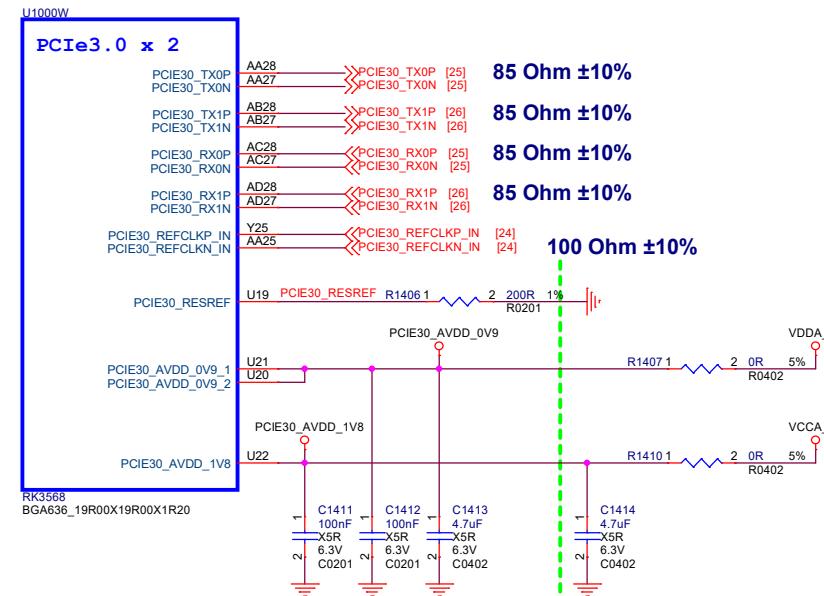
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package.

RK3568_V (USB2.0 HOST)

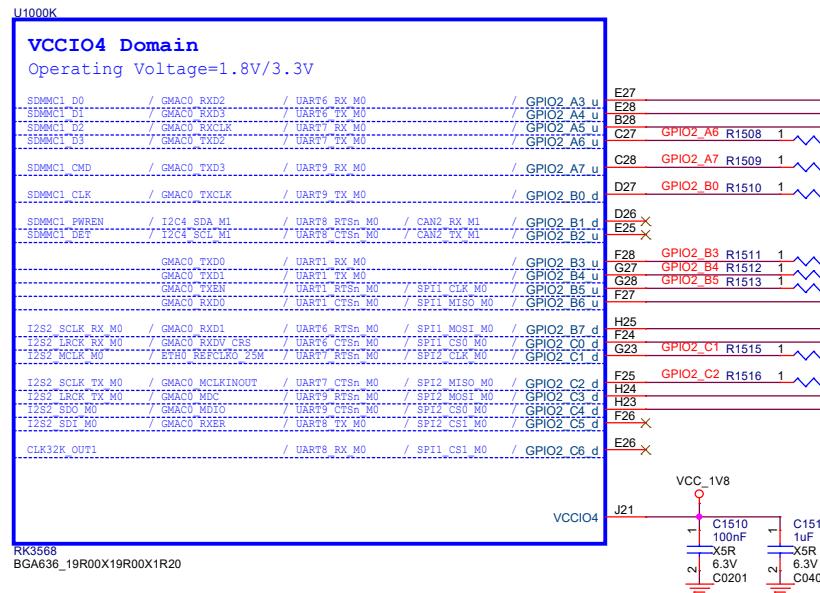


如果不使用的模块不供电，那么需要软件对DTS中对应的节点进行 disable_isable 配置，否则可能会引起内核初始化卡死现象。

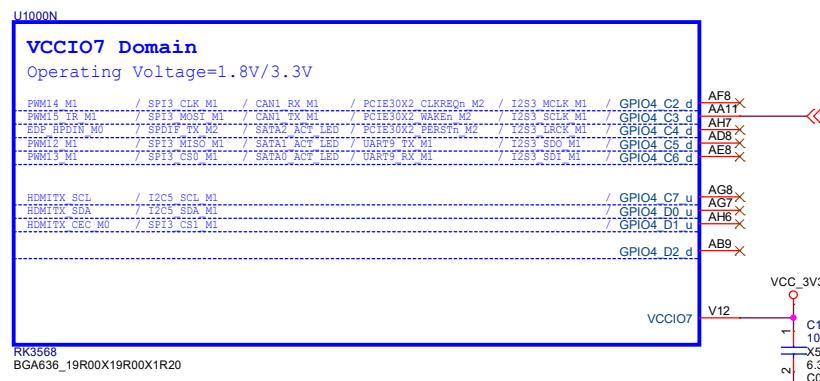
RK3568_W (PCIe3.0 x2)



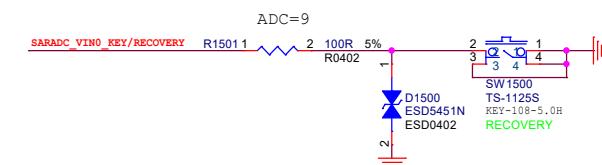
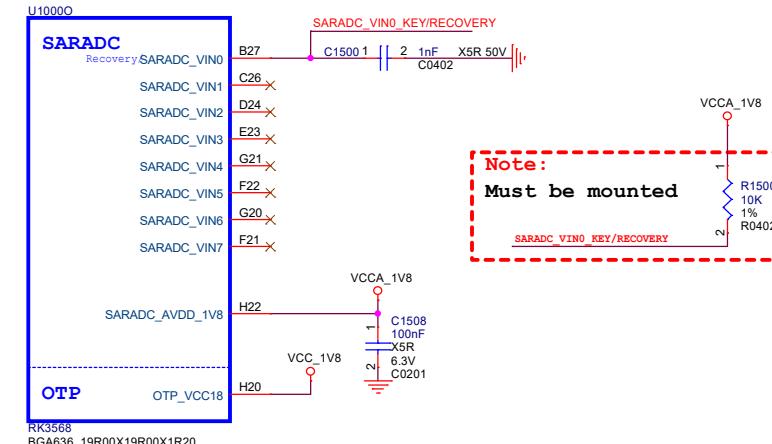
RK3568_K (VCCIO4 Domain)



RK3568_N (VCCIO7 Domain)

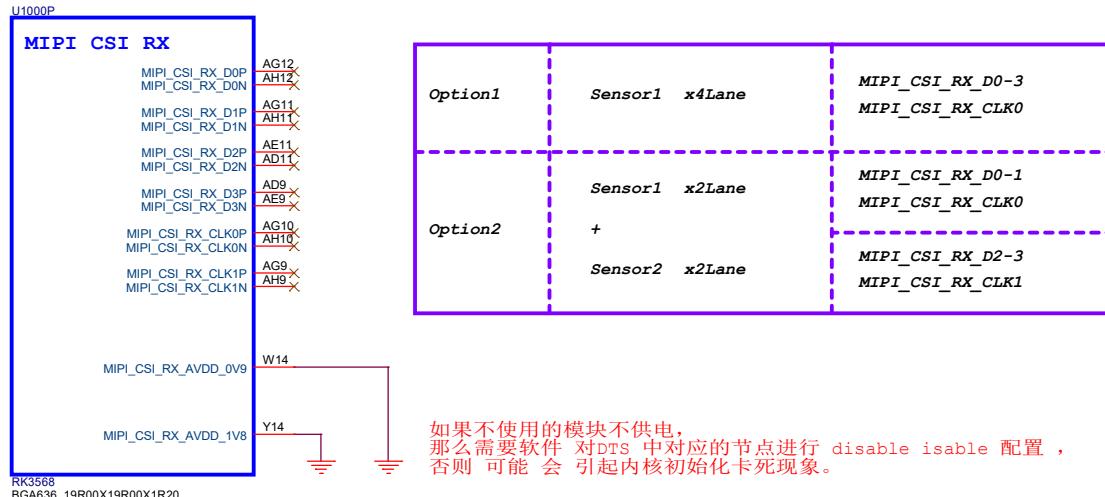


RK3568_O (SARADC/OTP)

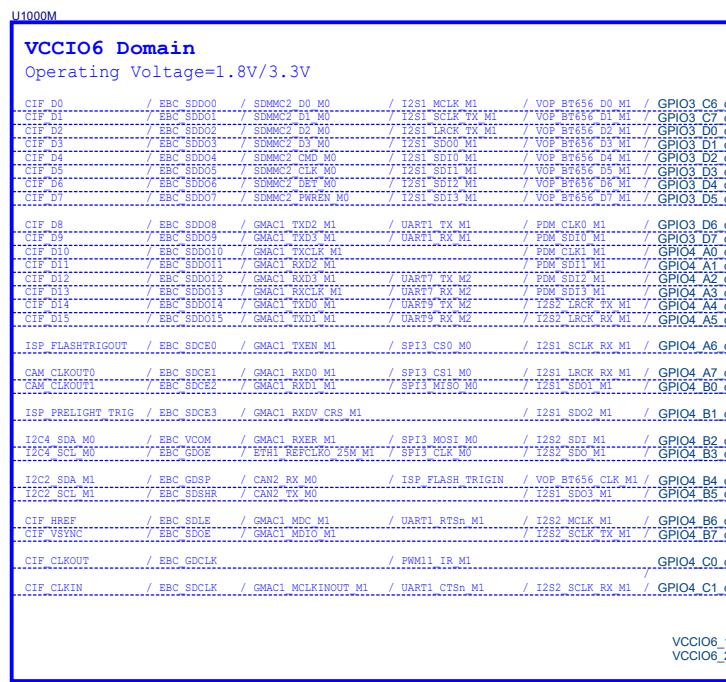


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3568_P(MIPI_CSI_RX)



RK3568_M(VCCIO6 Domain)



RK3568
BG636_19R00X19R00X1R20

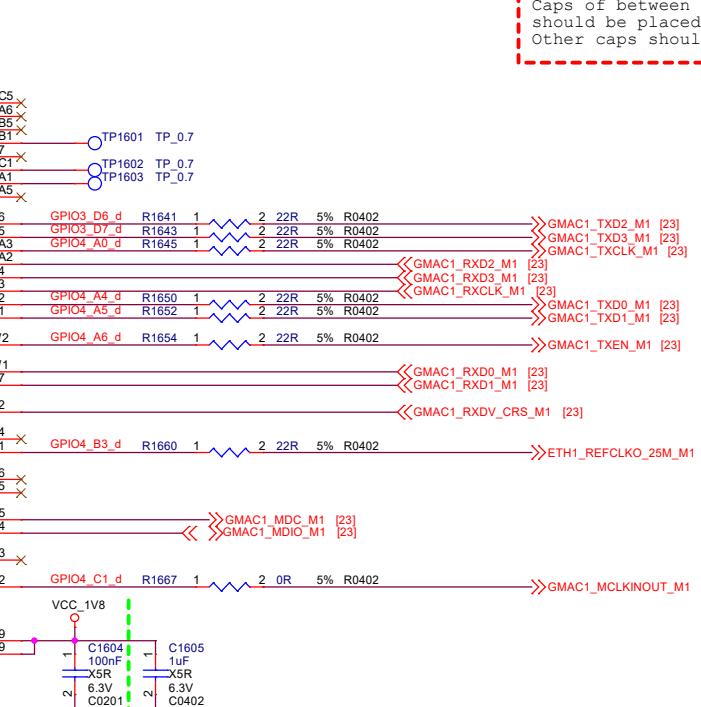
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

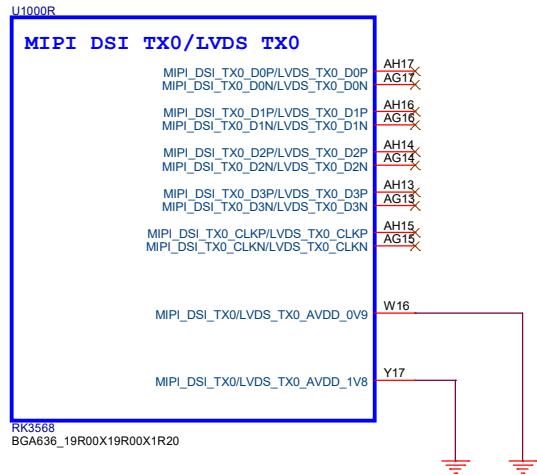
Note:

Caps between dashed green lines and U1000 should be placed under the U1000 package.

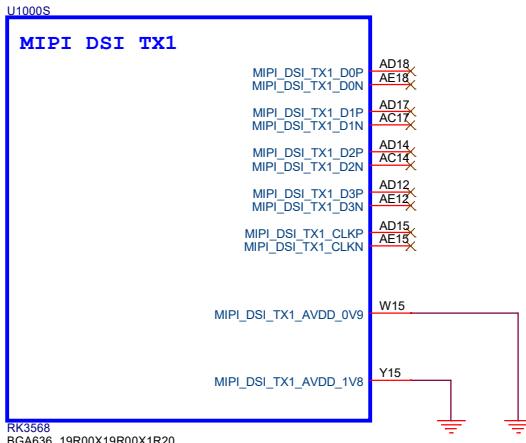
Other caps should be placed close to the U1000 package



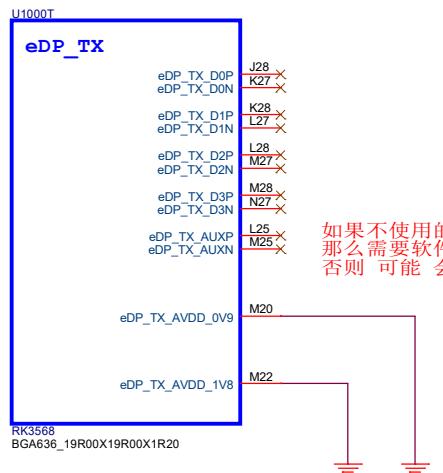
RK3568_R (MIPI_DSI_TX0/LVDS_TX0)



RK3568_S (MIPI_DSI_TX1)

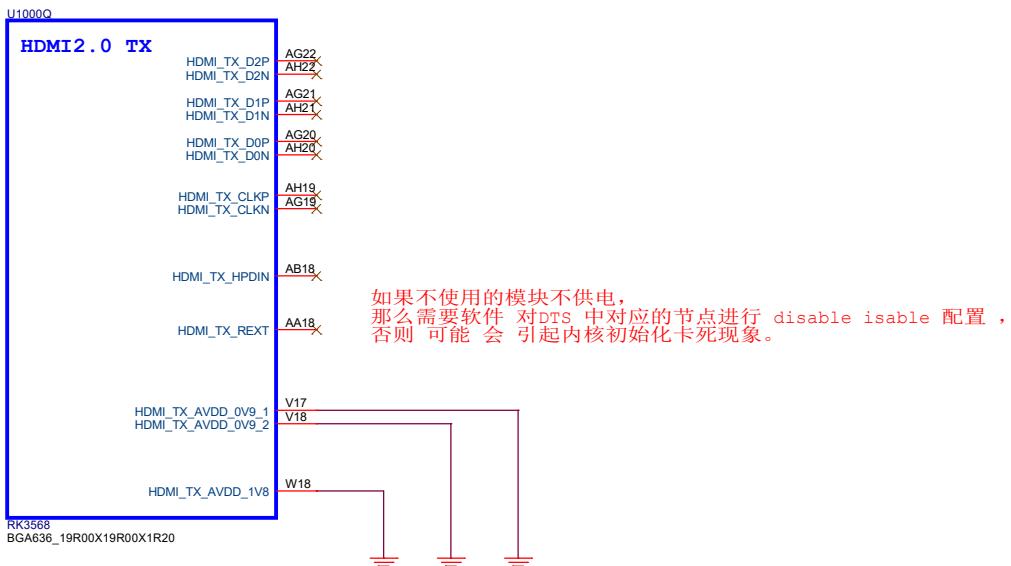


RK3568_T (eDP_TX)



Note:
Caps between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package.

RK3568_Q (HDMI2.0_TX)

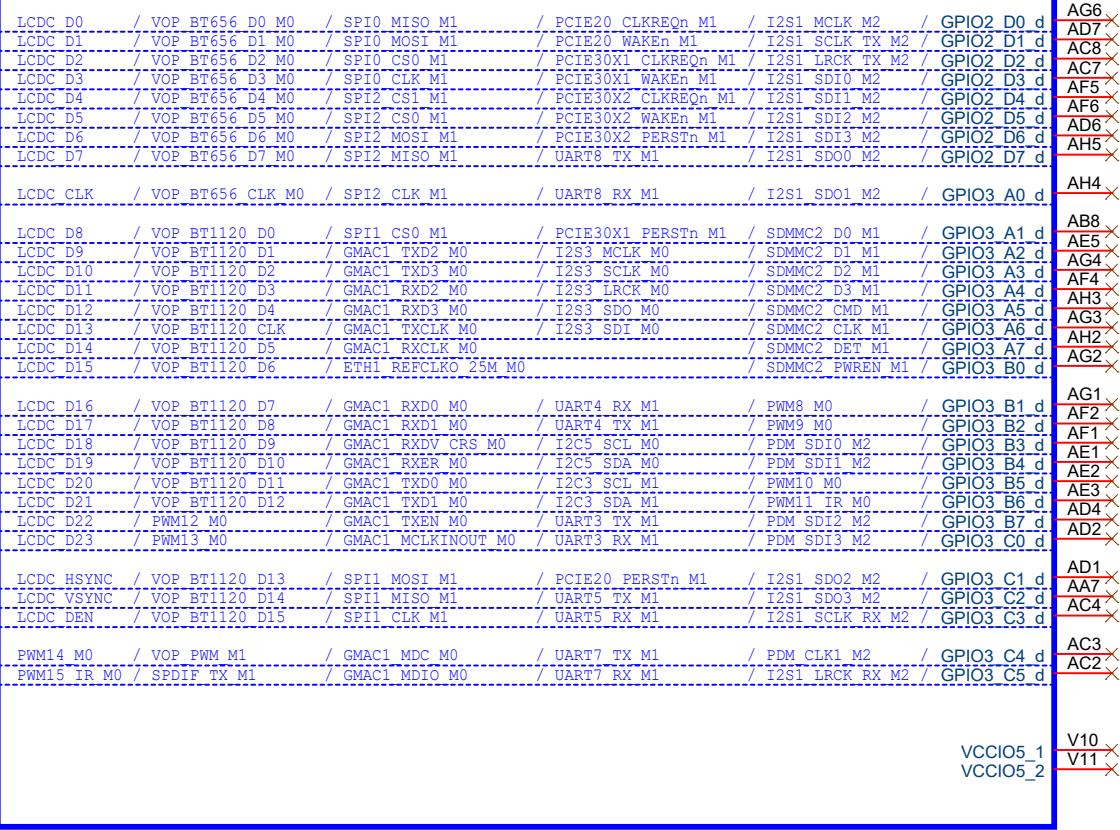


RK3568_L (VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V



RK3568
BGA636_19R00X19R00X1R20

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

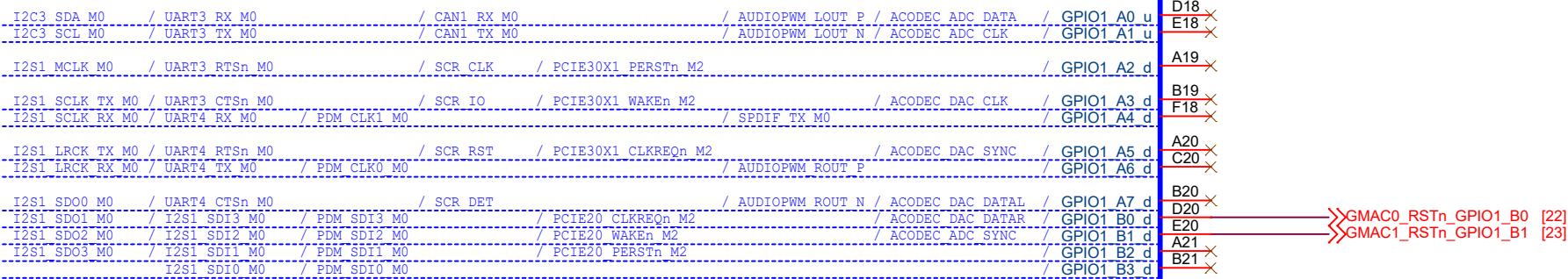
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Project	Lunzn_r68s
Size	Document Number 13.RK3568_VO Interface_2
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RK3568_H (VCCIO1 Domain)

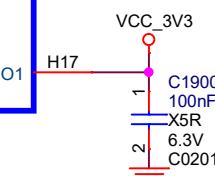
U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V



RK3568
BGA636_19R00X19R00X1R20



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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Document Number:

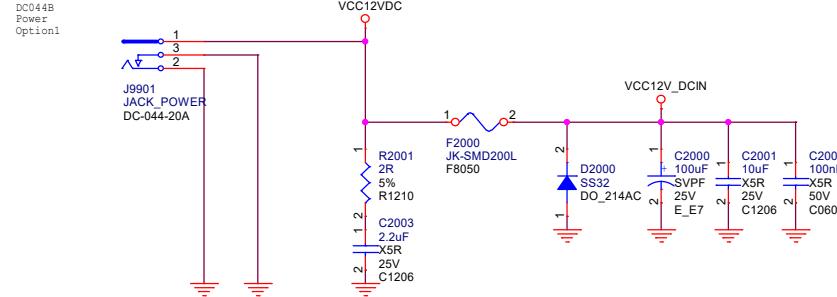
14.RK3568_Audio Interface

Rev: V1.1

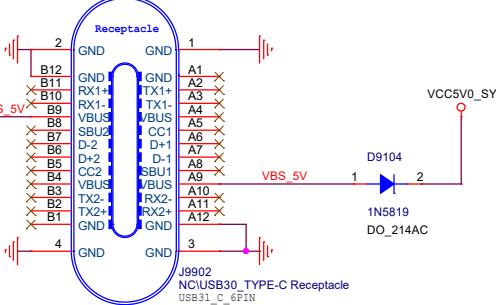
Date: Friday, May 06, 2022

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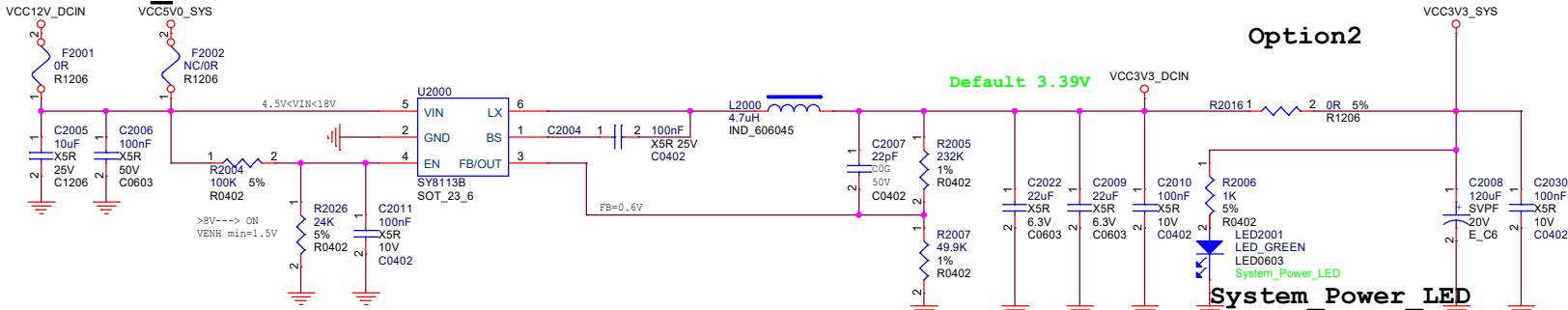
12V/3A DCIN



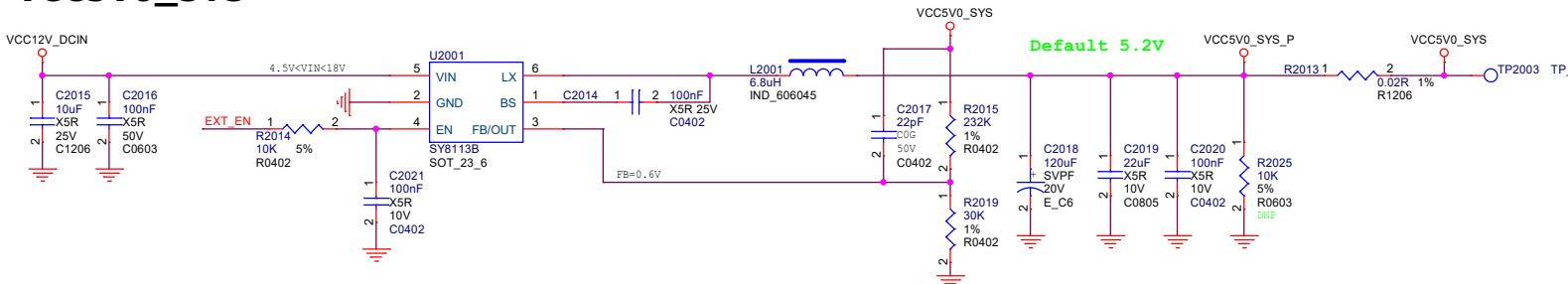
tepy-c 6pin power



VCC3V3_SYS

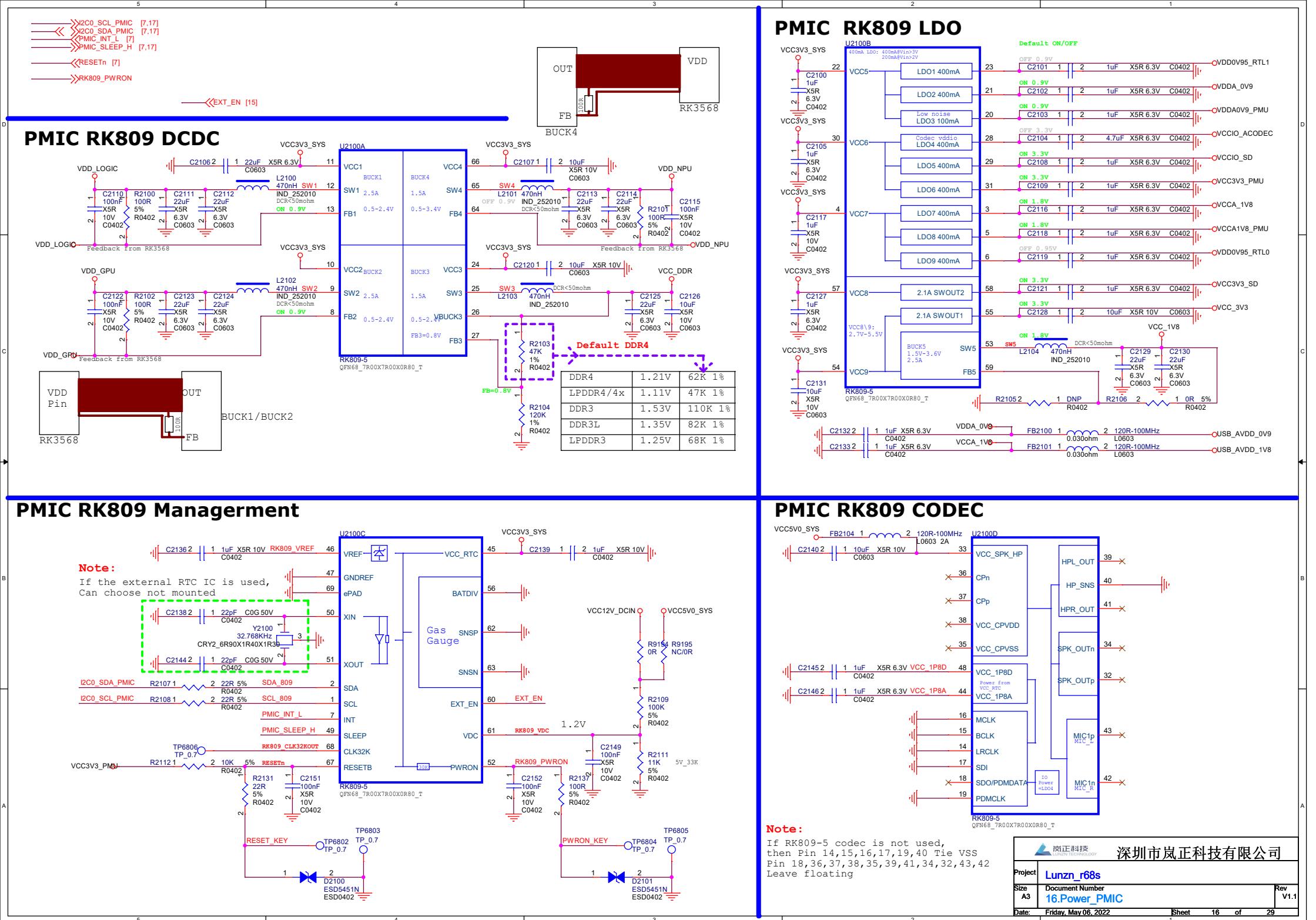


VCC5V0_SYS



VCC5V0_USB

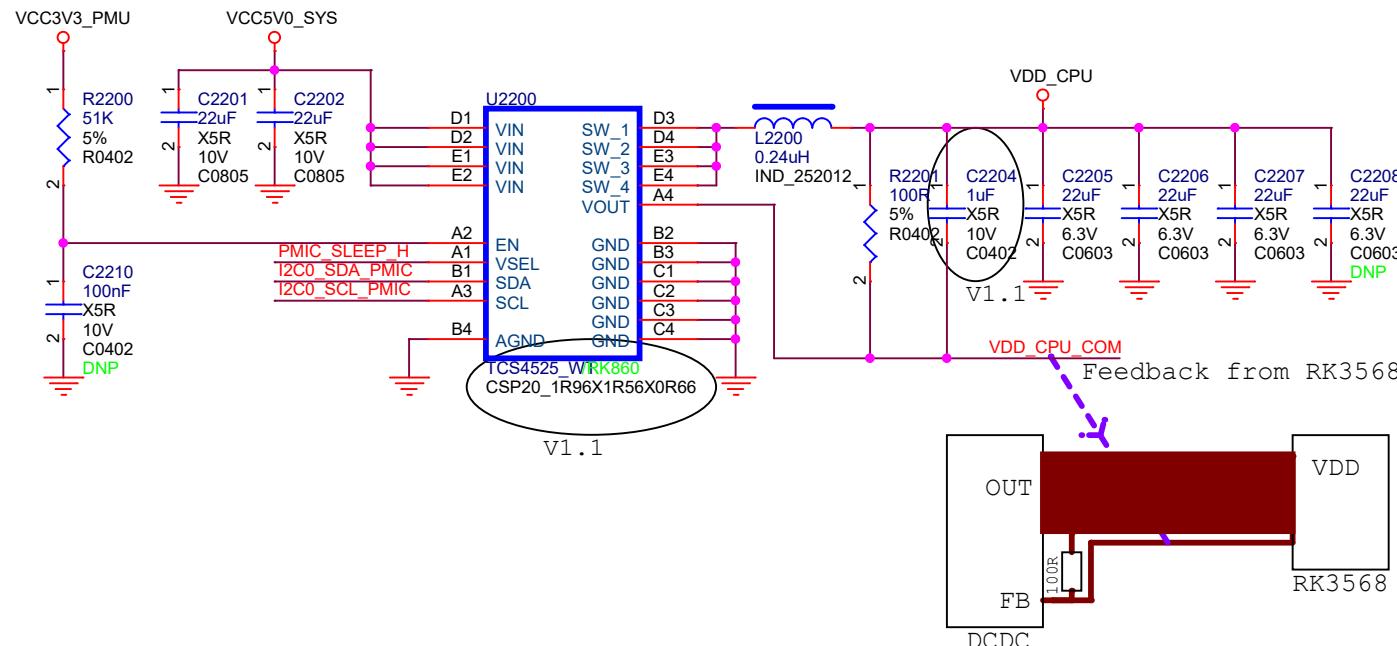




5 4 3 2 1

I2C0_SCL_PMIC [7,16]
 I2C0_SDA_PMIC [7,16]
 PMIC_SLEEP_H [7,16]
 VDD_CPU_COM [5]

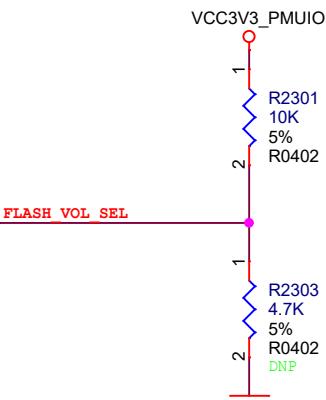
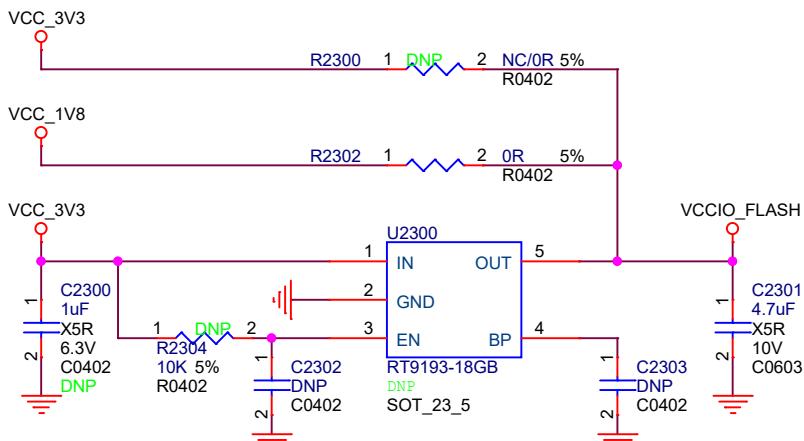
VDD_CPU



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Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



Note:
 FLASH_VOL_SEL state decided
 to VCCIO2 domain IO driven by default
 Logic=L: 3.3V IO driven
 Logic=H: 1.8V IO driven



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Project: Lunzn_r68s

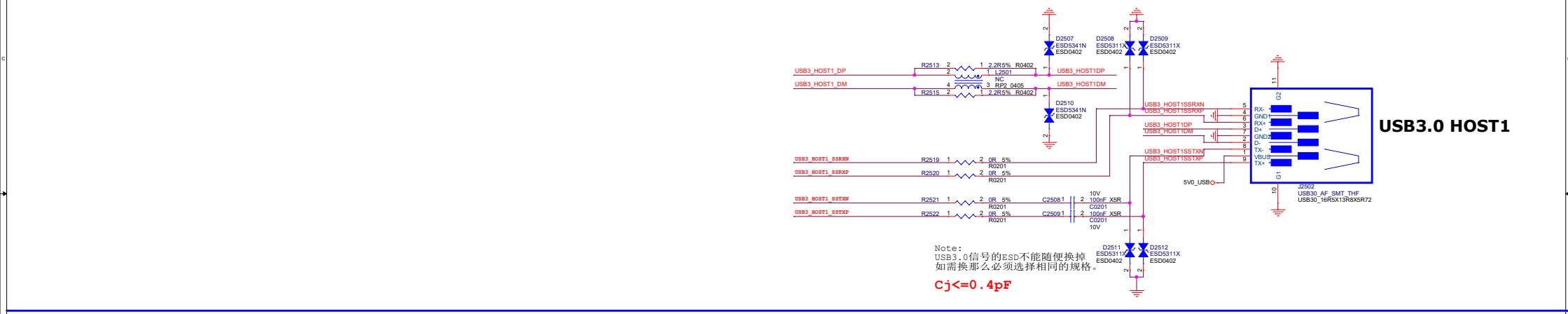
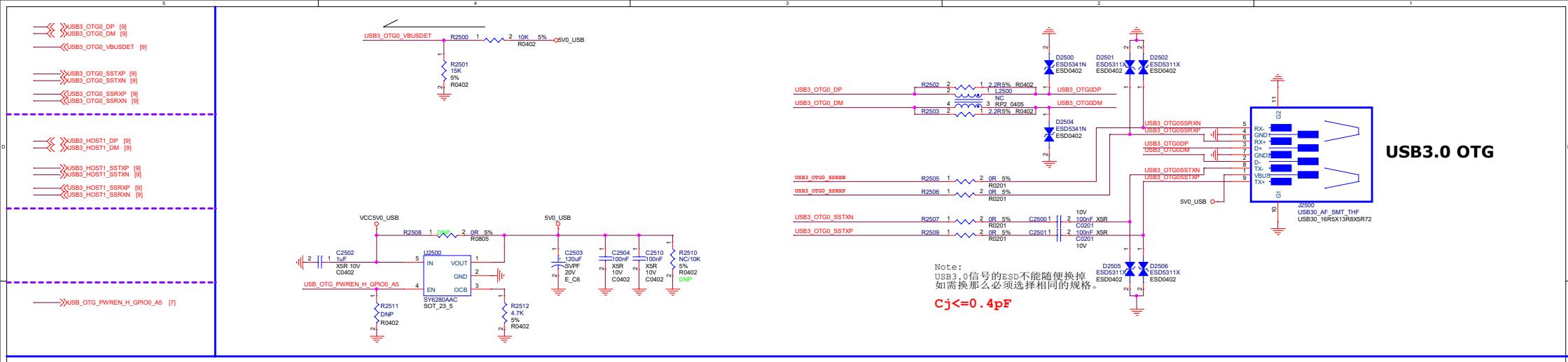
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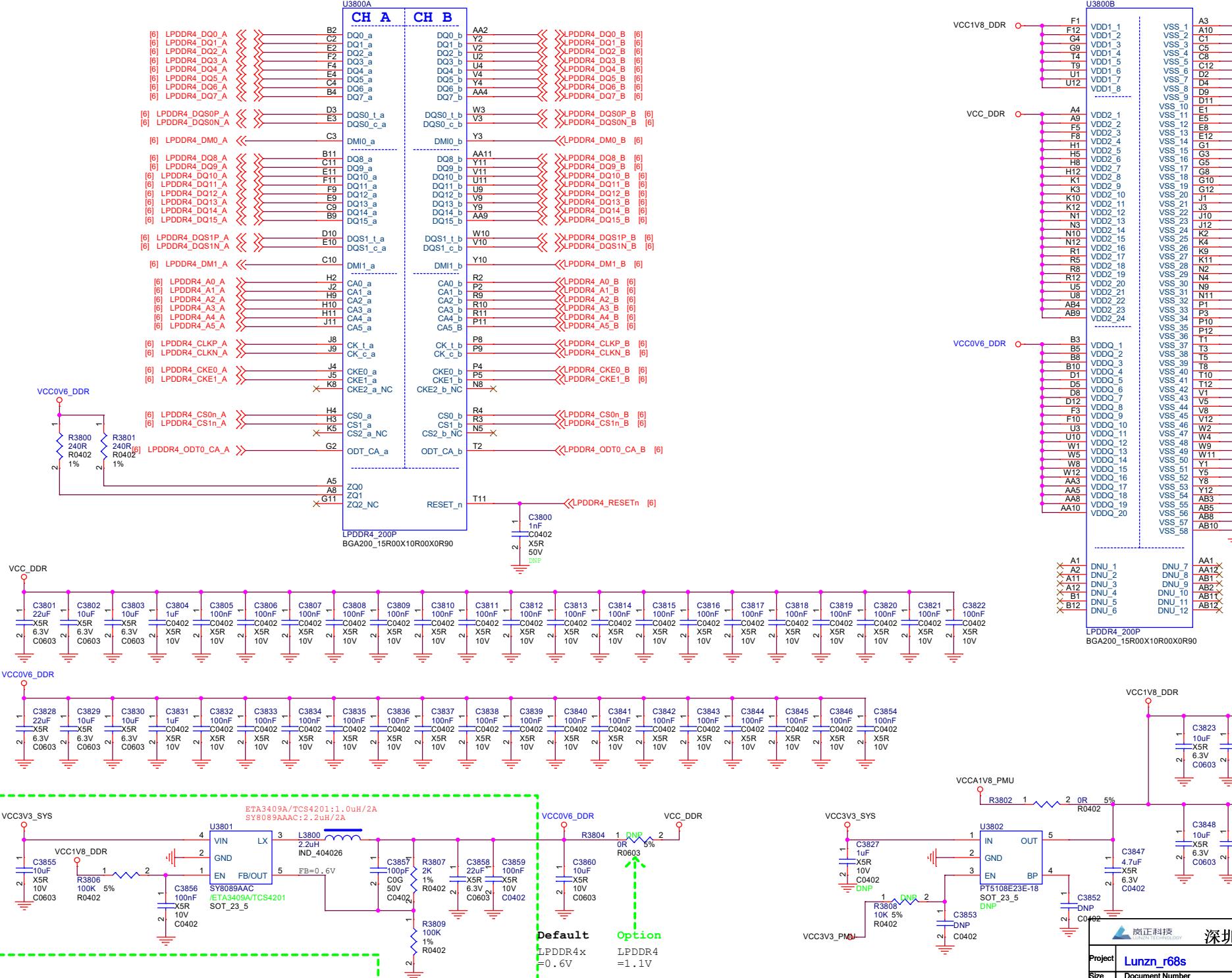
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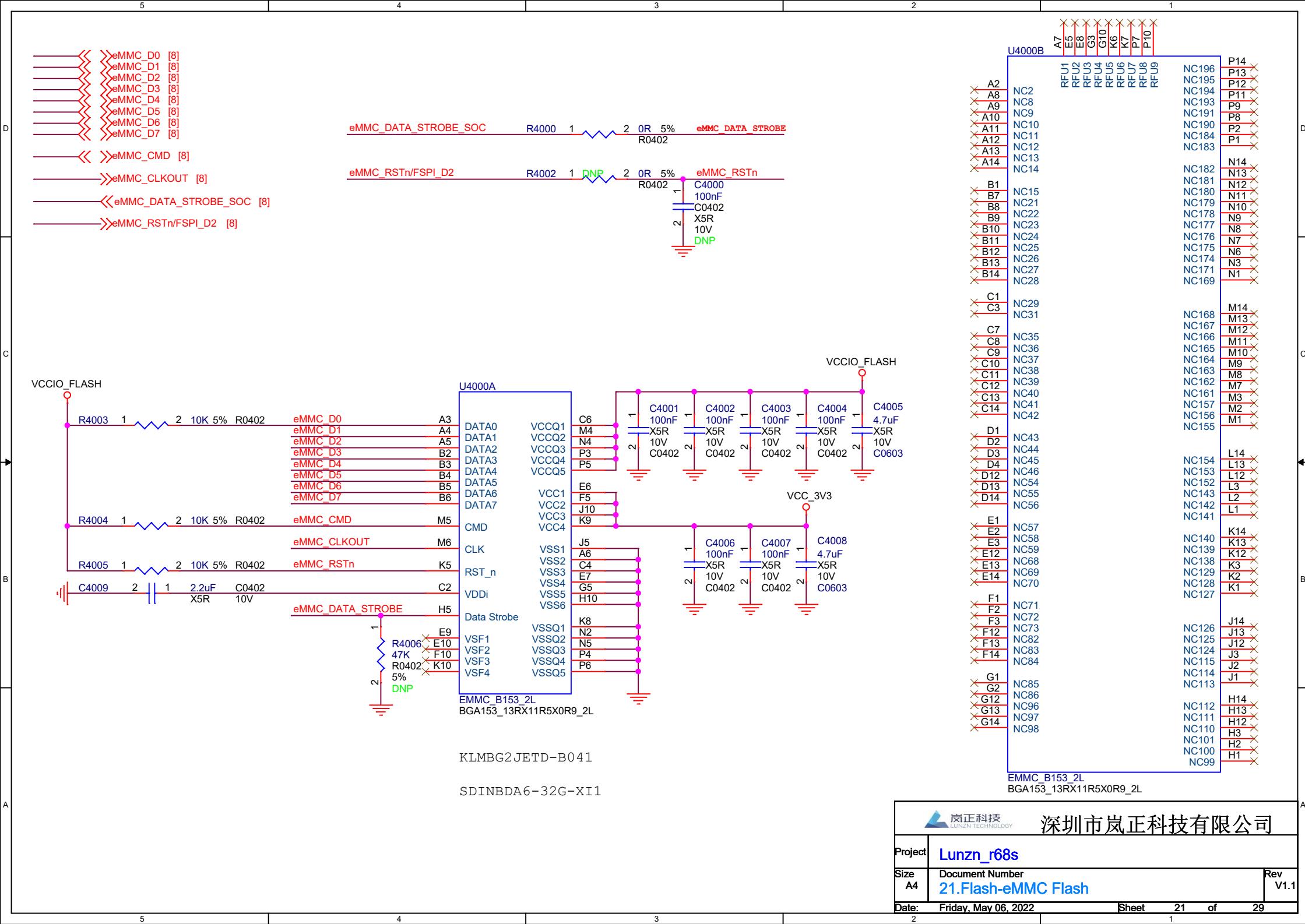


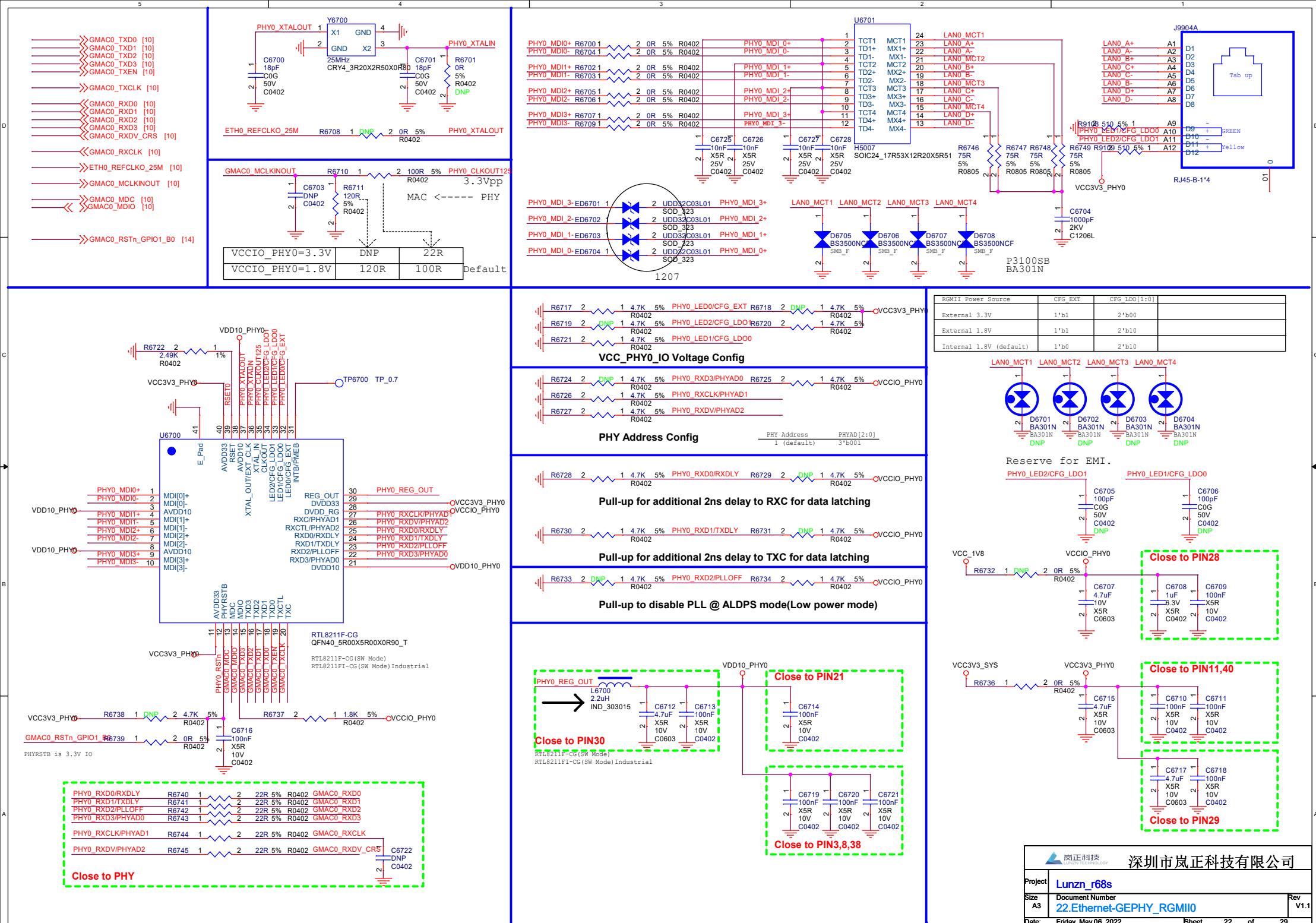


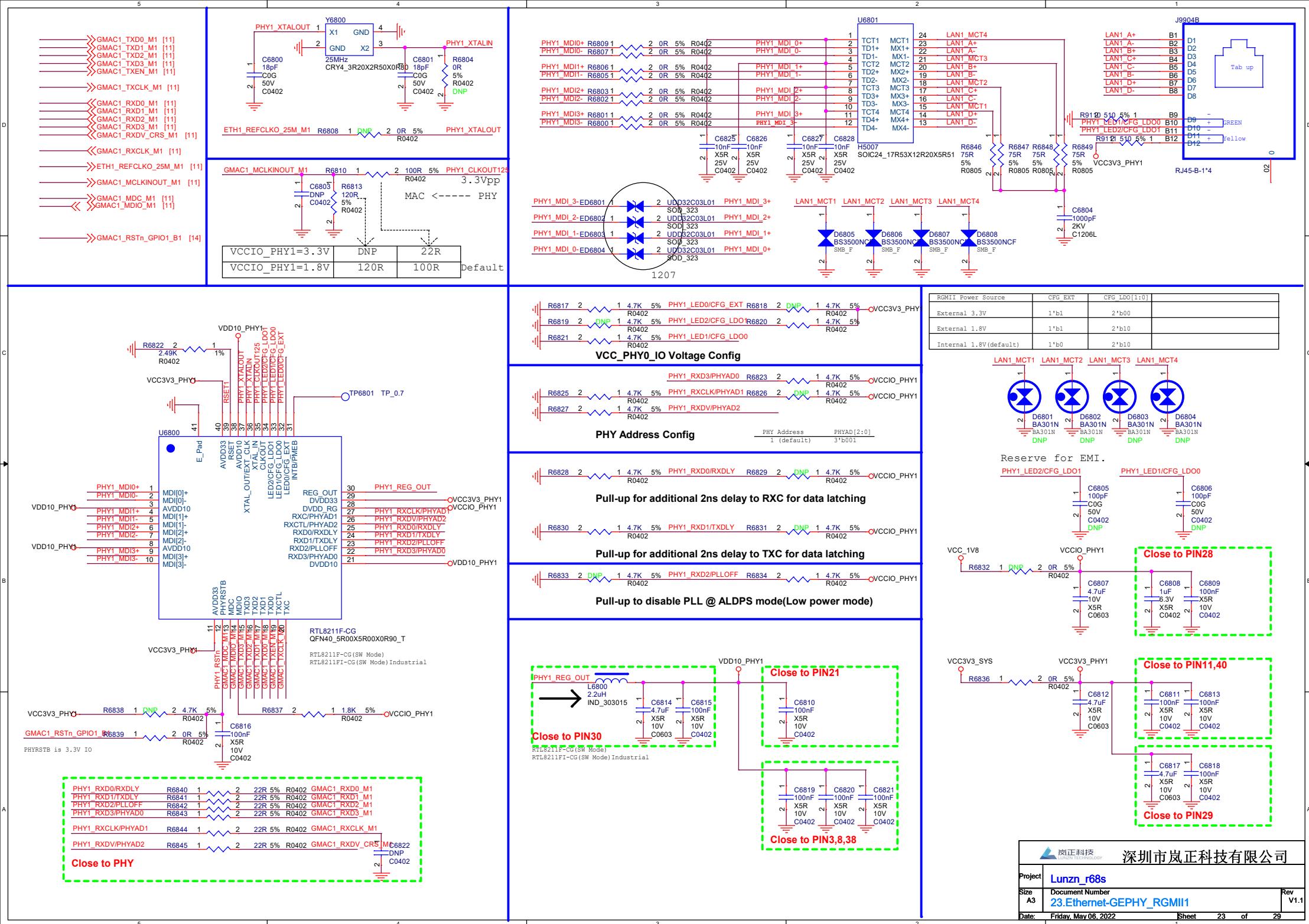
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UDRAM-LPDDR4X_1X32bit_200P V1.1
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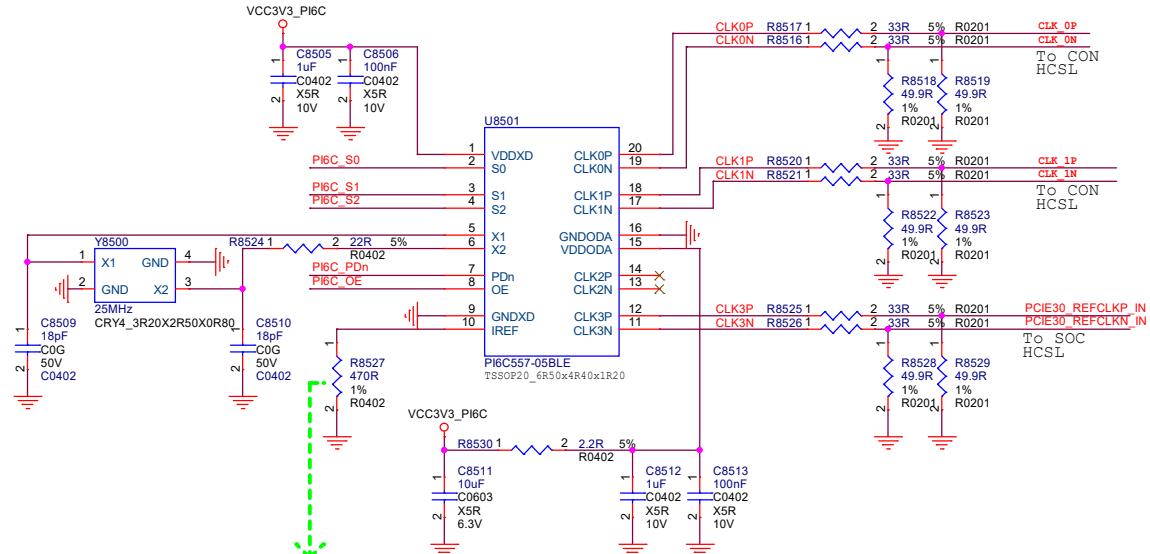
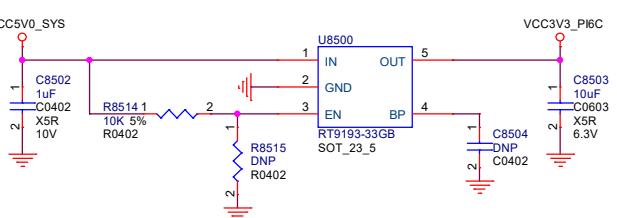
PCIE30_REFCLKP_IN [9]

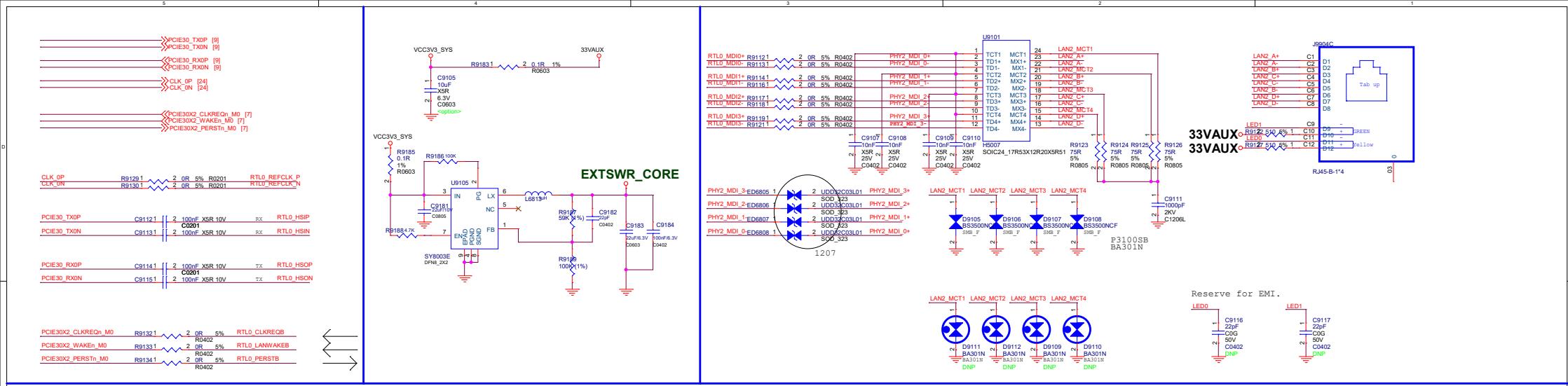
CLK_0P [25]

CLK_1P [26]

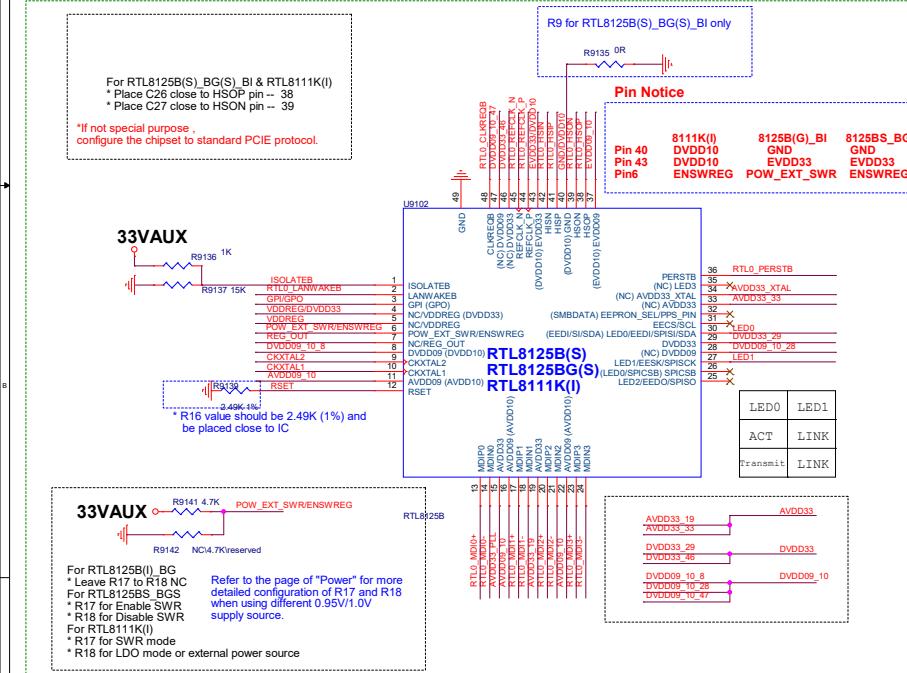
CLK_1N [26]

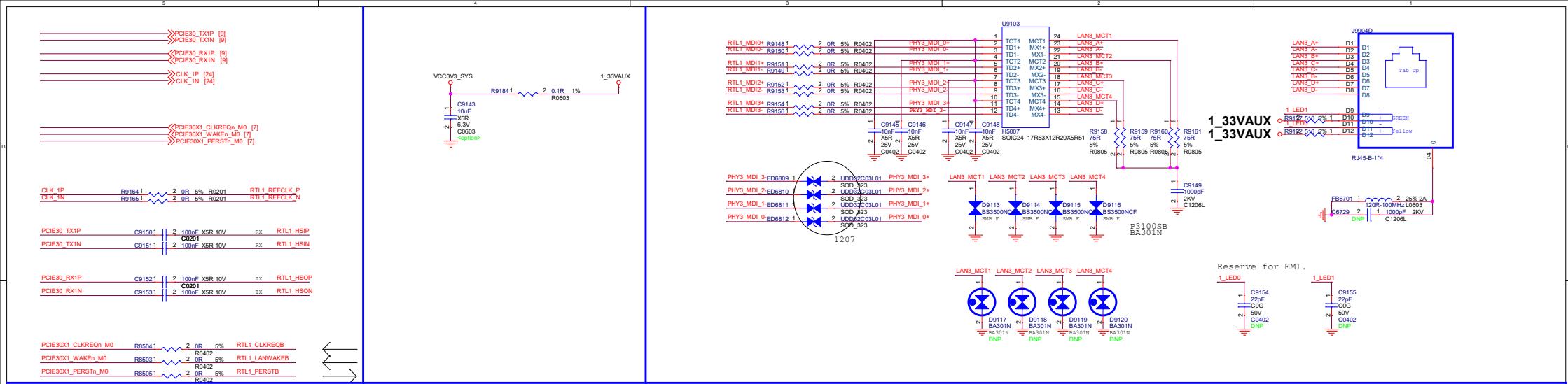
PI6C_S2	PI6C_S1	PI6C_S0	Spread %	Out Freq	
0	0	0	-0.5	100MHz	
0	0	1	-1.0	100MHz	
0	1	0	-1.5	100MHz	
0	1	1	No Spread	100MHz	
VCC3V3_PI6C	R8506 1	DNP	2 10K 5% R0402	PI6C_S2 R8507 1	2 10K 5% R0402
VCC3V3_PI6C	R8508 1	DNP	2 10K 5% R0402	PI6C_S0 R8509 1	DNP 2 10K 5% R0402
VCC3V3_PI6C	R8510 1	DNP	2 10K 5% R0402	PI6C_S1 R8511 1	DNP 2 10K 5% R0402
VCC3V3_PI6C	R8512 1	DNP	2 4.7K 5% R0402	PI6C_Pdn	
VCC3V3_PI6C	R8513 1	DNP	2 10K 5% R0402	PI6C_OE	



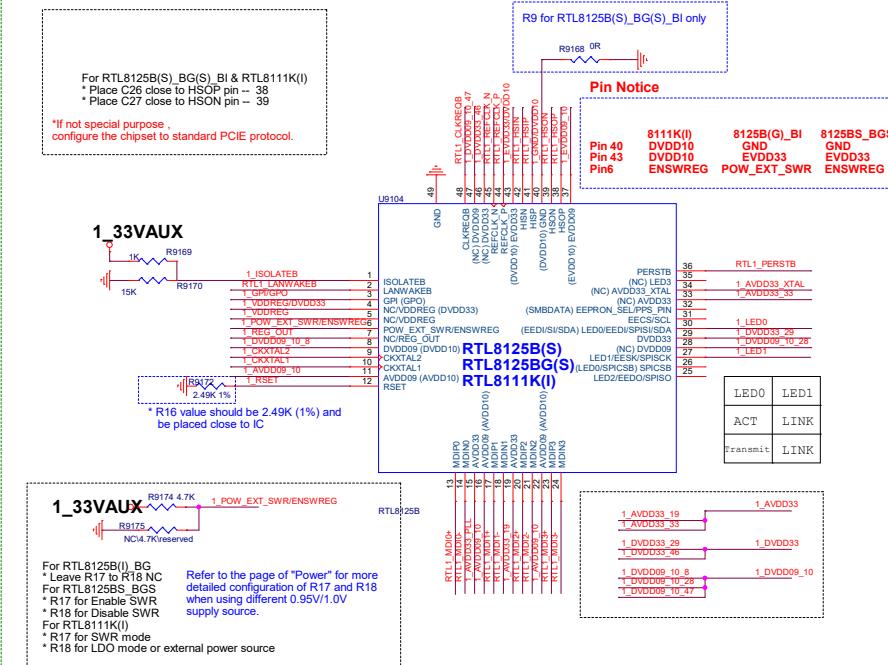


Ethernet PHY



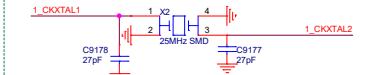


Ethernet PHY



Clock Source

Please must be use SMD type XTAL for RTL8125B(S)_BG(S)_BI



Refer to the page of "Reserved Components" for External Clock Source

For RTL8125B(S)_BG(S)_BI
R27 is based on the XTAI drive level spec to choose

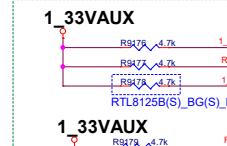
R27 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R25 on CKXTAL1 patch.

R25 is based on the XTAL drive level spec to choose

R25 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R27 on CKXTAL2 patch.

the appropriate resistor. Do not cascade R27 on CRAYTALL patch.

External Resistor



R29 PII for normal application

1_33VAUX

For RTL8125B(S)_BG(S)_BI & RTL8111K(I)

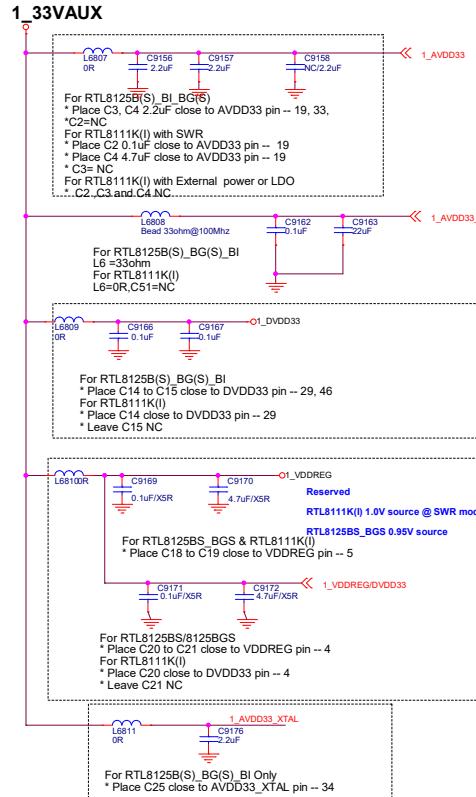
* R26 is needed for ensuring IC normal operation mode.

* R28, R30 could be saved by s

R₂₈, R₃₀ could be saved by using the pull-up resistors which might

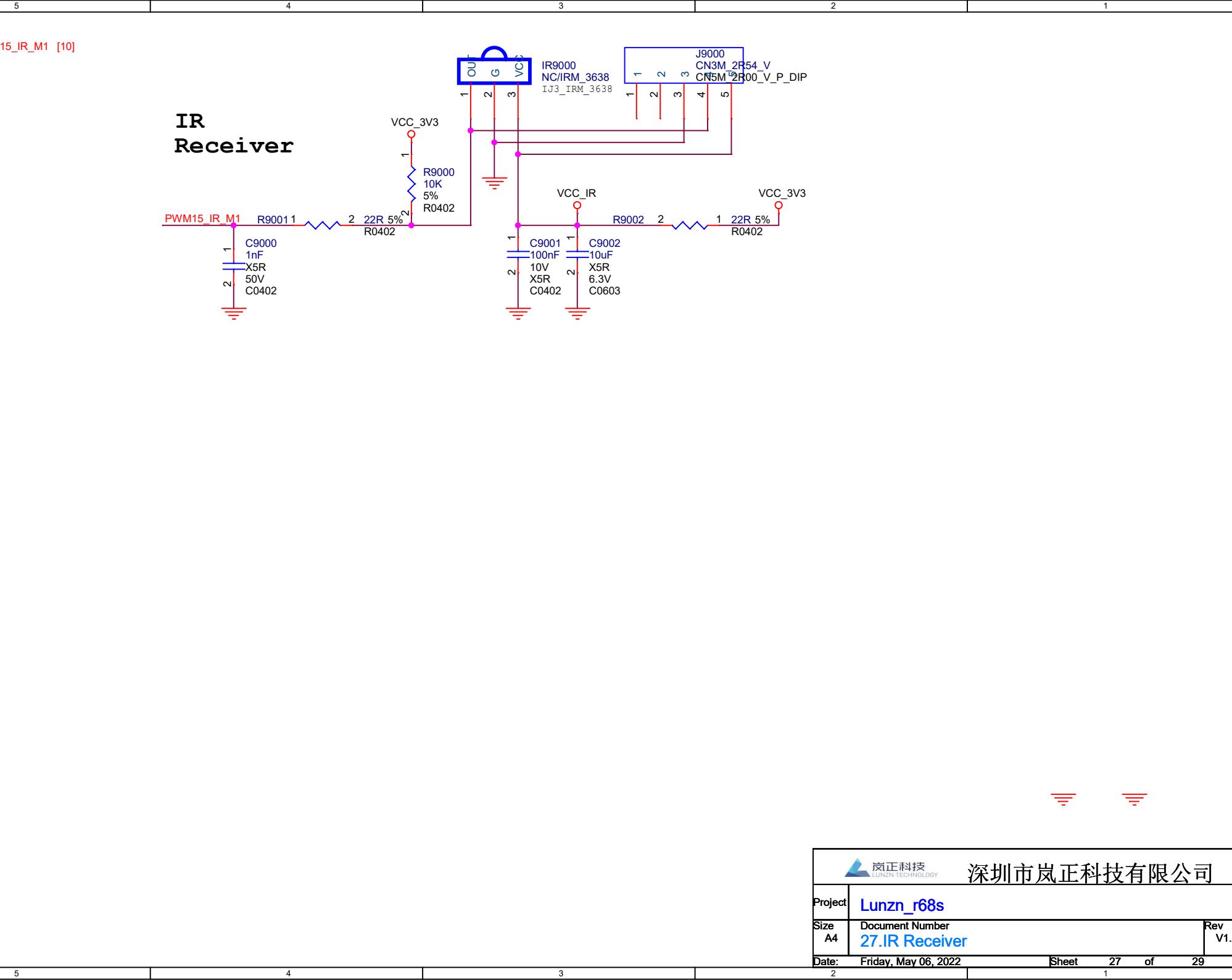
existed on the chipset side already.

3.3V



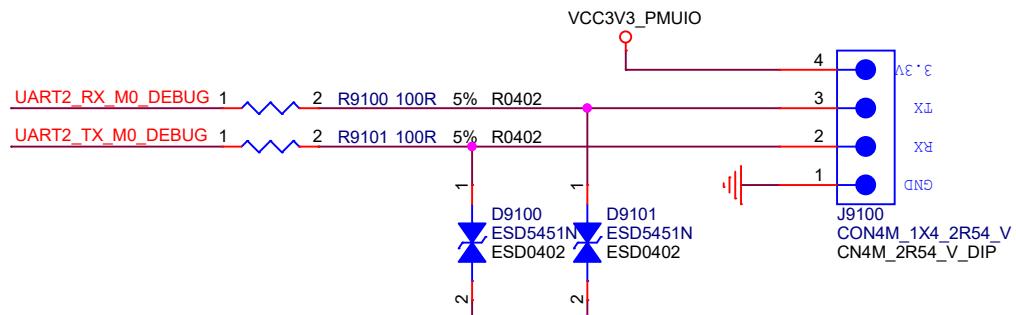
Core Source Option





UART2_RX_M0_DEBUG [7]
UART2_TX_M0_DEBUG [7]

Debug UART2



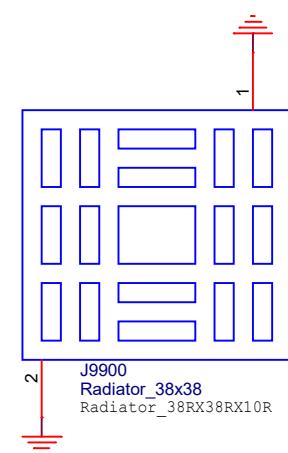
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Project	Lunzn_r68s
Size	Document Number 28.Debug UART
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5 4 3 2 1
H9900 HOLE_3R20
HOLE_C3R20_C6R00

H9901 HOLE_3R20
HOLE_C3R20_C6R00

H9902 HOLE_3R20
HOLE_C3R20_C6R00

H9903 HOLE_3R20
HOLE_C3R20_C6R00



TOP Mark
M9900 MARK MARK
M9901 MARK MARK
M9902 MARK MARK

BOTTOM Mark
M9903 MARK MARK
M9904 MARK MARK
M9905 MARK MARK

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深圳市岚正科技有限公司	
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