SX3 HDMI 4K Capture Card

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Drawing Numbers	
PCBA	121-60612-01
PCB	600-60612-01
FAB DRW	610-60612-01
ASSY DRW	620-60612-01
SCH DRW	630-60612-01

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SCH Title : SX3 HDMI 4K Capture Card

Page Title : Title Page

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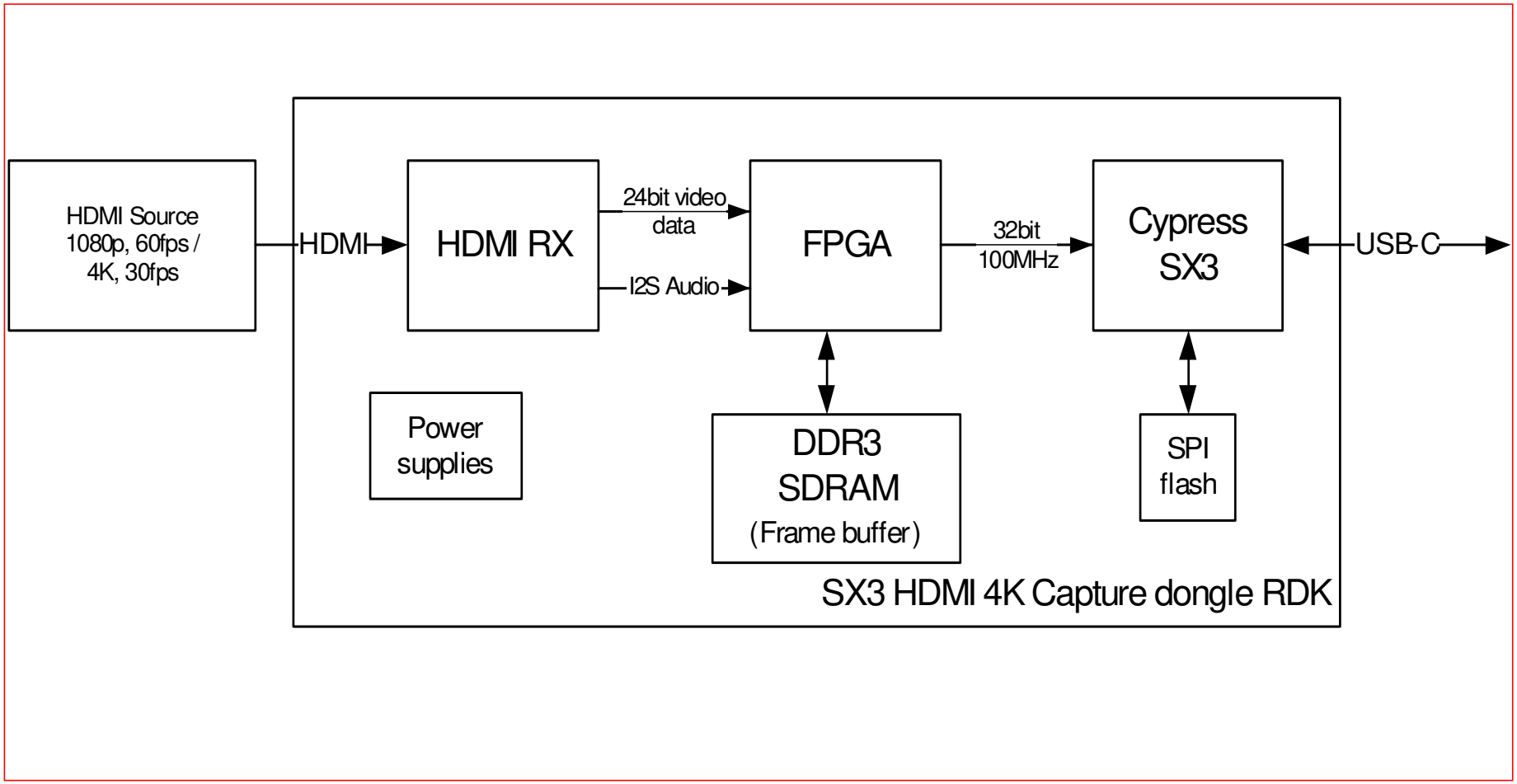

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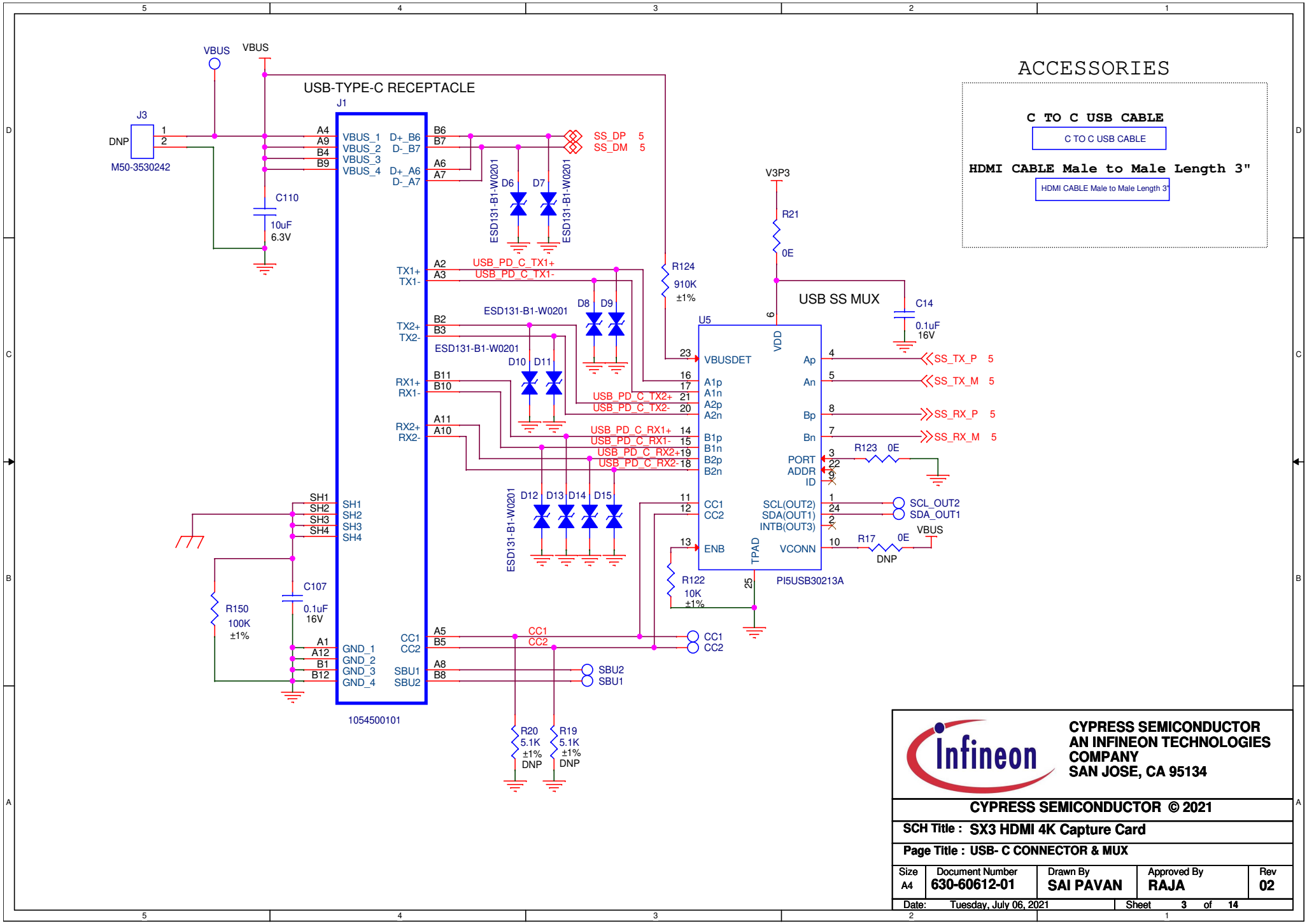
ACCESSORIES
C TO C USB CABLE
C TO C USB CABLE
HDMI CABLE Male to Male Length 3"
HDMI CABLE Male to Male Length 3"
USB-TYPE-C RECEPTACLE
J1
J3
DNP
M50-3530242
VBUS
C110
10uF
6.3V
ESD131-B1-W0201
D6
D7
SS_DP 5
SS_DM 5
USB_PD_C_TX1+
USB_PD_C_TX1-
D8
D9
R124
910K
±1%
V3P3
R21
0E
USB SS MUX
U5
C14
0.1uF
16V
VBUSDET
VDD
PI5USB30213A
SS_TX_P 5
SS_TX_M 5
SS_RX_P 5
SS_RX_M 5
R123 0E
SCL_OUT2
SDA_OUT1
R17 0E
DNP
USB_PD_C_TX2+
USB_PD_C_TX2-
USB_PD_C_RX1+
USB_PD_C_RX1-
USB_PD_C_RX2+
USB_PD_C_RX2-
D10
D11
D12
D13
D14
D15
R122
10K
±1%
TPAD
C107
0.1uF
16V
R150
100K
±1%
CC1
CC2
SBU1
SBU2
R20
5.1K
±1%
DNP
R19
5.1K
±1%
DNP
1054500101
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SCH Title : SX3 HDMI 4K Capture Card
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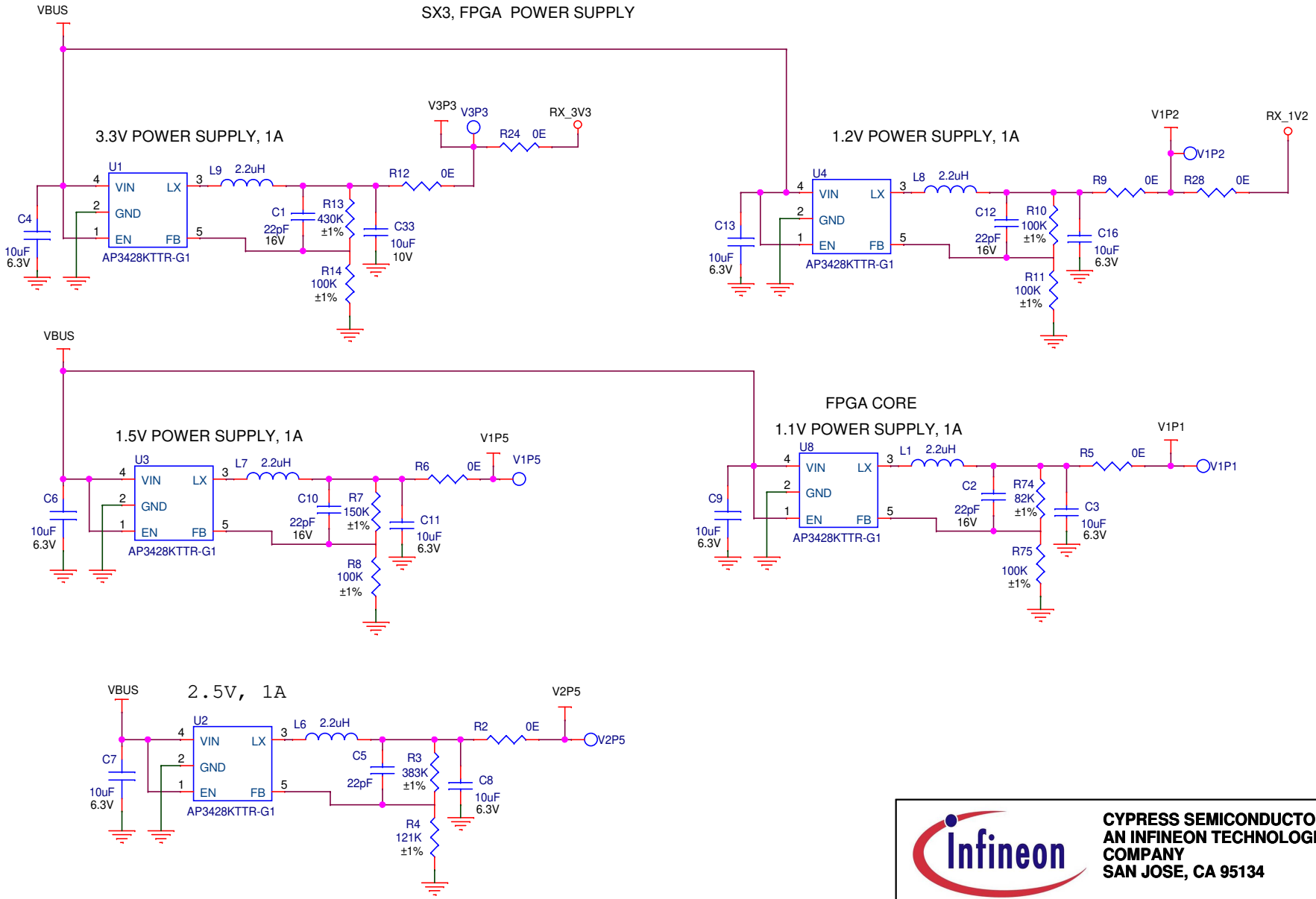
SX3, FPGA POWER SUPPLY



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SCH Title : SX3 HDMI 4K Capture Card				
Page Title : SX3,FPGA-POWER SUPPLY				
Size: A4	Document Number: 630-60612-01	Drawn By: SAI PAVAN	Approved By: RAJA	Rev: 02
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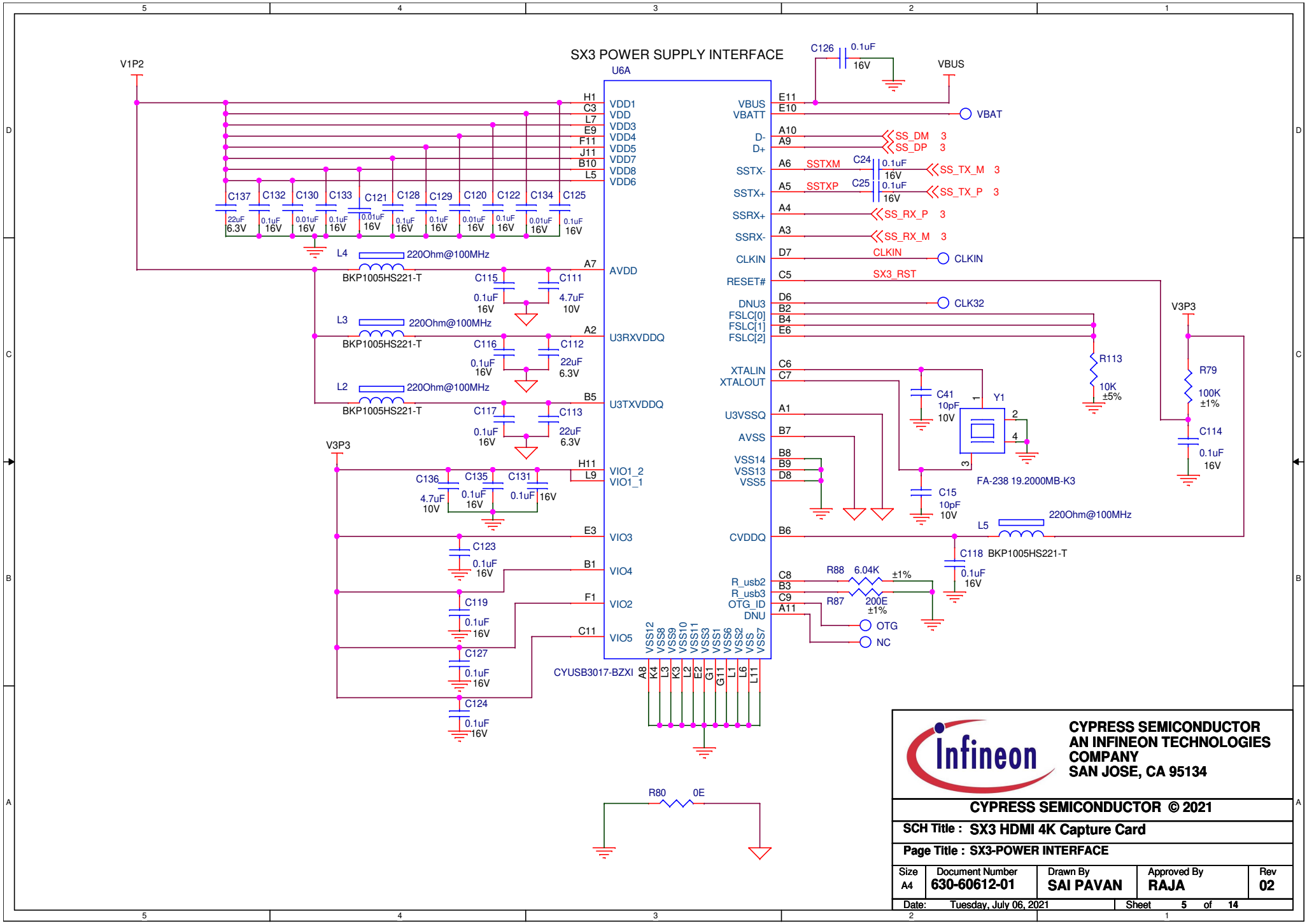

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Page Title : SX3-POWER INTERFACE				
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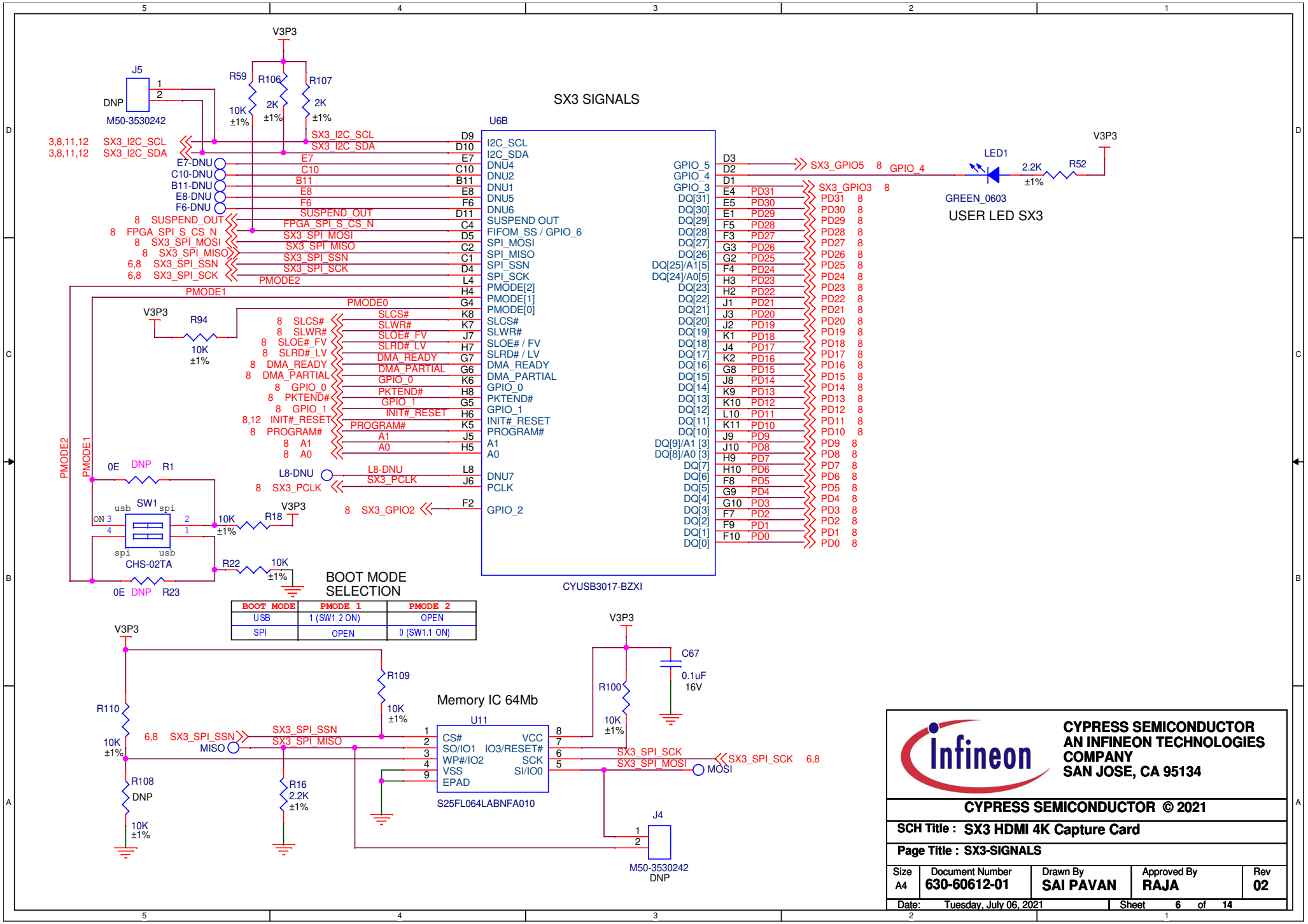

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Page Title :	SX3-SIGNALS

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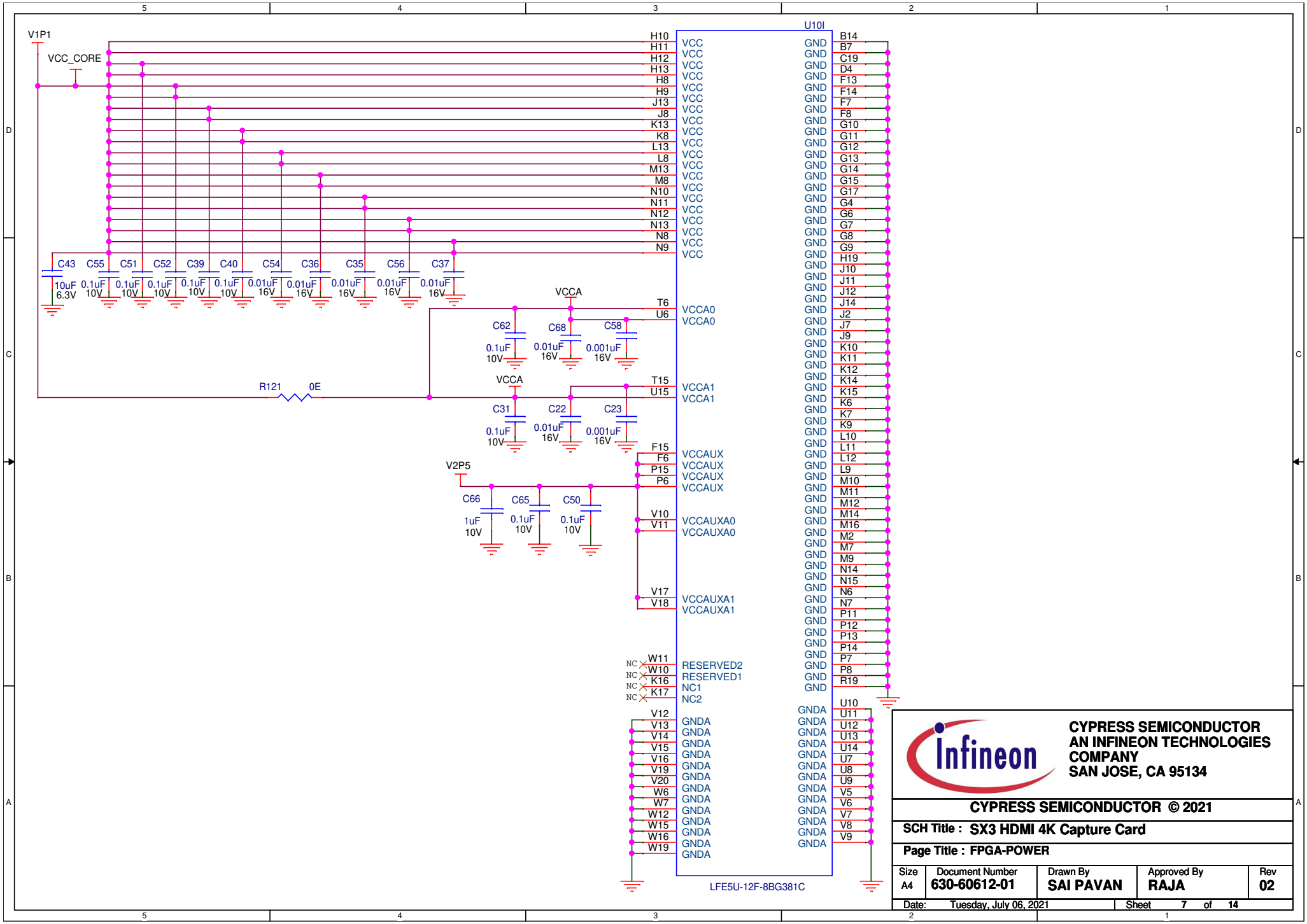

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Page Title : FPGA-POWER

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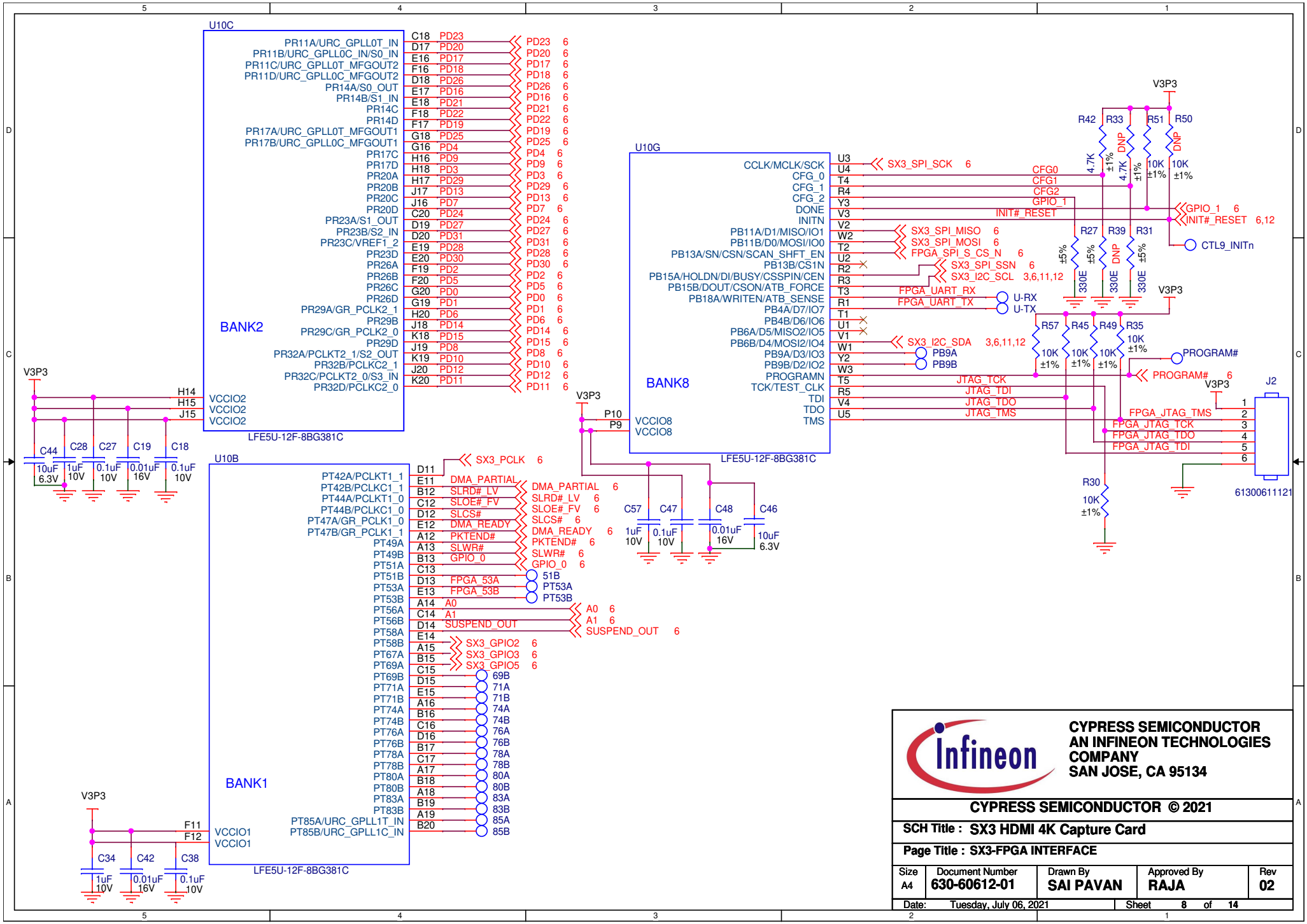
U10C
BANK2
LFE5U-12F-8BG381C
U10G
BANK8
LFE5U-12F-8BG381C
U10B
BANK1
LFE5U-12F-8BG381C
V3P3
J2
61300611121
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Page Title : SX3-FPGA INTERFACE
Size A4
Document Number 630-60612-01
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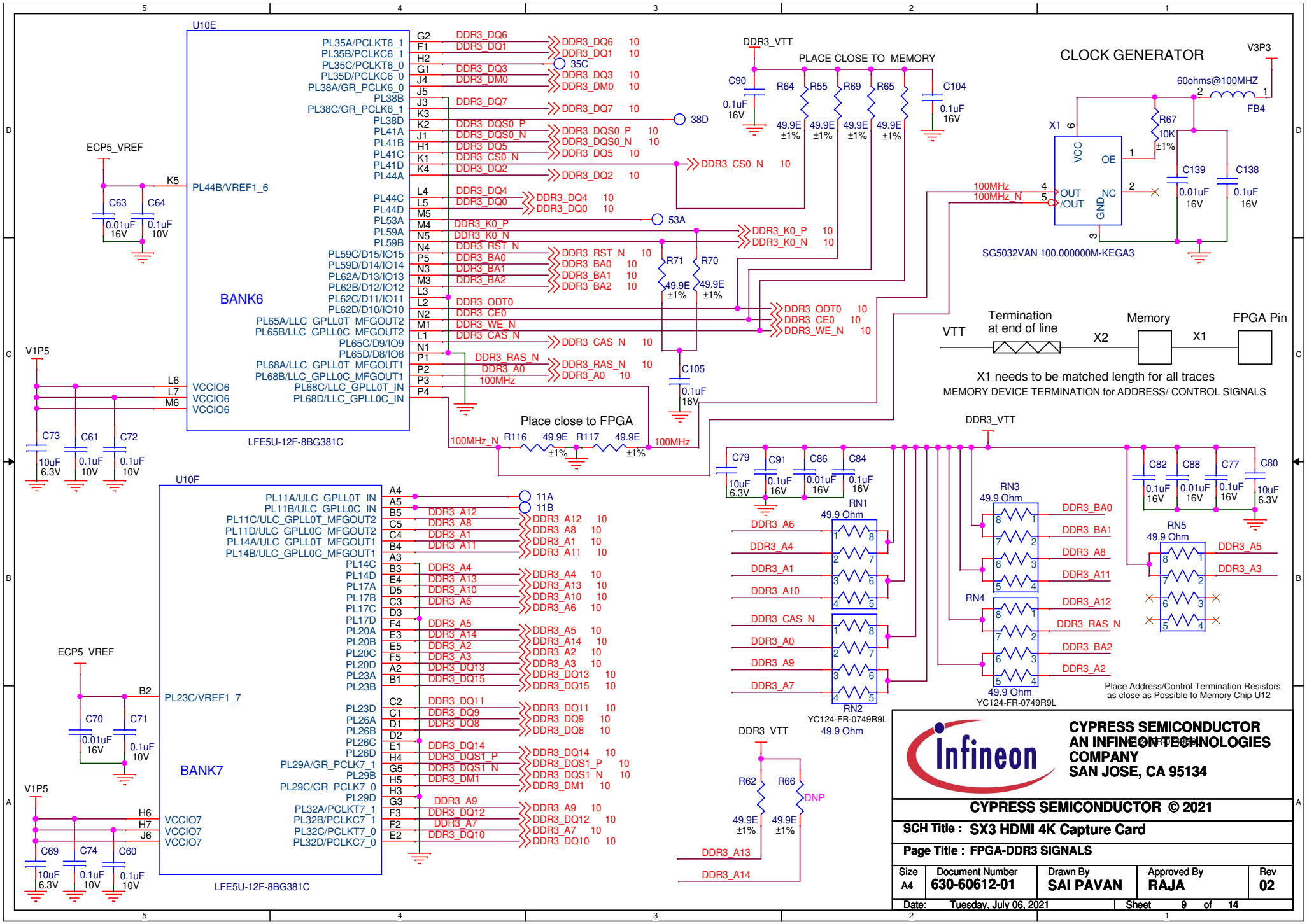
U10E
BANK6
LFE5U-12F-8BG381C
U10F
BANK7
LFE5U-12F-8BG381C
ECP5_VREF
PL44B/VREF1_6
PL23C/VREF1_7
V1P5
VCCIO6
VCCIO7
DDR3_VTT
PLACE CLOSE TO MEMORY
CLOCK GENERATOR
V3P3
60ohms@100MHZ
FB4
SG5032VAN 100.000000M-KEGA3
Termination at end of line
Memory
FPGA Pin
VTT
X2
X1
X1 needs to be matched length for all traces
MEMORY DEVICE TERMINATION for ADDRESS/ CONTROL SIGNALS
Place close to FPGA
100MHz_N
100MHz
RN1
RN2
RN3
RN4
RN5
49.9 Ohm
YC124-FR-0749R9L
Place Address/Control Termination Resistors as close as Possible to Memory Chip U12
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Page Title : FPGA-DDR3 SIGNALS
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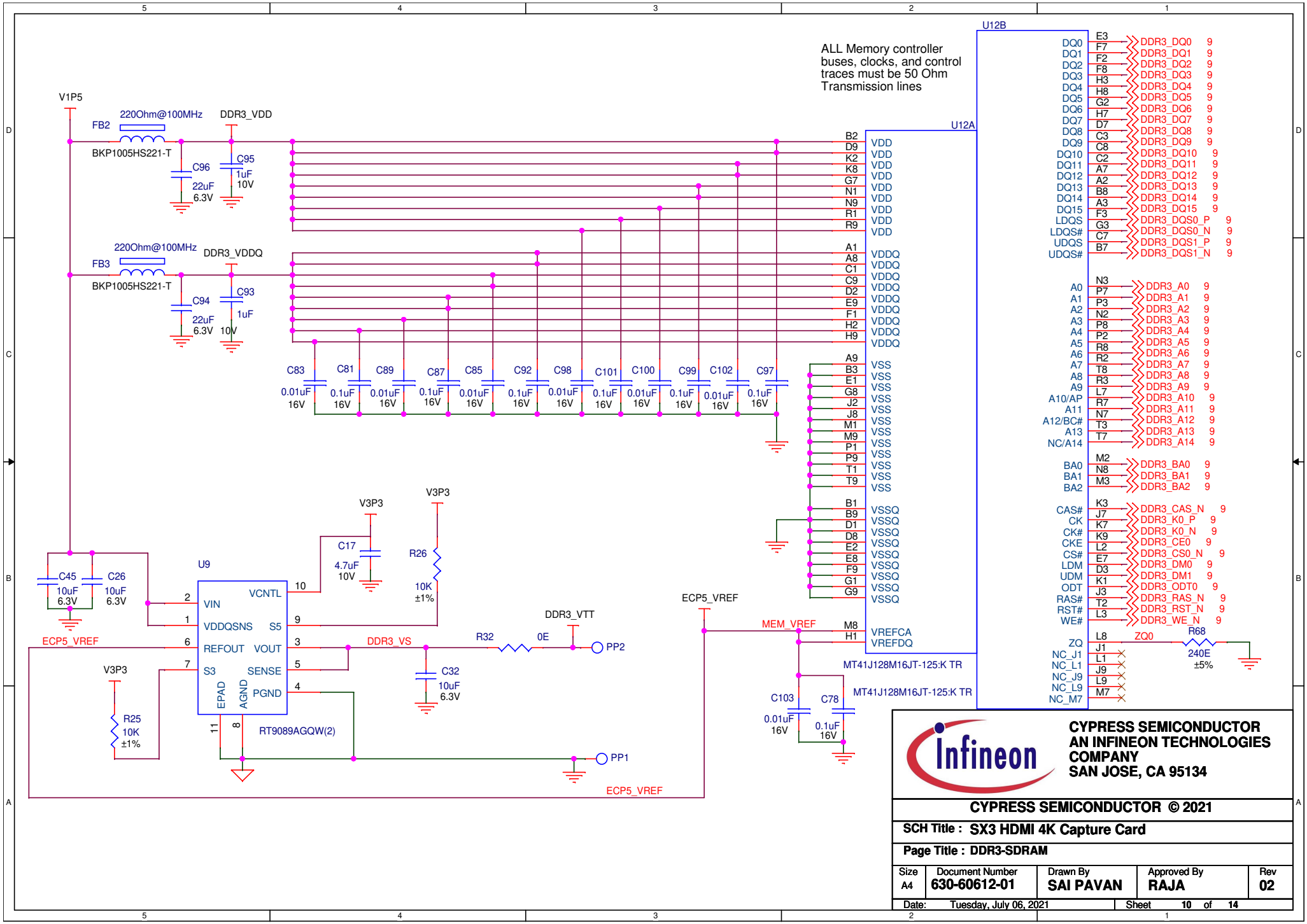
ALL Memory controller buses, clocks, and control traces must be 50 Ohm Transmission lines
V1P5
FB2
220Ohm@100MHz
BKP1005HS221-T
DDR3_VDD
C96
22uF
6.3V
C95
1uF
10V
FB3
220Ohm@100MHz
BKP1005HS221-T
DDR3_VDDQ
C94
22uF
6.3V
C93
1uF
10V
U12A
VDD
VDDQ
VSS
VSSQ
U12B
DDR3_DQ0
DDR3_DQ1
DDR3_DQ2
DDR3_DQ3
DDR3_DQ4
DDR3_DQ5
DDR3_DQ6
DDR3_DQ7
DDR3_DQ8
DDR3_DQ9
DDR3_DQ10
DDR3_DQ11
DDR3_DQ12
DDR3_DQ13
DDR3_DQ14
DDR3_DQ15
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_A0
DDR3_A1
DDR3_A2
DDR3_A3
DDR3_A4
DDR3_A5
DDR3_A6
DDR3_A7
DDR3_A8
DDR3_A9
DDR3_A10
DDR3_A11
DDR3_A12
DDR3_A13
DDR3_A14
DDR3_BA0
DDR3_BA1
DDR3_BA2
DDR3_CAS_N
DDR3_K0_P
DDR3_K0_N
DDR3_CE0
DDR3_CS0_N
DDR3_DM0
DDR3_DM1
DDR3_ODT0
DDR3_RAS_N
DDR3_RST_N
DDR3_WE_N
ZQ0
R68
240E
±5%
MT41J128M16JT-125:K TR
C83
C81
C89
C87
C85
C92
C98
C101
C100
C99
C102
C97
0.01uF
0.1uF
16V
C45
C26
10uF
6.3V
U9
VIN
VDDQSNS
REFOUT
S3
VCNTL
S5
VOUT
SENSE
PGND
EPAD
AGND
RT9089AGQW(2)
C17
4.7uF
10V
R26
10K
±1%
R25
10K
±1%
V3P3
ECP5_VREF
DDR3_VS
R32
0E
DDR3_VTT
PP2
PP1
C32
10uF
6.3V
MEM_VREF
VREFCA
VREFDQ
C103
C78
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Page Title : DDR3-SDRAM
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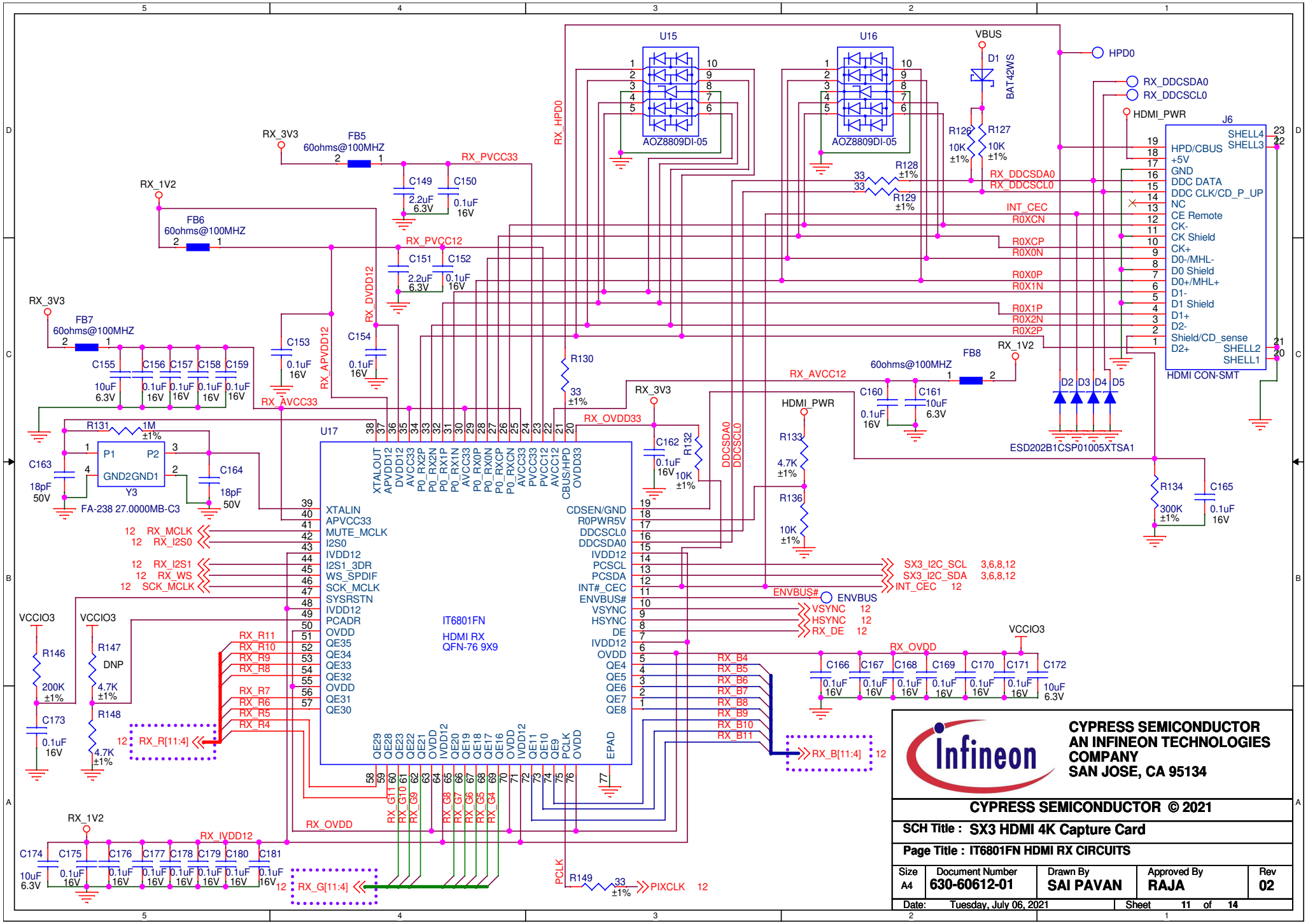
U15
AOZ8809DI-05
U16
AOZ8809DI-05
VBUS
D1
BAT42WS
HPD0
RX_DDCSDA0
RX_DDCSCL0
HDMI_PWR
J6
HDMI CON-SMT
HPD/CBUS
+5V
GND
DDC DATA
DDC CLK/CD_P_UP
NC
CE Remote
CK-
CK Shield
CK+
D0-/MHL-
D0 Shield
D0+/MHL+
D1-
D1 Shield
D1+
D2-
Shield/CD_sense
D2+
SHELL4
SHELL3
SHELL2
SHELL1
R126
10K ±1%
R127
10K ±1%
R128
33 ±1%
R129
33 ±1%
INT_CEC
R0XCN
R0XCP
R0X0N
R0X0P
R0X1N
R0X1P
R0X2N
R0X2P
RX_1V2
FB8
60ohms@100MHZ
C160
0.1uF 16V
C161
10uF 6.3V
D2 D3 D4 D5
ESD202B1CSP01005XTSA1
R134
300K ±1%
C165
0.1uF 16V
RX_3V3
FB5
60ohms@100MHZ
RX_PVCC33
C149
2.2uF 6.3V
C150
0.1uF 16V
RX_1V2
FB6
60ohms@100MHZ
RX_PVCC12
C151
2.2uF 6.3V
C152
0.1uF 16V
RX_3V3
FB7
60ohms@100MHZ
C155
10uF 6.3V
C156
0.1uF 16V
C157
0.1uF 16V
C158
0.1uF 16V
C159
0.1uF 16V
C153
0.1uF 16V
C154
0.1uF 16V
RX_APVDD12
RX_DVDD12
RX_AVCC33
R130
33 ±1%
RX_3V3
RX_OVDD33
C162
0.1uF 16V
R132
10K ±1%
R131
1M ±1%
C163
18pF 50V
C164
18pF 50V
Y3
FA-238 27.0000MB-C3
U17
IT6801FN
HDMI RX
QFN-76 9X9
XTALIN
APVCC33
MUTE_MCLK
I2S0
IVDD12
I2S1_3DR
WS_SPDIF
SCK_MCLK
SYSRSTN
IVDD12
PCADR
OVDD
QE35
QE34
QE33
QE32
OVDD
QE31
QE30
CDSEN/GND
R0PWR5V
DDCSCL0
DDCSDA0
IVDD12
PCSCL
PCSDA
INT#_CEC
ENVBUS#
VSYNC
HSYNC
DE
IVDD12
OVDD
QE4
QE5
QE6
QE7
QE8
EPAD
DDCSDA0
DDCSCL0
HDMI_PWR
R133
4.7K ±1%
R136
10K ±1%
ENVBUS#
ENVBUS
12 RX_MCLK
12 RX_I2S0
12 RX_I2S1
12 RX_WS
12 SCK_MCLK
SX3_I2C_SCL 3,6,8,12
SX3_I2C_SDA 3,6,8,12
INT_CEC 12
VSYNC 12
HSYNC 12
RX_DE 12
VCCIO3
VCCIO3
R146
200K ±1%
R147
DNP
4.7K ±1%
R148
4.7K ±1%
C173
0.1uF 16V
RX_R11
RX_R10
RX_R9
RX_R8
RX_R7
RX_R6
RX_R5
RX_R4
12 RX_R[11:4]
RX_B4
RX_B5
RX_B6
RX_B7
RX_B8
RX_B9
RX_B10
RX_B11
RX_B[11:4] 12
RX_OVDD
C166
C167
C168
C169
C170
C171
C172
0.1uF 16V
10uF 6.3V
VCCIO3
RX_1V2
RX_IVDD12
C174
C175
C176
C177
C178
C179
C180
C181
10uF 6.3V
0.1uF 16V
RX_OVDD
RX_G11
RX_G10
RX_G9
RX_G8
RX_G7
RX_G6
RX_G5
RX_G4
12 RX_G[11:4]
PCLK
R149
33 ±1%
PIXCLK 12
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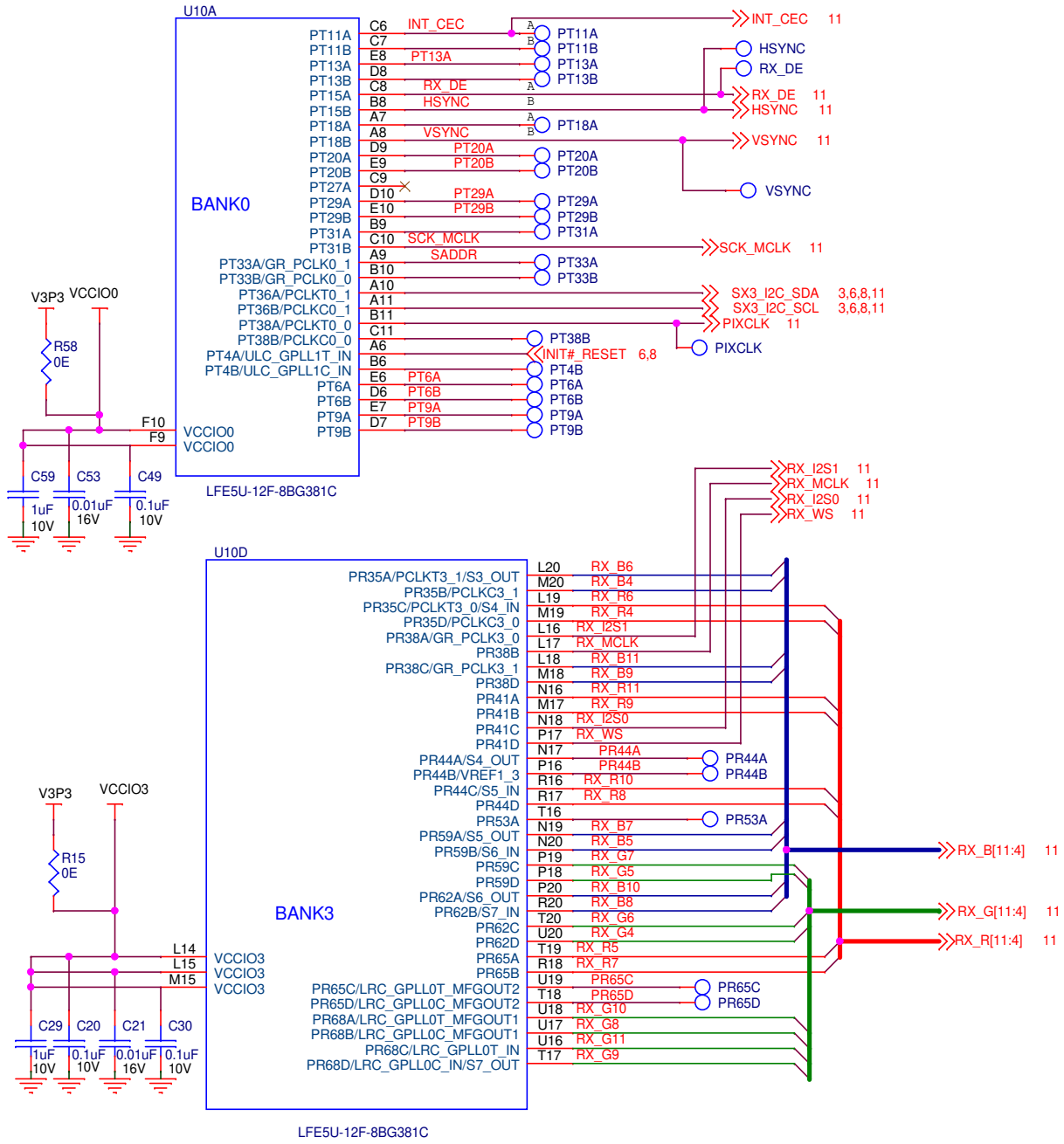
FPGA INTERFACE



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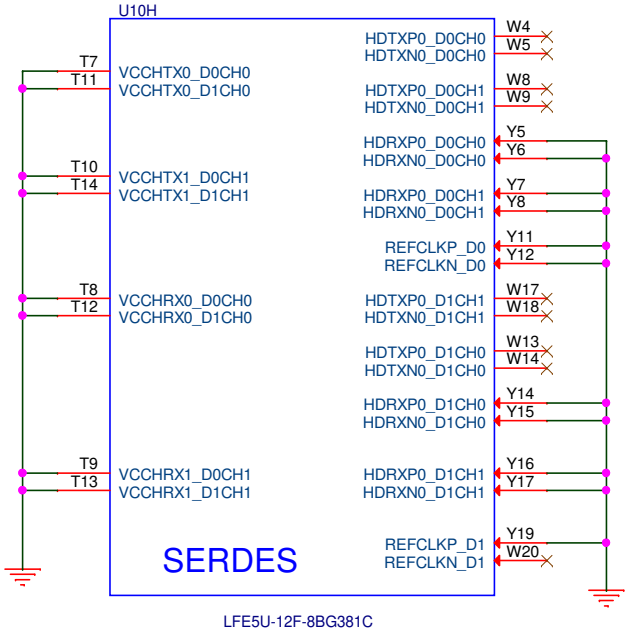

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Page Title : FPGA-SERDES (NOT USED)

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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Release	13/JULY/2020
02	1.Connected V5P0_J2 to VBUS. 2.Added DIP Switch SW1 & related circuits. 3.Connected S3 and S5 to Pullup Configuration. 4.Changed J2 JTAG connector from 1.27mm pitch 7pin to 2.54mm pitch with 5 pin. 5.SX3 pin names H6,K5 were Updated as INIT#_RESET,PROGRAM# 6.Added R28 0E in series to V1P2 & RX_1V2. 7.HDMI connector CN1 ref. changed as J6. 8.INIT#_RESET updated in 6,8 and 12th page 9.J2 connector updated as 6pin connector. 10.Replacement of SPI Flash to New Part (S25FL064LABNFA010) 11.Replacement of J1 Connecter to New Part (1054500101) 12.Replacement of FPGA U10 to New Part (LFE5U-12F-8BG381C)	19/MAR/2021

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