Houman Homayoun

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Irvine, California
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(949) 419-7457

RELEVANT EXPERIENCE

§ Design Architect
NOVELICS, Aliso Viejo, California, January 2007-October 2008.
Principal Designer of a parametrizable BIST microcontroller for testing different memories. Synthesizing, floor planning, power planning and place and routing in TSMC 90nm and IBM 65nm std cell libraries using Cadence Nano-Encounter, RTL Compiler and Synopsys DC Compiler and Astro. Automating the entire design flow using Perl. Successfully post-fabrication testing. Cooperating in design and verification of different embedded memories such as DRAMs and SRAMs.

§ Research Assistant
Center for Embedded Computer Systems, University of California Irvine, September 2006-Present.
Conducting research on reducing leakage power and temperature in memory, specifically peripheral circuits of L2 cache in high performance processors. Investigating architectural support for hardware resource adaptation in high performance and embedded processors.

§ Design/Firmware Engineer
Pishgam Tousee Niroo Co., Tehran, Iran, May 2005-September 2005.
Designed the controller part of a commercial display monitor using Motorola Microcontroller 68000 series. Designed & implemented embedded firmware running in the system.

§ Research Assistant
Computer Engineering Department, McMaster University, Canada, October 2005-April 2006.
Collaborated in designing a low power 5.12 Terabit capacity single-chip optoelectronic VLSI crossbar switch using 0.18 µm CMOS technology. Using LabVIEW and DAQ boards for real-time computer control.

§ Research Assistant
Computer Engineering Department, University of Victoria, Canada, September 2003-March 2005.
Developed software to simulate different variety of microprocessors and embedded systems. Developing microarchitectural techniques to increase performance and reduce power dissipation in Intel XScale processor.

§ Research Engineer
Electronic Research Center, Sharif University of Technology, Iran, October 2002-June 2003.
Collaborated in designing a data acquisition system with appliance of a 16 bit Intel 196 family microcontroller as controller/supervisor and a 32 bit 6711 TI series DSP as a processor unit.

§ Service Technician
Internship Position, Sinatech Co.Ltd Repair Section, Tehran, Iran, November 2001-April 2002.
Troubleshooting medical and research laboratory appliances such as Gas Chromatography Systems, Atomic Absorption spectrophotometry Instruments, all kind of Flash Point Tester Equipments and Cell Counter Instruments.

§ Software Developer
Internship Position, Mahab Ghods Company, Tehran, Iran, April 2001-Julyl 2001.
Implementation and design of HMI for management information system server and client application. Adding database modules and web server to management information system.

SELECTED PUBLICATION

Peer-reviewed Publications/Under Review

2010

(32) *"RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor*".
Houman Homayoun, Aseem Gupta, Alex Veidenbaum, Fadi J. Kurdahi, Nikil Dutt.
5th International Conference of High Performance Embedded Architectures and Compilers, (*HIPEAC 2010*).

(31) "*Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks*".
Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Fadi Kurdahi, Alex Veidenbaum.
11th IEEE International Symposium on Quality Electronic Design. (ISQED).

(30) "*Reducing Peak Temperature of an Integer Register File via Access Concentration*".
Houman Homayoun, Alex Veidenbaum. (Under Review).

(29) "*Beyond Memory Cells for Leakage and Temperature Control in SRAM-based Units, the Peripheral Circuits Story*".
Houman Homayoun, Aseem Gupta, Alex Veidenbaum. (Under Review).

(28) "*Cooperative Resource resizing, Frequency Scaling and Adaptive Pipelining to Improve Embedded Processor Performance and Energy-Delay Efficiency*".
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum. (Under Submission).

(27) "*Adaptive Architectural Technique to Reduce Leakage Power in Embedded Processor Functional Unit*".
Houman Homayoun, Alex Veidenbaum, Amirali Baniasadi. (Under Submission)

(26) "*Miss Rate Product Driven Techniques for Leakage Power Management in L2 Cache Peripheral Circuits"*.
Houman Homayoun, Alex Veidenbaum and Jean-Luc Gaudiot. (Under Submission).

(25) "*Multi-Copy Cache: A Highly Energy Efficient Cache Architecture"*.
Arup Chakraborty, **Houman Homayoun**, Amin Khejah, Nikil Dutt, Ahmed Eltawil, Fadi Kurdahi. (Under Submission)

2009

(24) "*Process Variation Aware Cache for Aggressive Voltage-Frequency Scaling*".
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
Design, Autimation & Test in Europe, *DATE 2009*, Nice, France.

(23) "*Fault Tolerant Cache Architecture for Sub 500mv Operation*".
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
In Proceedings of the 2009 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2009*. Grenoble, France.

(22) "*Inquisitive Defect Cache: A Means of Combating Manufacturing Induced Process Variation*".
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (TVLSI). (Under Review)

(21) *"A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation*".
Houman Homayoun, Avesta Sasan, Alex Veidenbaum, Jean-Luc Gaudiot.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (TVLSI). (Under Review)

(20) *"MZZ-HVS: Multi Modes Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits"*.
Houman Homayoun, Mohammad A. Makhzan and Alex Veidenbaum.

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (TVLSI). (Under Review)

2008

(19) *"Dynamic Register File Resizing and Frequency Scaling to Improve Embedded Processor Performance and Energy-Delay Efficiency"*.
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum.
ACM/IEEE 45TH Design Automation Conference, *DAC 2008*. Anaheim, U.S.A.

(18) *"Multiple Sleep Mode Leakage Control for Cache Peripheral Circuits in Embedded Processors"*.
Houman Homayoun, Mohammad Makhzan and Alex Veidenbaum.
In Proceedings of the 2008 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2008*. Atlanta, U.S.A.

(17) *"Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits"*.
Houman Homayoun, Alex Veidenbaum and Jean-Luc Gaudiot.
In Proceedings of XXVI IEEE International Conference on Computer Design, *ICCD 2008*. Lake Tahoe, U.S.A.

(16) *"Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-Of-Order Embedded Processors"*.
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum.
ACM SIGPLAN/SIGBED 2008 Conference on Languages, Compilers, and Tools for Embedded Systems, *LCTES 2008*.

(15) *"ZZ-HVS: Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits"*.
Houman Homayoun, Mohammad Makhzan and Alex Veidenbaum.
In Proceedings of XXVI IEEE International Conference on Computer Design, *ICCD 2008*. Lake Tahoe, U.S.A.

(14) *"A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation"*.
Houman Homayoun, Mohammad Makhzan, Jean-Luc Gaudiot, and Alex Veidenbaum.
International Symposium on Systems, Systems, Architectures, Modeling and Simulation. *SAMOS VIII 2008*, Samos, Greece.

2007

(13) *"Reducing Leakage Power in Peripheral Circuit of L2 Caches"*.
Houman Homayoun and Alexander V. Veidenbaum.
In Proceedings of IEEE International Conference on Computer Design, *ICCD 2007*. Lake Tahoe, U.S.A.

2006

(12) "*Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation"*.
Houman Homayoun and Amirali Baniasadi.
The 2nd workshop on unique chips and systems, in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software, *IEEE-ISPASS 2006*, Austin, U.S.A.

(11) "*Reducing Execution Unit Leakage Power in Embedded Processors*".
Houman Homayoun and Amirali Baniasadi.
The 6th International Conference on Embedded Computer Systems, *SAMOS VI-2006*. Samos, Greece.

(10) "*Reducing the Instruction Queue Leakage Power in Superscalar Processor*".
Houman Homayoun and Ted H. Szymanski.
The 19th Annual Canadian Conference on Electrical and Computer Engineering, *CCECE-2006*, Ottawa, Canada.

2005

(9) "*Analysis of Functional Unit Power Gating in Embedded Processors*".
Houman Homayoun and Amirali Baniasadi.

IFIP International Conference on Very Large Scale Integration System on Chip *IFIP VLSI-SOC 2005*. Perth, Wetsren Australia.

(8) "*Thread Scheduling Based on Low Quality Instruction Prediction for Simultaneous Multithreaded Processors*".
Houman Homayoun, Kin F. Li and Setareh Rafatirad.
The 3rd International IEEE NorthEast Workshop on Circuits and Systems, *IEEE-NEWCAS 2005*. Montreal, Canada.

(7) "*Functional Unit Power Gating in Simultaneous Multithreaded Processors*".
Houman Homayoun, Kin F. Li. and Setareh Rafatirad.
The IEEE Pacific Rim Conference on Communications, Computers and Signal Processing *IEEE-PACRIM 2005*. Victoria, Canada.

(6) *"Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation"*.
Houman Homayoun
Master of Applied Science Thesis, Electrical Engineering and Computer Science Department, University of Victoria, Canada, 2005.

2004 and Prior

(5) "*SimpleScalar Comprehensive Tutorial*".
Houman Homayoun and Amirali Baniasadi.
University of Victoria, Technical Report, September 2004.

(4) "*Akai Telephone Design, Practical StateCharts in C/C++*".
Houman Homayoun.
Senior Project Design, Technical Report, University of Victoria, *April 2004*.

(3) "*Survey on Instruction Issue Queue Design*".
Houman Homayoun.
University of Victoria, Technical Report, *December 2003*.

(2) "*Livermore Kernel Parallelization Using OpenMP*".
Houman Homayoun.
University Of Victoria, Technical Report , *December 2003***.**

(1) "*Computer Network Security and Hacking*".
Houman Homayoun, A.H.Ahmadi Motlagh, Pouya.S.Shobeiri.
Sanaee Publishing Company, Tehran, IRAN, *2003*.

EDUCATION

§ PhD
School of Information and Computer Science, Center for Embedded Computer Systems, University of California Irvine, September 2006-Present, Conducting research on power-efficient high performance/Embedded processor design. (GPA: 4.0/4.0).

§ Master of Applied Science
Electrical and Computer Engineering Department, University of Victoria, Canada, September 2003-March 2005, Thesis Title:" Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation", (GPA: 8.67/9).

§ Bachelor of Science
Electrical and Computer Engineering Department, Sharif University of Technology, Tehran, Iran, October 1998-May 2003,(GPA: 15/20).

TECHNICAL SKILLS

§ **Computer Programming Language**, C/C++: STL, OpenMp and POSIX, PHP, Pascal, MATLAB.

§ **ASIC Design Tool,** Back-end and front-end tools: Cadence Nano-Encounter and RTL Compiler, Synopsys IC and DC Compiler**.**

§ **Computer Hardware/Simulator Description Programming**, Verilog, VHDL, SimpleScalar, Hyper Threading Processor Simulator, System C, Assembly Language: Intel 8051(µc), Intel 80x86, HSPICE.

§ **Operating Systems**, Linux, VMS, UNIX, Windows.

§ **Others**, UML, StateCharts, MYSQL, HTML, LabVIEW.

§ **Equipment,** Oscilloscope, Function Generator, Spectrum Analyzer, Impedance Analyzer, Frequency Counter and Digital Multimeter.

PROVISIONAL PATENT

(P1) "No Instruction Set - No Pipeline BIST Microcontroller (NISP-BIST) for Testing Embedded SRAMs"
Houman Homayoun and Gil Winograd, Novelics Corporation, August 2008.

HONORS/AWARDS/RESEARCH GRANTS

§ "**Chair Fellowship***"*, University of California Irvine, *September 2006-September 2010.*

§ "**First Place**", IEEE Orange County and Western Digital Student Design Contest, 8th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California, Nov 2009.

§ "**First Place**", IEEE Orange County and Western Digital Student Design Contest, 7th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California, Nov 2008.

§ "**University Scholarship***"*, McMaster University, Canada, *September 2005-August 2006.*

§ "**NAHAAL Scholarship***"* for Excellence in Education and Research, *September 2001-August 2002*.

§ "**National Ranking***"*, Rank 55 among more than 500,000 participants in Iran Nationwide Universities Entrance Exam-*1998*.

EDUCATIONAL/ACADEMIC ACTIVITY

§ **Teaching Assistant**, Logic Design Lab, University of California Irvine, Computer Science Department, *January-March 2010.*

§ **Teaching Assistant**, Senior Design Project, University of California Irvine, Computer Science Department, *September-December 2009.*

§ **Teaching Assistant,** Introduction to Computer Design, University of California Irvine, Computer Science Department, *September-December 2007*.

§ **Laboratory and Tutorial Instructor**, Advanced Internet Communications, Electrical and Computer Engineering Department, McMaster University, *January 2006-March 2006*.

§ **Laboratory instructor**, General Physics, Physics Department, University of Victoria, *September 2004-December 2004*.

§ **Laboratory and Tutorial instructor**, Linear Circuit I, Electrical and Computer Engineering Department, University of Victoria, *May 2004-August 2004.*

§ **Laboratory instructor**, Electronic Circuit I, Electrical and Computer Engineering Department, University of Victoria, *January 2004-April 2004.*

§ **Laboratory instructor**, Microprocessor Systems, Electrical and Computer Engineering Department, University of Victoria, *September 2003-December 2003.*

§ **Tutorial instructor**, Digital Circuit Design, Electrical and Computer Engineering Department, Sharif University of Technology, *March 2002-July 2002.*

CONFERENCE COMMITTEE MEMBER/REVIEWER

§ **Reviewer** of The 23rd International Conference on Supercomputing (*ICS*) 2009.

§ **Reviewer** of International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, (*CASES*) 2009.

§ **Reviewer** of The 35th International Symposium on Computer Architecture, (*ISCA*) *2008.*

§ **Reviewer** of The XXVI IEEE International Conference on Computer Design, (*ICCD*) *2008*.

§ **Reviewer** of The IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems, (*TCAD*).

§ **Reviewer** of The ACM International Conference on Computing Frontiers, (*CF*) *2008.*

§ **Reviewer** of The IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (*TVLSI*).

§ **Reviewer** of The 20th International Symposium on Computer Architecture and High Performance Computing, (*SBAC-PAD*) *2007.*

§ **Reviewer** of International Symposium on Low Power Electronics and Design (*ISLPED*) 2009.

§ **Technical Program Committee member**, International Millennium Seminar on Electrical Engineering IMSEE'2000, Electrical Engineering Department, Sharif University of Technology, *1-3 March 2000*.

§ **Technical Program Committee member**, The First Educational Seminar and Specialized Course for Simulink, Electrical Engineering Department, Sharif University of Technology, *23-24 October 2000*.

GRADUATE LEVEL COURSE

Advanced Computer Architecture
Introduction to Parallel and Cluster Computing
Advanced Microprocessor Design
Digital VLSI Systems
Fundamentals of the Design and Analysis of Algorithms
Low Power Design Techniques
Matrix Computations for Signal Processing
Analog Filter Design
Advanced Digital Circuit Design
Design of Analog CMOS Circuit

REFERENCE

Prof. Alex Veidenbaum, University of California Irvine, U.S.A. (PhD Advisor)
Prof. Jean-Luc Gaudiot, University of California Irvine, U.S.A. (PhD Co-Advisor)
Prof. Fadi Kurdahi, University of California Irvine, U.S.A. (PhD Co-Advisor)
Prof. Nikil Dutt, University of California Irvine, U.S.A.
Prof. Elaheh Bozorgzadeh, University of California Irvine, U.S.A.
Prof. Kin F. Li, University of Victoria, Canada.
Prof. Nikitas Dimopolous, University of Victoria, Canada.
Prof. Sudeep Pasricha, Colorado State University, U.S.A.