DAC June 3-7, 2012

Tutorial 3: System-Level Exploration of Power, Temperature, Performance and Area for Multicore Architectures

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Abstract

With the proliferation of multicore architectures, system designers critically need simulation tools to perform early design space exploration of different architectural configurations. Designers typically need to evaluate the effect of different applications on power, performance, temperature, area and reliability of multicore architectures.

While architectural simulators such as Simplescalar integrated with HotSpot and Wattch have been used in the past to perform design space evaluation, several factors drive the need for new tools to address both changes in technology as well as the proliferation of multicore processor architectures. Many new simulation frameworks are emerging that attempt to accurately model power, temperature, area, and timing characteristics. These tools allow accurate modeling the effects of deep-submicron technologies, as well as all accurately model the various subcomponents of these complex multicore platforms.

This tutorial first briefly reviews the state of the art in simulators and modeling tools including; SMTSIM, GEM5, SESC as representative cycle accurate processor core performance simulators; DARSIM for cache interconnection network modeling and evaluation; HotSpot for thermal estimation; and CACTI and NVSIM for power and area modeling of various SRAM and NVM memory technologies and McPAT (Multicore Power, Area, and Timing) to model power, area, and timing of multicore architectures. The tutorial then presents example frameworks and workflows integrating these tools to allow the accurate modeling of various parameters of interest for state of the art multicore architectures.

Houman Homayoun is currently a 2010 National Science Foundation Computing Innovation Postdoctoral Fellow working at the University of California, San Diego. His research is on power-temperature and reliability-aware memory and processor design optimizations, where he has published more than 30 technical papers on the subject, including some of the earliest work in the field to address the importance of cross-layer power and temperature optimization in memory peripheral circuits. Houman was a recipient of the four-year UC-Irvine Computer Science Department chair fellowship. He received his PhD degree from the Department of Computer Science at the University of California, Irvine in 2010. He has served as a Technical Program Committee member for a number of international conferences including ISLPED, ISQED and CF. He is a member of the IEEE and the ACM.

Manish Arora is currently working towards his PhD in the Department of Computer Science and Engineering at University of California, San Diego. Manish has a MS in computer engineering from University of Texas at Austin (2010) and a Bachelor in ECE from Indian Institute of Technology Kharagpur (2000). Manish previously worked in the industry from 2000-2008 including at Samsung Electronics Global R&D, Korea from 2002-2008 where he was a senior multimedia signal-processing researcher/manager. Manish has 14 publications and 15 patents/invention disclosures in the area of efficient implementation techniques and DSP algorithms. His current research interests include low power computer architecture for irregular computations, heterogeneous architectures, GPU architectures and parallel systems.