Houman Homayoun

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PERSONAL

ü **Residency Status** Canadian Permanent Resident ü **Marital Status** Married

OBJECTIVE

§ **Objective**, To find a challenging position that enables me to utilize my skills for solving state of the art problems, and provides opportunities for advancement.
§ **Availability** ASAP.

QUALIFICATIONS

§ Expertise and hands-on experience in low power design, memory design and hardware verification.
§ Skillful in ASIC design.
§ Experienced in designing low power micro-architectural techniques for high performance and embedded processors.
§ Strong background in designing fault tolerant memory (SRAM) and Cache architectures for process variation tolerance.
§ Expertise in designing parametrizable BIST microcontroller for embedded memories.
§ Expertise in System modeling.
§ 7+ years of professional work experience in development and research environment.
§ 4+ years of lecturing and teaching experience, mentoring and presentation skills.

EDUCATION

§ **PhD** *September 2006-May 2010 (expected), (GPA: 4.0/4.0)*
School of Information and Computer Science, Center for Embedded Computer Systems, University of California Irvine.
Thesis: Cooperative Architectural and Circuit Techniques for Leakage-Temperature and Reliability Aware SRAM Cache Design.

§ **Master of Applied Science** *September 2003-March 2005, (GPA: 8.67/9)*
Electrical and Computer Engineering Department, University of Victoria, Canada.
Thesis: Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation.

§ **Bachelor of Science** *October 1998-May 2003,(GPA: 15/20)*
Electrical and Computer Engineering Department, Sharif University of Technology.

TECHNICAL SKILLS

§ **Computer Programming Language**, C/C++: STL, OpenMp, Perl, PHP, Pascal, MATLAB.
§ **ASIC Design Tool,** Back-end and front-end tools: Cadence Nano-Encounter and RTL Compiler, Synopsys IC and DC Compiler**.**
§ **Computer Hardware/Simulator Description Programming**, Verilog, VHDL, SimpleScalar, Hyper Threading Processor Simulator, System C, Assembly Language: Intel 8051(µc), Intel 80x86, HSPICE.
§ **Operating Systems**, Linux, VMS, UNIX, Windows.
§ **Others**, UML, StateCharts, MYSQL, HTML, LabVIEW.
§ **Equipment,** Oscilloscope, Function Generator, Spectrum Analyzer, Impedance Analyzer, Frequency Counter and Digital Multimeter.

RELEVANT EXPERIENCE

§ **Graduate Researcher**, Center for Embedded Computer Systems, University of California Irvine, *September 2006-Present*

Ø Conducting research in low power, low temperature and reliability aware multi-core and memory subsystem design.
Ø Developed new circuit technique referred as multi sleep mode zig-zag horizontal and vertical sleep transistor sharing to reduce leakage power in SRAM peripheral circuitry. Implemented the circuit technique in L1 and L2 Caches, Register file, Branch Predictor, Reorder Buffer and ITLB/DTLB of high performance (Core ™2 Duo) and embedded (ARM 11) processors. Developed micro-architectural approaches to control the new circuit to reduce power while maintaining performance. Developed a cycle accurate performance model based on Simplescalar and M5 micro-architecture simulator for performance and power measurements when running SPEC2K Benchmarks.
Ø Developed a novel algorithm referred as access concentration and activity redistribution for reducing temperature in processor Hotspots including Register file and L1 Cache. Implemented the algorithm in MIPS-74K embedded processor register file. Used Standard Benchmarks (SPEC2K and MiBench) for evaluation.
Ø Developed novel techniques for clock tree synthesis to reduce leakage power in the clock tree network. Implemented the algorithm in an industry standard back-end tool (synopsis ASTRO).
Ø Developed a new architectural approach to adapt Register File, Instruction Queue, Reorder Buffer, Load and Store Queue size in accordance with program behavior to reduce their power dissipation. Developed circuit assist to enable resource adaptation in these processor units.
Ø Designed fault tolerant Cache architectures for process variation tolerance.
Ø Publishing more than 25 referred papers in top journals and conferences in the field.

§ **Design Architect,** NOVELICS, Aliso Viejo, California *January 2007-October 2008*

Ø Principal Designer of a parametrizable BIST microcontroller for testing different memories.
Ø Frond-end and back-end design including Synthesizing, floor planning, power planning and place and routing in TSMC 90nm and IBM 65nm std cell libraries using Cadence Nano-Encounter, RTL Compiler and Synopsys DC Compiler and Astro.
Ø Automating the entire design flow using Perl.
Ø Automating the design verification flow.

- Successfull post-fabrication testing.
- Contributing in design and verification of different embedded memories such as DRAMs and SRAMs.

§ **Design/Firmware Engineer,** Pishgam Tousee Niroo Co., Tehran *May 2005-September 2005*
- Designed the controller part of a commercial display monitor using Motorola Microcontroller 68000.

§ **Researcher**, Computer Engineering Department, McMaster University, Canada *October 2005-April 2006*
- Collaborated in designing a low power 5.12 Terabit capacity single-chip optoelectronic VLSI crossbar switch.

§ **Graduate Researcher,** Computer Engineering Department, University of Victoria, Canada *September 2003-March 2005*
- Developed cycle accurate simulator to model different variety of embedded processor.
- Developed microarchitectural techniques to increase performance and reduce power dissipation in Intel XScale processor functional units.
- Publishing 6 referred conference papers.

§ **Researcher**, Electronic Research Center, Sharif University of Technology, Tehran, Iran *October 2002-June 2003*
- Collaborated in designing a data acquisition system with appliance of a 16 bit Intel 196 family microcontroller as controller/supervisor and a 32 bit 6711 TI series DSP as a processor unit.

§ **Service Technician,** Internship Position, Sinatech Co.Ltd, Iran, Tehran *November 2001-April 2002*
- Troubleshooting medical and research laboratory appliances such as Gas Chromatography Systems, Atomic Absorption spectrophotometry Instruments, Flash Point Tester Equipments and Cell Counter Instruments.

HONORS/AWARDS/RESEARCH GRANTS

§ "**4-Years Chair Fellowship Award**", University of California Irvine, Computer Science Dept. *September 2006-September 2010*

§ "**First Place**", IEEE Orange County and Western Digital Student Design Contest. *Nov 2009*
8th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.

§ "**First Place**", IEEE Orange County and Western Digital Student Design Contest. *Nov 2008*
7th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.

§ **"DAC Student Award Mentor**", Design Automation Conference (DAC), *June 2008*

§ "**University Scholarship***"*, McMaster University, Canada. *September 2005-August 2006*

§ "**NAHAAL Scholarship***"* for Excellence in Education and Research. *September 2001-August 2002*

§ "**National Ranking***"*, Rank 55 among more than 500,000 participants. *September 1998*
Iran Nationwide Universities Entrance Exam.

SELECTED PUBLICATION

§ *"A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation"*. *(TVLSI)*
Houman Homayoun, Avesta Sasan, Alex Veidenbaum, Jean-Luc Gaudiot.

§ *"MZZ-HVS: Multi Modes Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits"*. *(TVLSI)*
Houman Homayoun, Avesta Sasan and Alex Veidenbaum.

§ *"RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor*".
Houman Homayoun, Aseem Gupta, Alex Veidenbaum, Fadi J. Kurdahi, Nikil Dutt. (*HiPEAC 2010*)

§ *"Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks*".
Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Fadi Kurdahi, Alex Veidenbaum. *(ISQED-2010)*

§ *"Exploiting Power Budgeting in Thermal-Aware Dynamic Placement for Reconfigurable Systems"* *(ISLPED-2010)*
Shahin Golshan, Kazutoshi Wakabayashi, Benjamin Carrión Schäfer, **Houman Homayoun**, Elaheh Bozorgzadeh.

§ "*Process Variation Aware Cache for Aggressive Voltage-Frequency Scaling*".
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi. (*DATE-2009)*

§ *"Dynamic Register File Resizing and Frequency Scaling to Improve Embedded Processor Performance and Energy-Delay Efficiency"*.
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum. (*DAC-2008)*

§ *"Multiple Sleep Mode Leakage Control for Cache Peripheral Circuits in Embedded Processors"*.
Houman Homayoun, Mohammad Makhzan and Alex Veidenbaum. (*CASES-2008)*

§ *"Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits"*.
Houman Homayoun, Alex Veidenbaum and Jean-Luc Gaudiot (*ICCD-2008)*

PROVISIONAL PATENT

§ *"No Instruction Set - No Pipeline BIST Microcontroller (NISP-BIST) for Testing Embedded SRAMs"* *August 2008*
Houman Homayoun and Gil Winograd, Novelics Corporation.

GRADUATE LEVEL COURSE

- Advanced Computer Architecture
- Introduction to Parallel and Cluster Computing
- Advanced Microprocessor Design
- Digital VLSI Systems
- Fundamentals of the Design and Analysis of Algorithms
- Low Power Design Techniques
- Matrix Computations for Signal Processing
- Analog Filter Design
- Advanced Digital Circuit Design
- Design of Analog CMOS Circuit