

# Houman Homayoun

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## PERSONAL

|                                  |                                   |                         |                          |
|----------------------------------|-----------------------------------|-------------------------|--------------------------|
| Ü <b>Date and Place of Birth</b> | Iran, Tehran, August, 10, 1980    | Ü <b>Marital Status</b> | Married                  |
| Ü <b>Citizenship</b>             | Iran, Canadian Permanent Resident | Ü <b>Language</b>       | English, Persian (Farsi) |

## PROFILE

### § Objective

To find a challenging position with a company that enables me to utilize my skills for solving state of the art problems, and provides opportunities for advancement.

### § Availability

ASAP for full time position.

## EDUCATION

### § PhD

September 2006-May 2010 (expected), (GPA: 4.0/4.0)

School of Information and Computer Science, Center for Embedded Computer Systems, University of California Irvine.

Thesis: Leakage-Temperature and Reliability Aware SRAM Cache Design.

### § Master of Applied Science

September 2003-March 2005, (GPA: 8.67/9)

Electrical and Computer Engineering Department, University of Victoria, Canada.

Thesis: Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation.

### § Bachelor of Science

October 1998-May 2003, (GPA: 15/20)

Electrical and Computer Engineering Department, Sharif University of Technology, Tehran, Iran.

## RELEVANT EXPERIENCE

### § Research Assistant

September 2006-Present

Center for Embedded Computer Systems, University of California Irvine, Conducting research in embedded system design, chip multiprocessor design, computer architecture, and VLSI CAD with specific focus on low power design architecture, circuit for low power design, thermal-aware design, reliability-aware memory design, and performance evaluation and improvement.

### § Design Architect

January 2007-October 2008

NOVELICS, Aliso Viejo, California, Principal Designer of a parametrizable BIST microcontroller for testing different memories. Synthesizing, floor planning, power planning and place and routing in TSMC 90nm and IBM 65nm std cell libraries using Cadence Nano-Encounter, RTL Compiler and Synopsys DC Compiler and Astro. Automating the entire design flow using Perl. Successfully post-fabrication testing. Cooperating in design and verification of different embedded memories such as DRAMs and SRAMs.

### § Design/Firmware Engineer

May 2005-September 2005

Pishgam Tousee Niroo Co., Tehran, Iran, Designed the controller part of a commercial display monitor using Motorola Microcontroller 68000.

### Research Assistant

October 2005-April 2006

Computer Engineering Department, McMaster University, Canada, Collaborated in designing a low power 5.12 Terabit capacity single-chip optoelectronic VLSI crossbar switch.

### § Research Assistant

September 2003-March 2005

Computer Engineering Department, University of Victoria, Canada, Developed software to simulate different variety of microprocessors and embedded systems. Developing microarchitectural techniques to increase performance and reduce power dissipation in Intel XScale processor.

### § Research Engineer

October 2002-June 2003

Electronic Research Center, Sharif University of Technology, Tehran, Iran, Collaborated in designing a data acquisition system with appliance of a 16 bit Intel 196 family microcontroller as controller/supervisor and a 32 bit 6711 TI series DSP as a processor unit.

### § Service Technician

November 2001-April 2002

Internship Position, Sinatch Co.Ltd Repair Section, Tehran, Iran, Troubleshooting medical and research laboratory appliances such as Gas Chromatography Systems, Atomic Absorption spectrophotometry Instruments, Flash Point Tester Equipments and Cell Counter Instruments.

### § Software Developer

April 2001-July 2001

Internship Position, Mahab Ghods Company, Tehran, Iran, Implementation and design of HMI for management information system server and client application. Adding database modules and web server to management information system.

## HONORS/AWARDS/RESEARCH GRANTS

§ **“Chair Fellowship”**, University of California Irvine, Computer Science Department.

September 2006-September 2010

§ **“First Place”**, IEEE Orange County and Western Digital Student Design Contest.

Nov 2009

8th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.

§ **“First Place”**, IEEE Orange County and Western Digital Student Design Contest.

Nov 2008

7th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.

§ **“DAC Student Mentor”** Award, Design Automation Conference (DAC),

June 2008

§ “**University Scholarship**”, McMaster University, Canada.  
 § “**NAHAAL Scholarship**” for Excellence in Education and Research.  
 § “**National Ranking**”, Rank 55 among more than 500,000 participants.  
 Iran Nationwide Universities Entrance Exam.

September 2005-August 2006  
September 2001-August 2002  
September 1998

## SELECTED PUBLICATION

- ü “*Multiple Sleep Modes Leakage Control in Peripheral Circuits of a All Major SRAM-Based Processor Units*”.  
**Houman Homayoun**, Avesta Sasan, Aseem Gupta, Alex Veidenbaum, Fadi Kurdahi, Nikil Dutt (CF-2010)
- ü “*RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor*”.  
**Houman Homayoun**, Aseem Gupta, Alex Veidenbaum, Fadi J. Kurdahi, Nikil Dutt. (HiPEAC 2010)
- ü “*Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks*”.  
**Houman Homayoun**, Shahin Golshan, Eli Bozorgzadeh, Fadi Kurdahi, Alex Veidenbaum. (ISQED-2010)
- ü “*Process Variation Aware Cache for Aggressive Voltage-Frequency Scaling*”.  
 Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi. (DATE-2009)
- ü “*Fault Tolerant Cache Architecture for Sub 500mv Operation*”.  
 Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi. (CASES-2009)
- ü “*Dynamic Register File Resizing and Frequency Scaling to Improve Embedded Processor Performance and Energy-Delay Efficiency*”.  
**Houman Homayoun**, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum. (DAC-2008)
- ü “*Multiple Sleep Mode Leakage Control for Cache Peripheral Circuits in Embedded Processors*”.  
**Houman Homayoun**, Mohammad Makhzan and Alex Veidenbaum. (CASES-2008)
- ü “*Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-Of-Order Embedded Processors*”.  
**Houman Homayoun**, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum. (LCTES-2008)
- ü “*ZZ-HVS: Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits*”.  
**Houman Homayoun**, Mohammad Makhzan and Alex Veidenbaum. (ICCD-2008)
- ü “*Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits*”.  
**Houman Homayoun**, Alex Veidenbaum and Jean-Luc Gaudiot (ICCD-2008)
- ü “*A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation*”.  
**Houman Homayoun**, Mohammad Makhzan, Jean-Luc Gaudiot, and Alex Veidenbaum. (SAMOS-2008)
- ü “*Reducing Leakage Power in Peripheral Circuit of L2 Caches*”.  
**Houman Homayoun** and Alexander V. Veidenbaum. (ICCD-2007)

## TECHNICAL SKILLS

§ **Computer Programming Language**, C/C++: STL, OpenMp, Perl, PHP, Pascal, MATLAB.  
 § **ASIC Design Tool**, Back-end and front-end tools: Cadence Nano-Encounter and RTL Compiler, Synopsys IC and DC Compiler.  
 § **Computer Hardware/Simulator Description Programming**, Verilog, VHDL, SimpleScalar, Hyper Threading Processor Simulator, System C, Assembly Language: Intel 8051(µc), Intel 80x86, HSPICE.  
 § **Operating Systems**, Linux, VMS, UNIX, Windows.  
 § **Others**, UML, StateCharts, MYSQL, HTML, LabVIEW.  
 § **Equipment**, Oscilloscope, Function Generator, Spectrum Analyzer, Impedance Analyzer, Frequency Counter and Digital Multimeter.

## PROVISIONAL PATENT

§ “*No Instruction Set - No Pipeline BIST Microcontroller (NISP-BIST) for Testing Embedded SRAMs*” August 2008  
**Houman Homayoun** and Gil Winograd, Novelics Corporation.

## GRADUATE LEVEL COURSE

- |   |  |
|---|--|
| <ul style="list-style-type: none"> <li>ü Advanced Computer Architecture</li> <li>ü Introduction to Parallel and Cluster Computing</li> <li>ü Advanced Microprocessor Design</li> <li>ü Digital VLSI Systems</li> <li>ü Fundamentals of the Design and Analysis of Algorithms</li> </ul> | <ul style="list-style-type: none"> <li>ü Low Power Design Techniques</li> <li>ü Matrix Computations for Signal Processing</li> <li>ü Analog Filter Design</li> <li>ü Advanced Digital Circuit Design</li> <li>ü Design of Analog CMOS Circuit</li> </ul> |
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## REFERENCE

Prof. Alex Veidenbaum, University of California Irvine, U.S.A. (PhD Advisor)  
 Prof. Jean-Luc Gaudiot, University of California Irvine, U.S.A. (PhD Co-Advisor)  
 Prof. Fadi Kurdahi, University of California Irvine, U.S.A. (PhD Co-Advisor)  
 Prof. Nikil Dutt, University of California Irvine, U.S.A.  
 Prof. Elaheh Bozorgzadeh, University of California Irvine, U.S.A.