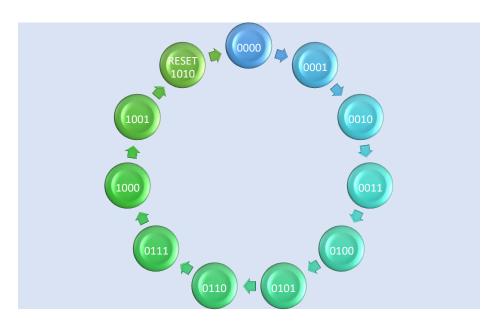
### LABORATORIO LOGICA SECUENCIAL

### PROBLEMA 1

Diseñe un Contador del 0 al 9. Usar el FF JK

### Incluya:

- Tabla de Verdad y de Excitación.
- Diagramas de Estados.
- Diagramas Lógicos.
- Simulación (LiveWire, Multisim)



	E	STADO I	RESENT	E	X		ESTADO	FUTURO									
	A	В	С	D		A	В	C	D	JA	KA	JB	KB	JC	KC	JD	KD
0	0	0	0	0	0	0	0	0	0	0	X	0	X	0	X	0	X
0	0	0	0	0	1	0	0	0	1	0	X	0	X	0	X	1	X
	0	0	0	1	0	0	0	0	1	0	X	0	X	0	X	X	0
	0	0	0	1	1	0	0	1	0	0	X	0	X	1	X	X	1
2	0	0	1	0	0	0	0	1	0	0	X	0	X	X	0	0	X
2	0	0	1	0	1	0	0	1	1	0	X	0	X	X	0	1	X
3	0	0	- 1	1	0	0	0	1	1	0	X	0	X	X	0	X	0
3	0	0	- 1	1	1	0	1	0	0	0	X	1	X	X	1	X	1
4	0	1	0	0	0	0	1	0	0	0	X	X	0	0	X	0	X
	0	1	0	0	1	0	1	0	1	0	X	X	0	0	X	1	X
5	0	1	0	1	0	0	1	0	1	0	X	X	0	0	X	X	0
-	0	1	0	1	1	0	1	1	0	0	X	X	0	1	X	X	1
6	0	1	- 1	0	0	0	1	1	0	0	X	X	0	X	0	0	X
0	0	1	1	0	1	0	1	1	1	0	X	X	0	X	0	1	X
7	0	1	- 1	1	0	0	1	1	1	0	X	X	0	X	0	X	0
	0	1	- 1	1	1	- 1	0	0	0	1	X	X	1	X	1	X	1
8	1	0	0	0	0	- 1	0	0	0	X	0	0	X	0	X	0	X
8	1	0	0	0	1	- 1	0	0	1	X	0	0	X	0	X	1	X
9	1	0	0	1	0	1	0	0	1	X	0	0	X	0	X	X	0
,	1	0	0	1	1	- 1	0	1	0	X	0	0	X	1	X	X	1
RESETEO	1	0	1	0	0	- 1	0	1	0	X	0	0	X	X	0	0	X
KLSETEO	1	0	1	0	1	0	0	0	0	X	1	0	X	X	1	0	X

Misma tabla pero por partes para que se entienda:

**Entradas:** 

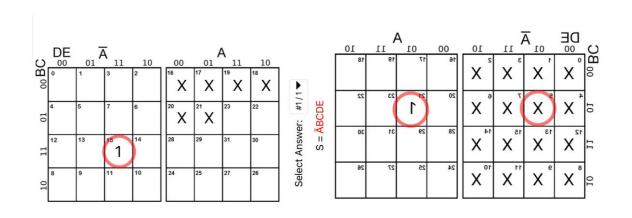
	E	STADO F	RESENT	E	X		ESTADO	FUTURO		
	A	В	C	D		A	В	C	D	
0	0	0	0	0	0	0	0	0	0	
U	0	0	0	0	1	0	0	0	1	
1	0	0	0	1	0	0	0	0	1	
1	0	0	0	1	1	0	0	1	0	
2	0	0	1	0	0	0	0	1	0	
2	0	0	1	0	1	0	0	1	1	
3	0	0	1	1	0	0	0	1	1	
3	0	0	1	1	1	0	1	0	0	
4	0	1	0	0	0	0	1	0	0	
4	0	1	0	0	1	0	1	0	1	
5	0	1	0	1	0	0	1	0	1	
3	0	1	0	1	1	0	1	1	0	
6	0	1	1	0	0	0	1	1	0	
· ·	0	1	1	0	1	0	1	1	1	
7	0	1	1	1	0	0	1	1	1	
/	0	1	1	1	1	1	0	0	0	
8	1	0	0	0	0	1	0	0	0	
0	1	0	0	0	1	1	0	0	1	
9	1	0	0	1	0	1	0	0	1	
9	1	0	0	1	1	1	0	1	0	
RESETEO	1	0	1	0	0	1	0	1	0	
KESETEO	1	0	1	0	1	0	0	0	0	

# Salidas del flip flop

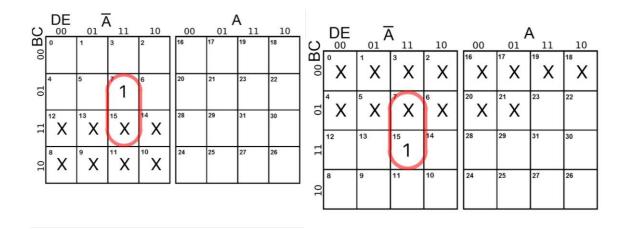
			Salidas				
JA	KA	JB	KB	JC	KC	JD	KD
0	X	0	X	0	X	0	X
0	X	0	X	0	X	1	X
0	X	0	X	0	X	X	0
0	X	0	X	1	X	X	1
0	X	0	X	X	0	0	X
0	X	0	X	X	0	1	X
0	X	0	X	X	0	X	0
0	X	1	X	X	1	X	1
0	X	X	0	0	X	0	X
0	X	X	0	0	X	1	X
0	X	X	0	0	X	X	0
0	X	X	0	1	X	X	1
0	X	X	0	X	0	0	X
0	X	X	0	X	0	1	X
0	X	X	0	X	0	X	0
1	X	X	1	X	1	X	1
X	0	0	X	0	X	0	X
X	0	0	X	0	X	1	X
X	0	0	X	0	X	X	0
X	0	0	X	1	X	X	1
X	0	0	X	X	0	0	X
X	1	0	X	X	1	0	X

## KMaps y ecuaciones:

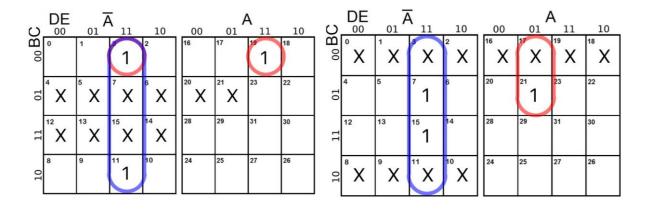
# **Funcion JA y KA**



# **Funcion JB y KB**



# **Funcion JC y KC**

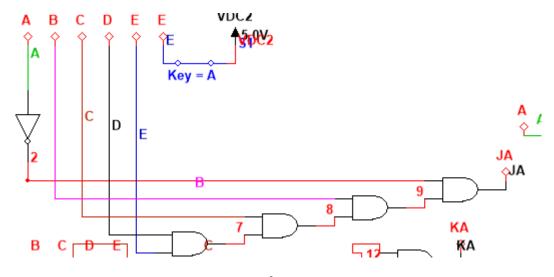


# **Funcion JD y KD**

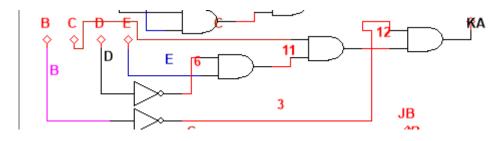
DE	Ā			A	A			DE	Ā	Ā				١	
	01 11	10	00	01	11	10	$_{1}^{\circ}$	00	01	11	10	00	01	11	10
80°	1 <sup>3</sup> X	X	16	1	19 X	18 X	00 E	̈́Χ	Х	1	2	16 X	X	19	18
10	1 7 X	X	20	21	23	22	01	ΔX	ΣX	1	6	<sup>20</sup> X	<sup>21</sup> X	23	22
12 13	1 15 X	14 X	28	29	31	30	11	12 X	13 X	15	14	28	29	31	30
10	1 <sup>11</sup> X	<sup>10</sup> X	24	25	27	26	10	<sup>8</sup> X	°X	"1	10	24	25	27	26

A'BCDX JA B'CD'X KA A'CDX JB A'CDX ΚB B'C'DX + A'DXJC AB'D'X + A'DXKC B'C'X+A'X JD B'C'X+A'X KD

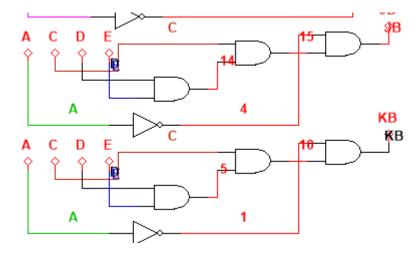
### **Funcion JA**



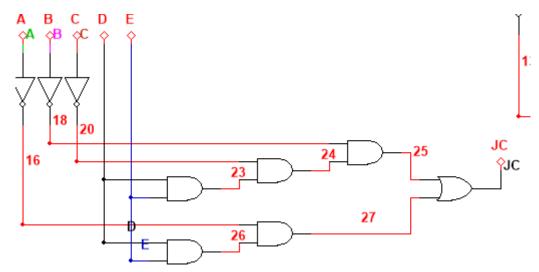
**Funcion KA** 

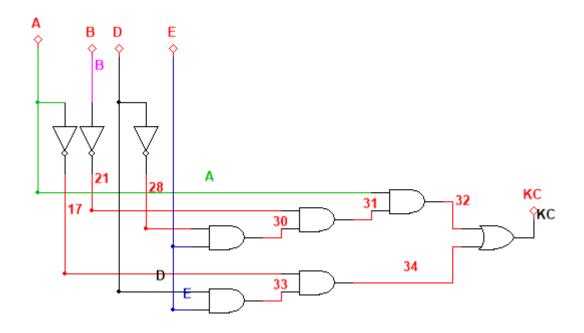


# Funcion JB y KB



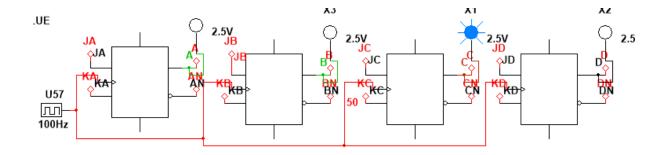
# Funcion JC y KC



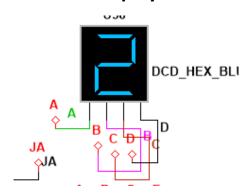


# Funcion JD y KD A B C E A B

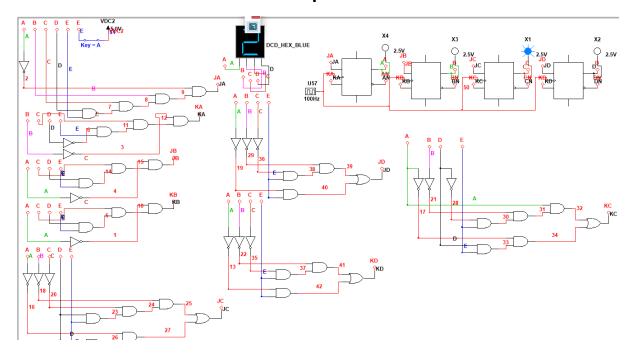
Flip flop



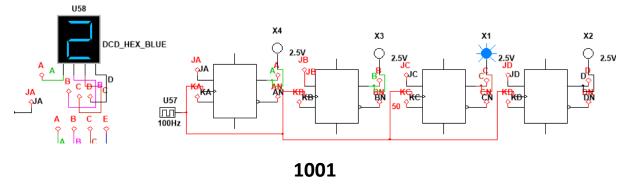
# Display

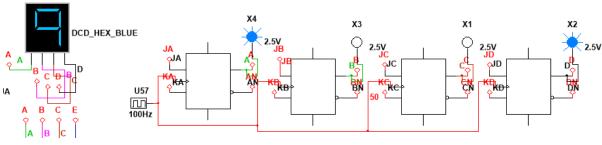


# Completo:

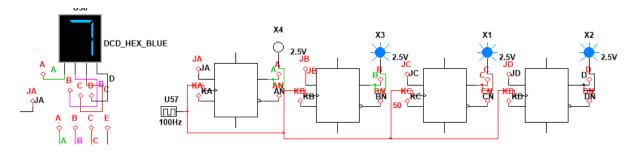


0010





# 0111

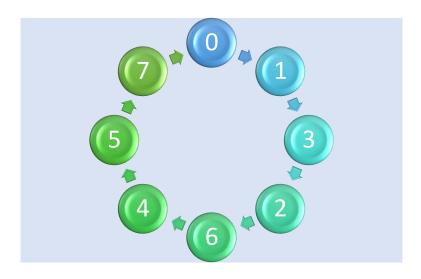


### PROBLEMA 2

Un contador con la siguiente secuencia binaria: 0,1,3,2,6,4,5,7 y que se repita. Use Flip-Flops RS.

### Incluya:

- Tabla de Verdad y de Excitación.
- Diagramas de Estados.
- Diagramas Lógicos.
- Simulación (LiveWire, Multisim)



# Tabla completa:

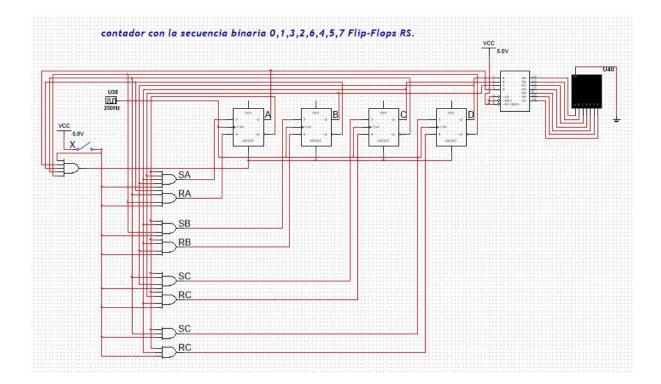
	Е	STADO F	RESENT	Έ	х		ESTADO	FUTURO	)	0         X         0         X         0         X         0           0         X         0         X         0         X         1           0         X         0         X         0         X         X           0         X         0         X         1         0         X           0         X         0         X         X         0         0           0         X         1         0         X         0         0           0         X         0         X         X         0         0         X           0         X         X         0         0         X         0         0         X           0         X         X         0         0         X         1         0         X         0         0         X         1         0         X         0         0         X         X         0         0         X         X         0         0         X         X         0         0         X         X         0         0         X         X         0         0         X         X         0							
	Α	В	С	D		Α	В	С	D	SA	RA	SB	RB	SC	RC	SD	RD
0	0	0	0	0	0	0	0	0	0	0	Х	0	Х	0	Х	0	Χ
U	0	0	0	0	1	0	0	0	1	0	X	0	Х	0	Х	1	0
1	0	0	0	1	0	0	0	0	1	0	X	0	Х	0	Х	X	0
'	0	0	0	1	1	0	0	1	1	0	X	0	X	1	0	X	0
2	0	0	1	0	0	0	0	1	0	0	Х	0	X	X	0	0	X
2	0	0	1	0	1	0	1	1	0	0	X	1	0	X	0	0	X
3	0	0	1	1	0	0	0	1	1	0	X	0	Х	Х	0	X	0
3	0	0	1	1	1	0	0	1	0	0	X	0	X	Х	0	0	1
4	0	1	0	0	0	0	1	0	0	0	X	Х	0	0	Х	0	Х
-	0	1	0	0	1	0	1	0	1	0	X	Х	0	0	X	1	0
5	0	1	0	1	0	0	1	0	1	0	X	Х	0	0	Х	X	0
3	0	1	0	1	1	0	1	1	1	0	X	Х	0	1	0	X	0
6	0	1	1	0	0	0	1	1	0	0	X	Х	0	Х	0	0	X
0	0	1	1	0	1	0	1	0	0	0	X	Х	0	0	1	0	X
7	0	1	1	1	0	0	1	1	1	0	X	Х	0	Х	0	X	0
,	0	1	1	1	1	1	0	0	0	1	0	0	1	0	1	0	1
8	1	0	0	0	0	1	0	0	0	Х	0	0	X	0	Х	0	Χ
O	1	0	0	0	1	0	0	0	0	0	1	0	X	0	Х	0	X

Tabla separada para que se vea bien

	Е	STADO F	RESENT	Έ	х	ESTADO FUTURO  A B C D  0 0 0 0 0  0 0 0 1  0 0 0 1  0 0 1 1  0 0 1 1  0 0 1 1  0 0 1 0  0 1 0  0 1 0  0 1 1  0 0 1 0  0 1 0  0 1 0 0  1 0 0 1  0 1 0 0			)
	Α	В	С	D		Α	В	С	D
0	0	0	0	0	0	0	0	0	0
U	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	0	0	1
	0	0	0	1	1	0	0	1	1
2	0	0	1	0	0	0	0	1	0
۷	0	0	1	0	1	0	1	1	0
3	0	0	1	1	0	0	0	1	1
3	0	0	1	1	1	0	0	1	0
4	0	1	0	0	0	0	1	0	0
4	0	1	0	0	1	0	1	0	1
5	0	1	0	1	0	0	1	0	1
3	0	1	0	1	1	0	1	1	1
6	0	1	1	0	0	0	1	1	0
U	0	1	1	0	1	0	1	0	0
7	0	1	1	1	0	0	1	1	1
/	0	1	1	1	1	1	0	0	0
8	1	0	0	0	0	1	0	0	0
Ö	1	0	0	0	1	0	0	0	0

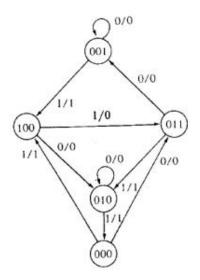
			SAL	IDAS			
SA	RA	SB	RB	SC	RC	SD	RD
0	Χ	0	Χ	0	Χ	0	Χ
0	Χ	0	Χ	0	Χ	1	0
0	Х	0	Χ	0	Χ	Χ	0
0	Χ	0	Χ	1	0	Χ	0
0	Χ	0	Χ	Χ	0	0	Χ
0	Χ	1	0	Χ	0	0	Χ
0	Χ	0	Χ	Χ	0	Χ	0
0	Χ	0	Χ	Χ	0	0	1
0	Χ	Χ	0	0	Χ	0	Χ
0	Χ	Χ	0	0	Χ	1	0
0	Χ	Χ	0	0	Χ	Χ	0
0	Χ	Χ	0	1	0	Χ	0
0	Χ	Χ	0	Χ	0	0	Χ
0	Χ	Χ	0	0	1	0	X
0	Χ	Χ	0	Χ	0	Χ	0
1	0	0	1	0	1	0	1
Χ	0	0	Χ	0	Χ	0	Χ
0	1	0	Χ	0	Χ	0	Χ

	2	ζ				Σ	ζ'				Σ	ζ				<u> </u>	ζ'		
	S.	A				S	A				R	A				R	A		
AB\CD	00	O1	11	10	AB\CD	00	O1	11	10	AB\CD	00	O1	11	10	AB\CD	00	O1	11	10
00					00					00	X	X	X	X	00	X	X	X	X
O1			1		O1					O1	X	X		X	O1	X	X	X	X
11					11					11					11				
10					10	X				10	1				10				
			JA	4 = A	'BCDX								K	A = E	B'C'D'X				
	7	ζ				2	ζ'				2	ζ				2	C'		
	S	В				S	В				R	В				R	В		
AB\CD	00	O1	11	10	AB\CD	00	O1	11	10	AB\CD	00	O1	11	10	AB\CD	00	O1	11	10
00				1	00					00	X	X	X		00	B\CD OO O1 1 OO X X 2 O1			X
O1	X	X		X	O1	X	X	X	X	O1			1		O1				
11					11					11					11				Ш
10					10					10	X				10	X			
			J	B = A	A'CD'X								K	B = A	10 X X X Y X Y RC				
	Σ	ζ				Σ	ζ				Σ	ζ				Σ	C		
	S	С				S	С				R	С				R	С		
AB\CD	00	O1	11	10	AB\CD	00	O1	11	10	AB\CD	00	O1	11	10	AB\CD	_		11	10
00		1	X	X	00			X	Χ	OO	X				00	X	X		
O1		1			O1			X	X	O1	X		1	1	O1	X	X		
11					11					11					11				$oxed{oxed}$
10					10					10	Χ				10	X			
			J	C = A	A'C'DX								K	C = I	A'BCX				
	7	ζ				Σ	C				Σ	ζ				RC 0 00 01 11 X X X X X X X X RD			
	S	D				S	D				R	D				R	D		
AB\CD	OO	O1	11	10	AB\CD	00	O1	11	10	AB\CD	00	O1	11	10	AB\CD	00	O1	11	10
00	1	X			00		X	X		00			1	X	00	X			X
01	1	X			O1		X	X		O1			1	X	O1	X			X
11					11					11	7.				11	77			$\square$
10	L				10					10	X				10	X			
				JD = .	A'C'X								1	KD =	A'CX				



### PROBLEMA 3

Un circuito secuencial tiene una entrada y una salida. El diagrama de estado se muestra abajo. Diseñe un circuito secuencial con FF tipo D.



- Tabla de Verdad y de Excitación.
- Diagramas de Estados.
- Diagramas Lógicos.
- Simulación (LiveWire, Multisim)

	ESTA	DO PRES	ENTE	X	EST	ADO FUT	URO	SALI	DAS	
	A	В	C		A	В	C	DA	DB	DC
0	0	0	0	0	0	1	1	0	1	1
U	0	0	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	1	0	0	1
1	0	0	1	1	1	0	0	1	0	0
2	0	1	0	0	0	1	0	0	1	0
2	0	1	0	1	0	0	0	0	0	0
3	0	1	1	0	0	0	1	0	0	1
3	0	1	1	1	0	1	0	0	1 0 0 0 0 1	0
4	1	0	0	0	0	1	0	0	1	0
4	1	0	0	1	0	1	1	0	1	1

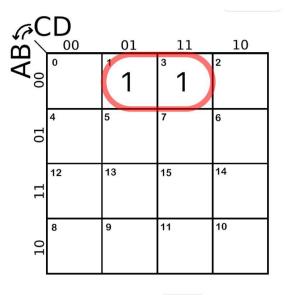
# Tabla separada para que se entienda

	ESTA	DO PRES	ENTE	X	EST	ADO FUT	URO
	A	В	C		A	В	C
0	0	0	0	0	0	1	1
U	0	0	0	1	1	0	0
1	0	0	1	0	0	0	1
1	0	0	1	1	1	0	0
2.	0	1	0	0	0	1	0
2	0	1	0	1	0	0	0
3	0	1	1	0	0	0	1
3	0	1	1	1	0	1	0
4	1	0	0	0	0	1	0
+	1	0	0	1	0	1	1

	SALIDAS	
DA	DB	DC
0	1	1
1	0	0
0	0	1
1	0	0
0	1	0
0	0	0
0	0	1
0	1	0
0	1	0
0	1	1

# **Kmaps y funciones:**

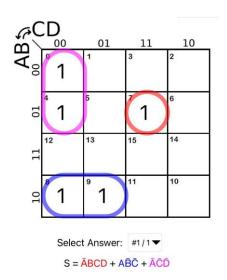
DA



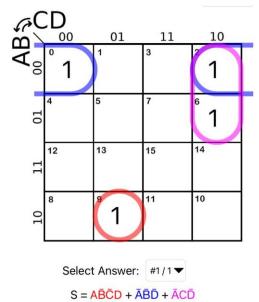
Select Answer: #1/1▼

 $S = \bar{A}\bar{B}D$ 

DB

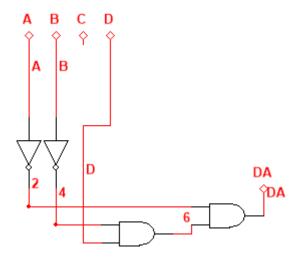


DC

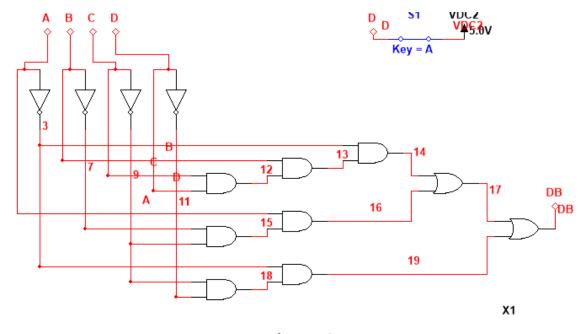


S = ADOD + ADD + ACD

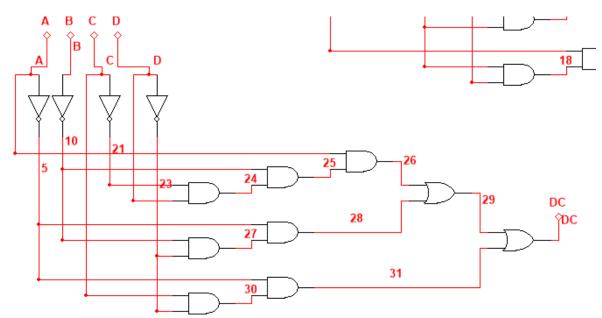
# **Funcion DA**



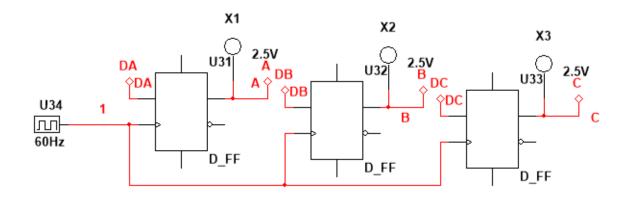
**Funcion DB** 



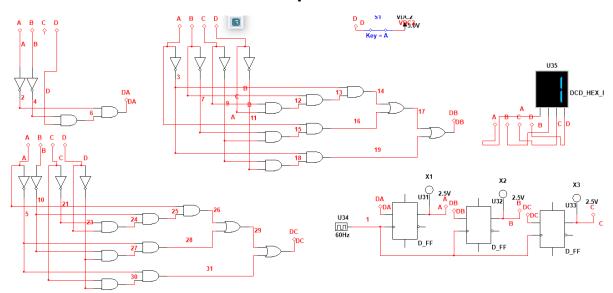
# **Funcion DC**



Flip Flop

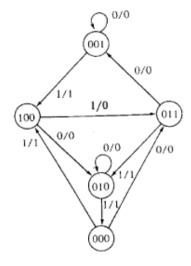


# Completo:



# SISTEMAS DIGITALES LOGICA SECUENCIAL PRACTICA # 1

- 1-) Un circuito secuencial tiene una entrada y una salida. El diagrama de estado se muestra abajo. Diseñe un circuito secuencial con:
  - (a) FFT
  - (b) FF RS



# FF tipo T

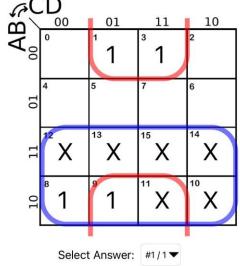
A	В	С	D	A	В	C	<b>T1</b>	<b>T2</b>	T3
0	0	0	0	0	1	1	0	1	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	0	1	0	0	0
0	0	1	1	1	0	0	1	0	1
0	1	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0
0	1	1	0	0	0	1	0	1	0
0	1	1	1	0	1	0	0	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	1	0	1	1	1	1	1

Por partes para entenderlo

	Pres	ente			Futuro	
A	В	C	D	A	В	C
0	0	0	0	0	1	1
0	0	0	1	1	0	0
0	0	1	0	0	0	1
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	0	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1

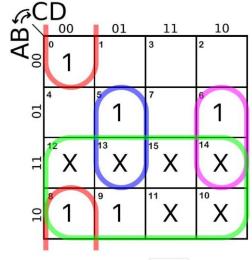
	Salidas	
<b>T1</b>	<b>T2</b>	<b>T3</b>
0	1	1
1	0	0
0	0	0
1	0	1
0	0	0
0	1	0
0	1	0
0	0	1
1	1	0
1	1	1

**KMaps funciones** 



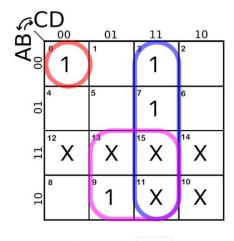
 $S = \overline{B}D + A$ 





Select Answer: #1/1▼

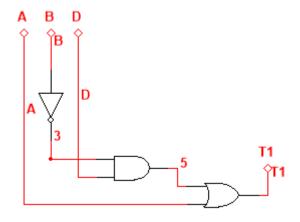
$$S = \overline{B}\overline{C}\overline{D} + B\overline{C}D + BC\overline{D} + A$$



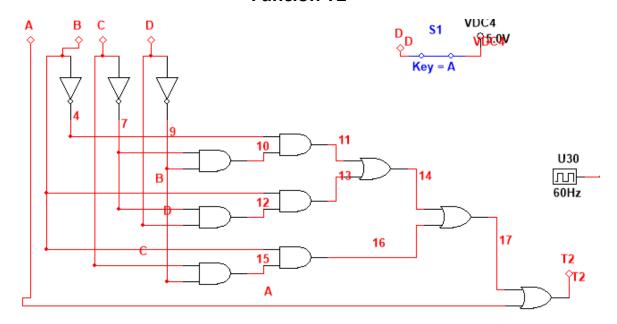
Select Answer: #1/1▼

$$S = \overline{A}\overline{B}\overline{C}\overline{D} + CD + AD$$

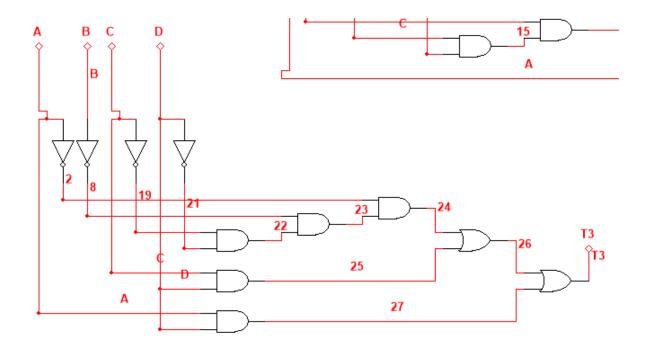
# **Funcion T1**



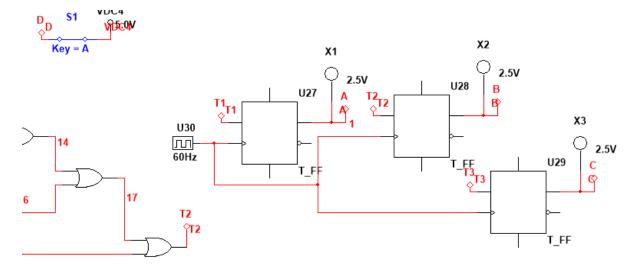
# **Funcion T2**



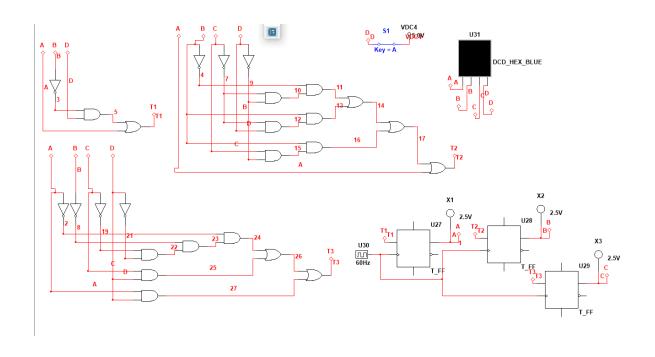
Funcion T3



Flip flop



Completo:



# FF tipo RS

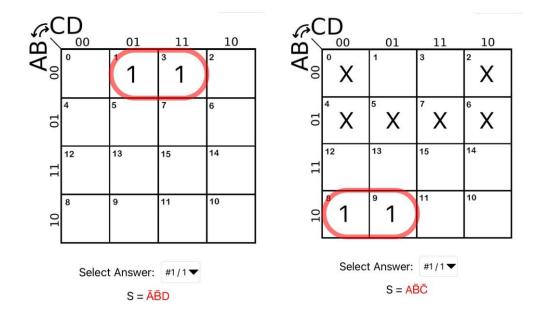
	ESTAI	DO PRES	SENTE	X	ESTA	DO FUT	TURO			SALI	DAS		
	A	В	C		A	В	C	SA	RA	SB	RB	SC	RC
0	0	0	0	0	0	1	1	0	X	1	0	1	0
0	0	0	0	1	1	0	0	1	0	0	X	0	X
1	0	0	1	0	0	0	1	0	X	0	X	X	0
1	0	0	1	1	1	0	0	1	0	0	X	0	1
2	0	1	0	0	0	1	0	0	X	X	0	0	X
2	0	1	0	1	0	0	0	0	X	0	1	0	X
3	0	1	1	0	0	0	1	0	X	0	1	X	0
3	0	1	1	1	0	1	0	0	X	X	0	0	1
4	1	0	0	0	0	1	0	0	1	1	0	0	X
4	1	0	0	1	0	1	1	0	1	1	0	1	0

Por partes para que se entoenda:

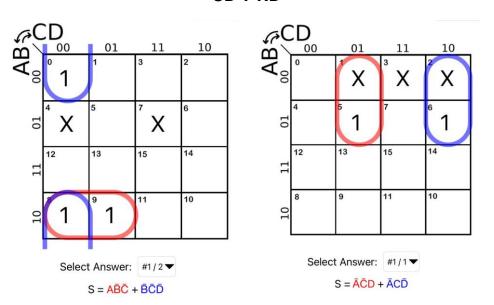
	ESTAI	DO PRES	SENTE	X	ESTA	DO FUT	URO
	A	В	C		A	В	C
0	0	0	0	0	0	1	1
U	0	0	0	1	1	0	0
1	0	0	1	0	0	0	1
1	0	0	1	1	1	0	0
2	0	1	0	0	0	1	0
2	0	1	0	1	0	0	0
3	0	1	1	0	0	0	1
3	0	1	1	1	0	1	0
1	1	0	0	0	0	1	0
4	1	0	0	1	0	1	1

	SALIDAS							
S	SA	RA	SB	RB	SC	RC		
	0	X	1	0	1	0		
	1	0	0	X	0	X		
	0	X	0	X	X	0		
	1	0	0	X	0	1		
	0	X	X	0	0	X		
	0	X	0	1	0	X		
	0	X	0	1	X	0		
	0	X	X	0	0	1		
	0	1	1	0	0	X		
	0	1	1	0	1	0		

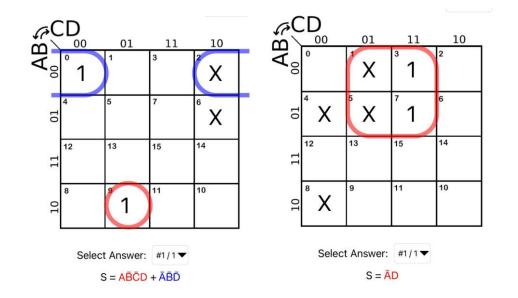
Kmaps y funciones SA Y RA

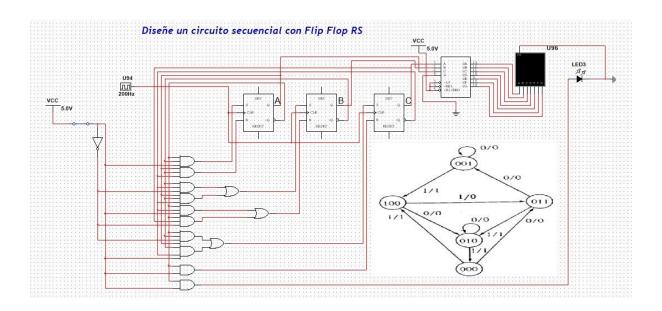


### **SBYRB**



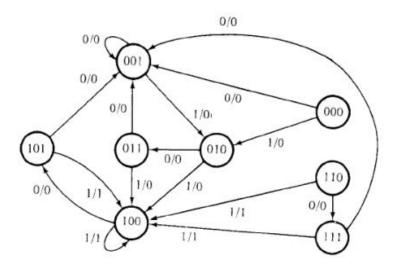
**SCYRC** 





2-) Un circuito secuencial tiene una entrada y una salida. El diagrama de estado se muestra abajo. Diseñe un circuito secuencial con:

### (a) FF RS



	ESTA	DO PRES	ENTE	X	EST	ADO FUT	URO			SAL	IDA		
	A	В	C		A	В	C	SA	RA	SB	RB	SC	RC
0	0	0	0	0	0	0	1	0	X	0	X	1	0
U	0	0	0	1	0	1	0	0	X	1	0	0	X
1	0	0	1	0	0	0	1	0	X	0	X	X	0
1	0	0	1	1	0	1	0	0	X	1	0	0	1
2	0	1	0	0	0	1	1	0	X	X	0	1	0
	0	1	0	1	1	0	0	1	0	0	1	0	X
3	0	1	1	0	0	0	1	0	X	0	1	X	0
3	0	1	1	1	1	0	0	1	0	0	1	0	1
4	1	0	0	0	1	0	1	X	0	0	X	1	0
4	1	0	0	1	1	0	0	X	0	0	X	0	X
5	1	0	1	0	0	0	1	0	1	0	X	X	0
3	1	0	1	1	1	0	0	X	0	0	X	0	1
6	1	1	0	0	1	1	1	X	0	X	0	1	0
0	1	1	0	1	1	0	0	X	0	0	1	0	X
7	1	1	1	0	0	0	1	0	1	0	1	X	0
/	1	1	1	1	1	0	0	X	0	0	1	0	1

Por separado para que se entienda:

	ESTA	DO PRES	ENTE	X	EST	ADO FUT	URO
	A	В	C		A	В	C
0	0	0	0	0	0	0	1
U	0	0	0	1	0	1	0
1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0
2	0	1	0	0	0	1	1
Δ	0	1	0	1	1	0	0
3	0	1	1	0	0	0	1
3	0	1	1	1	1	0	0
4	1	0	0	0	1	0	1
4	1	0	0	1	1	0	0
5	1	0	1	0	0	0	1
3	1	0	1	1	1	0	0
6	1	1	0	0	1	1	1
0	1	1	0	1	1	0	0
7	1	1	1	0	0	0	1
1	1	1	1	1	1	0	0

			SAL	.IDA			
	SA	RA	SB	RB	SC	RC	
	0	X	0	X	1	0	
	0	X	1	0	0	X	
	0	X	0	X	X	0	
	0	X	1	0	0	1	
	0	X	X	0	1	0	
	1	0	0	1	0	X	
	0	X	0	1	X	0	
	1	0	0	1	0	1	
	X	0	0	X	1	0	
	X	0	0	X	0	X	
	0	1	0	X	X	0	
	X	0	0	X	0	1	
	X	0	X	0	1	0	
	X	0	0	1	0	X	
	0	1	0	1	X	0	
	X	0	0	1	0	1	
	SA					RA	
AB\CX	00 0	1 11	10	AB\CX	00	01	11
OO O1		1 1	+	00		X	X
11		X X		11			
10		X X		10			
	SA = BX					RA = CX'	
	SB		Lia		T	RB	T
AB\CX OO	00 0	1 11 1 1	10	AB\CX OO	00 X	O1	11
01	X			01		1	1
11 10	X			10	X	1 X	1 X
	SB = A'B'X				RB	= BX + BC	
	SC					RC	
AB\CX	00 0	1 11	10	AB\CX	00	O1	11
	1		X	00		X	1
00			3.7				-
00 01 11	1 1		X	O1 11		X	1

