

 [Nemecxpetr](#) / [Digital-electronics-1](#) MIT License

☆ 0 stars 🍴 0 forks

☆ Star

👁 Unwatch ▼

[Code](#)[Issues](#)[Pull requests](#)[Actions](#)[Projects](#)[Wiki](#)[Security](#)[Insights](#)[Settings](#) main ▼

...

[Digital-electronics-1](#) / [Labs](#) / [03-vivado](#) / [README.md](#)

Nemecxpetr Update README.md

 1 contributor

Raw

Blame



149 lines (96 sloc) | 6.18 KB

3 Vivado

Lab assignment

1. Preparation tasks (done before the lab at home). Submit:

- ☒ Figure or table with connection of 16 slide switches and 16 LEDs on Nexys A7 board.

2. Two-bit wide 4-to-1 multiplexer. Submit:

- ☒ Listing of VHDL architecture from source file `mux_2bit_4to1.vhd` with syntax highlighting,
- ☒ Listing of VHDL stimulus process from testbench file `tb_mux_2bit_4to1.vhd` with syntax highlighting,
- ☒ Screenshot with simulated time waveforms; always display all inputs and outputs.

3. A Vivado tutorial. Submit:

- ☒ Your tutorial for Vivado design flow: project creation, adding source file, adding testbench file, running simulation, (adding XDC constraints file).

1. Table with connection of 16 slide switches and 16 LEDs on Nexys A7 board

From this [schematic](#) we can see the connections of slide switches and LEDs on Nexys A7 board and to which FPGA pins they are connected and how.

SW	SW pins	SW Connection type	LEDs	LED pins	SW Connection Type
1	J15	IOSTANDARD LVCMOS33	1	H17	IOSTANDARD LVCMOS33
2	L16	IOSTANDARD LVCMOS33	2	K15	IOSTANDARD LVCMOS33
3	M13	IOSTANDARD LVCMOS33	3	J13	IOSTANDARD LVCMOS33
4	R15	IOSTANDARD LVCMOS33	4	N14	IOSTANDARD LVCMOS33
5	R17	IOSTANDARD LVCMOS33	5	R18	IOSTANDARD LVCMOS33
6	T18	IOSTANDARD LVCMOS33	6	V17	IOSTANDARD LVCMOS33
7	U18	IOSTANDARD LVCMOS33	7	U17	IOSTANDARD LVCMOS33
8	R13	IOSTANDARD LVCMOS33	8	U16	IOSTANDARD LVCMOS33
9	T8	IOSTANDARD LVCMOS18	9	V16	IOSTANDARD LVCMOS33
10	U8	IOSTANDARD LVCMOS18	10	T15	IOSTANDARD LVCMOS33
11	R16	IOSTANDARD LVCMOS33	11	U14	IOSTANDARD LVCMOS33
12	T13	IOSTANDARD LVCMOS33	12	T16	IOSTANDARD LVCMOS33

SW	SW pins	SW Connection type	LEDs	LED pins	SW Connection Type
13	H6	IOSTANDARD LVCMOS33	13	V15	IOSTANDARD LVCMOS33
14	U12	IOSTANDARD LVCMOS33	14	V14	IOSTANDARD LVCMOS33
15	U11	IOSTANDARD LVCMOS33	15	V12	IOSTANDARD LVCMOS33
16	V10	IOSTANDARD LVCMOS33	16	V11	IOSTANDARD LVCMOS33

2. Two-bit wide 4-to-1 multiplexer

Architecture from mux_2bit_4to1.vhd

```
architecture Behavioral of mux_2bit_4to1 is
begin

    f_o <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;

end architecture Behavioral;
```

Stimulus process from tb_mux_2bit_4to1.vhd

```
p_stimulus : process
begin

    s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00";
    s_sel <= "00"; wait for 50 ns;

    s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "01";
    s_sel <= "00"; wait for 50 ns;

    s_d <= "00"; s_c <= "00"; s_b <= "01"; s_a <= "00";
    s_sel <= "00"; wait for 50 ns;

    s_d <= "00"; s_c <= "00"; s_b <= "01"; s_a <= "01";
    s_sel <= "00"; wait for 50 ns;

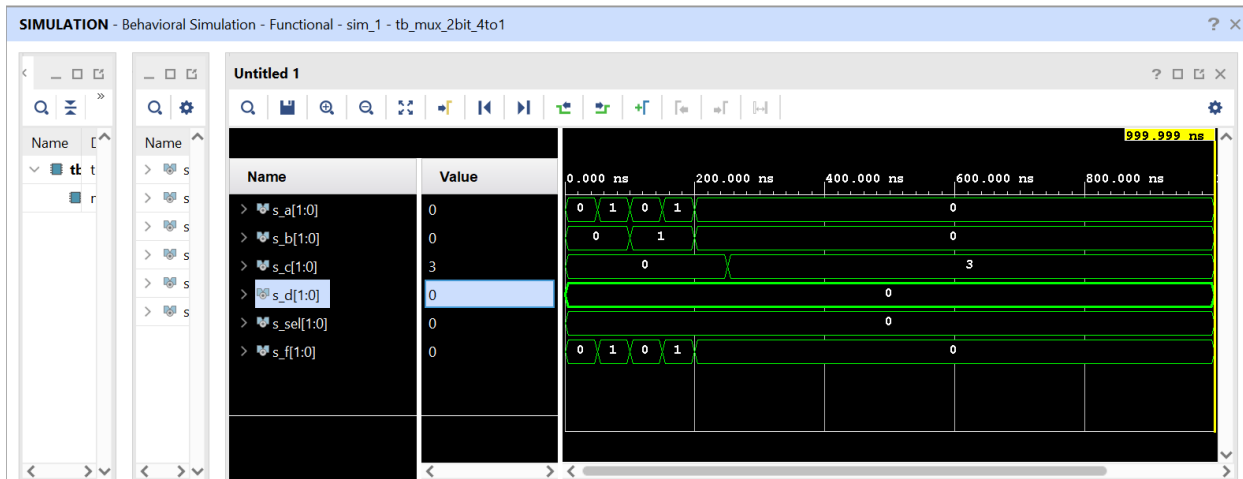
    s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00";
    s_sel <= "00"; wait for 50 ns;
```

```
s_d <= "00"; s_c <= "11"; s_b <= "00"; s_a <= "00";
s_sel <= "00"; wait for 50 ns;
```

```
report "Stimulus process finished" severity note;
```

```
wait;
end process p_stimulus;
```

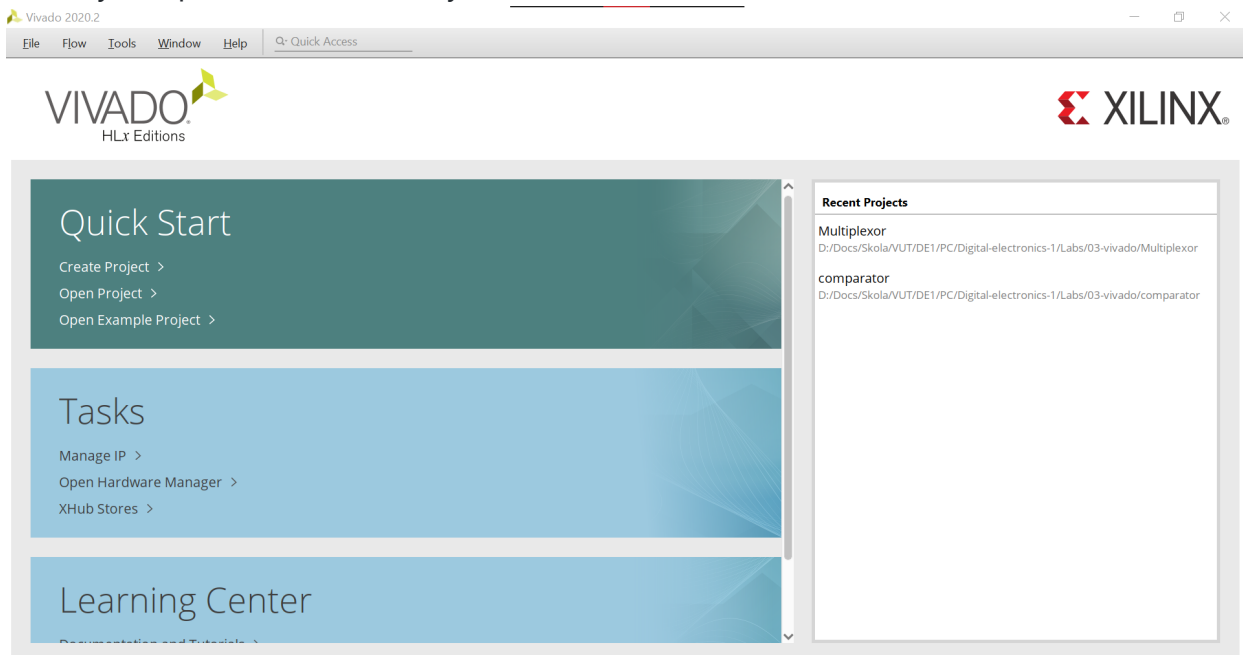
Simulated time waveforms:



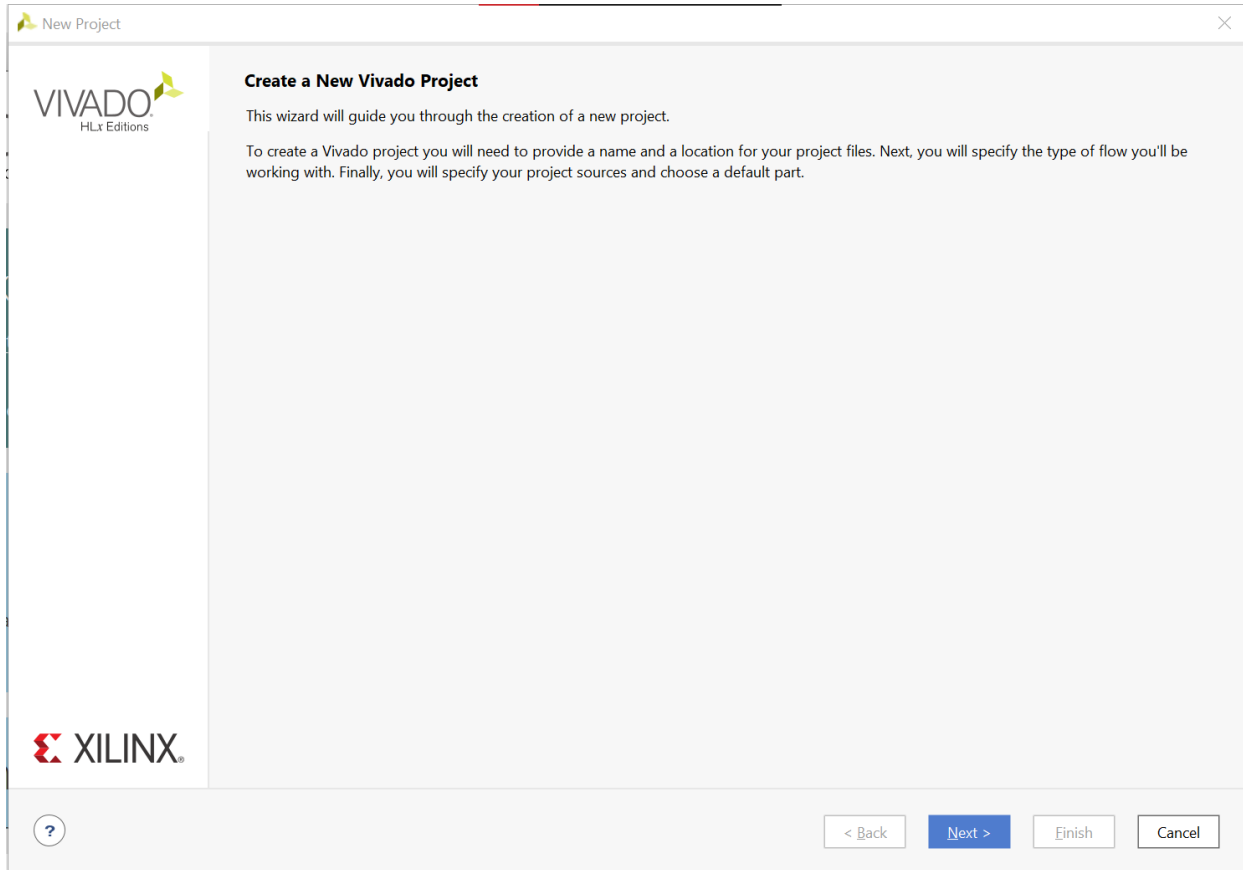
3. A Vivado tutorial

If you want to create vhdl code in Vivado here is a short tutorial on how to begin.

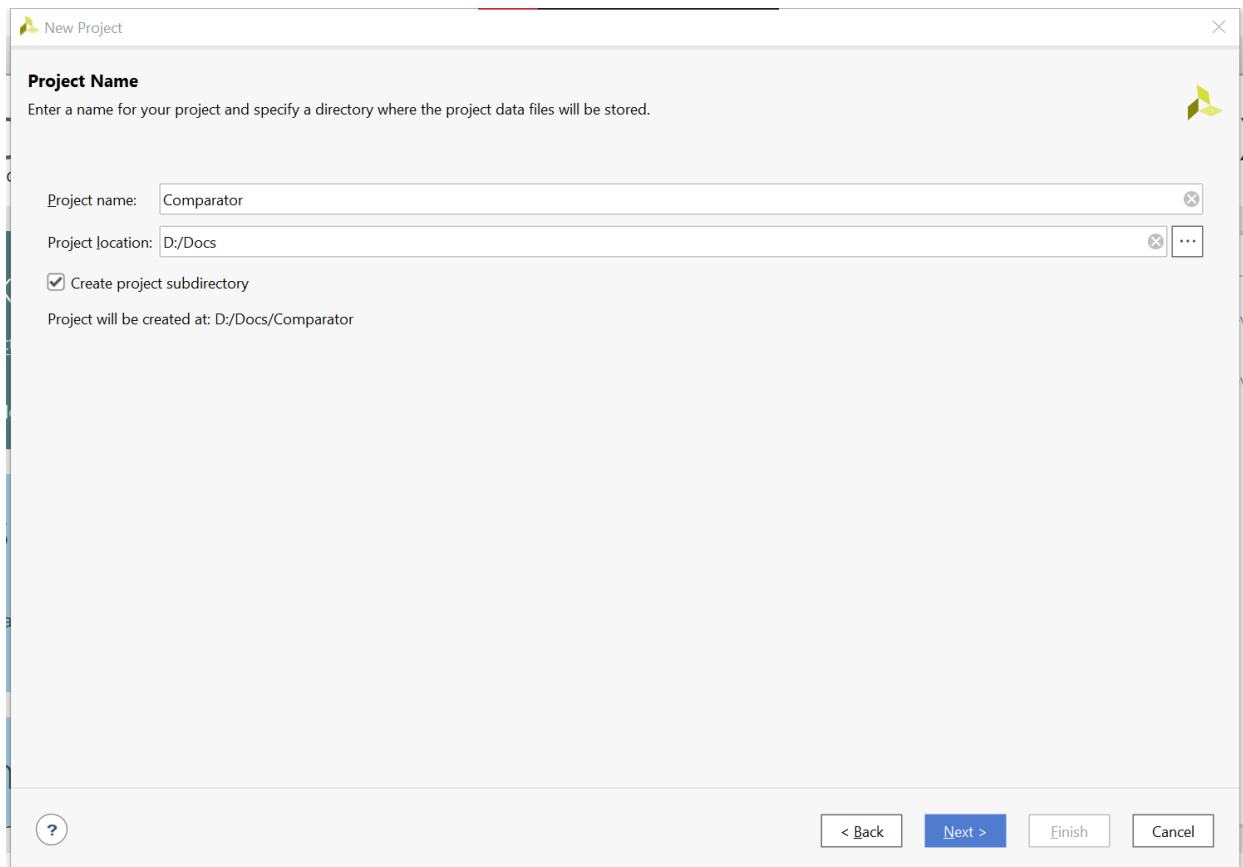
When you open Vivado 2020.2 you should see this window:



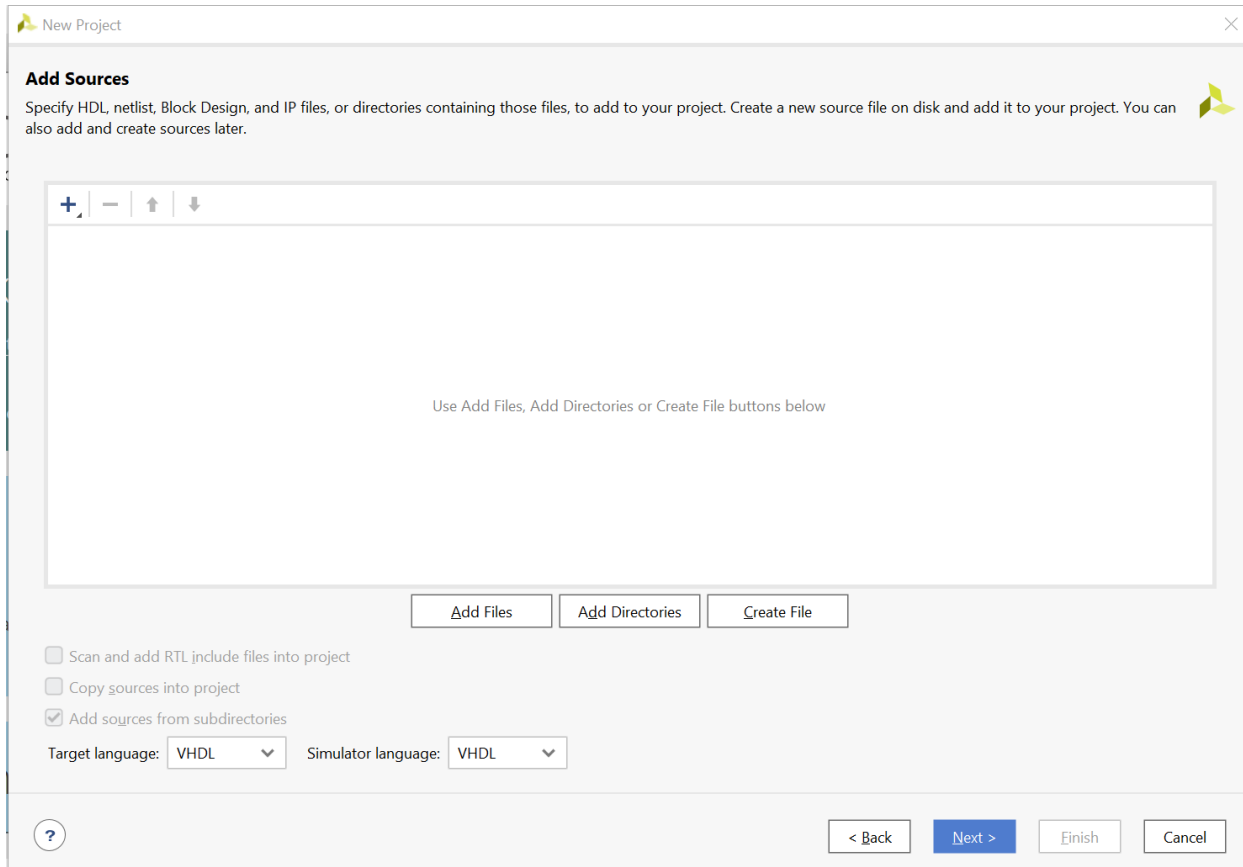
- Click on create project .



- Click **Next** to choose Project name and Location.
- Project name is in our case **Comparator** and location is a place on our hard drive where all the files are gonna be stored in one file folder. This folder is gonna be created by the program and named with the Project name.

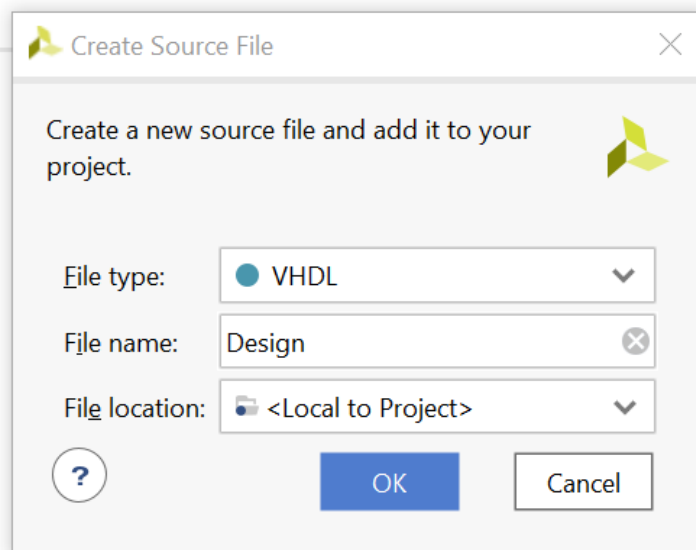


- Click **Next** until you see the page for adding sources.
- Don't worry though. You can always click **Back** and change everything you need.



- **Create File** to create an equivalent to `design.vhd` in EDA Playground.

ter.



Add Files

Add Directories

Create File

- Click **Next** and you can add constraints (.xdc) You can skip this step for you can add them later while working on the project. But the proces is same as before. Constraints specifies which pin from a board (a board we are gonna add to our project in the next step) we are gonna use for which input or output signals of our code. That's basically a reason why it is ok to skip this step and do it

Next step is important for connection of our project to a particular board from Xilinx we want to use so pay attention. If you want to use Nexys 50 but don't have it [here](#) is a tutorial on how to add it.

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All
Family: All Speed: All Static power: All

Search: Q

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceivers
xc7k70tfbg676-1	676	300	41000	82000	135	0	240	8	0
xc7k70tfbv484-3	484	285	41000	82000	135	0	240	4	0
xc7k70tfbv484-2	484	285	41000	82000	135	0	240	4	0
xc7k70tfbv484-2L	484	285	41000	82000	135	0	240	4	0
xc7k70tfbv484-1	484	285	41000	82000	135	0	240	4	0
xc7k70tfbv676-3	676	300	41000	82000	135	0	240	8	0
xc7k70tfbv676-2	676	300	41000	82000	135	0	240	8	0
xc7k70tfbv676-2L	676	300	41000	82000	135	0	240	8	0
xc7k70tfbg676-1	676	300	41000	82000	135	0	240	8	0
xc7k70tfbg484-2L	484	285	41000	82000	135	0	240	4	0

Navigation: ? < Back **Next >** Finish Cancel

- Click on **Boards** and choose which one you are gonna be using. In our case we will use Nexus A7-50T

Default Part
Choose a default Xilinx part or board for your project.

Parts | **Boards**

[Reset All Filters](#) Install/Update Boards

Vendor: Name: Board Rev:

Search:

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Re
Nexys A7-50T		digilentinc.com	1.0	xc7a50ticsg324-1L	324	D.0

[? < Back Next > Finish Cancel](#)

- Click **Next** and you will see a summary. If there is some problem or you made a mistake feel free to go back and change everything we did so far.

New Project Summary

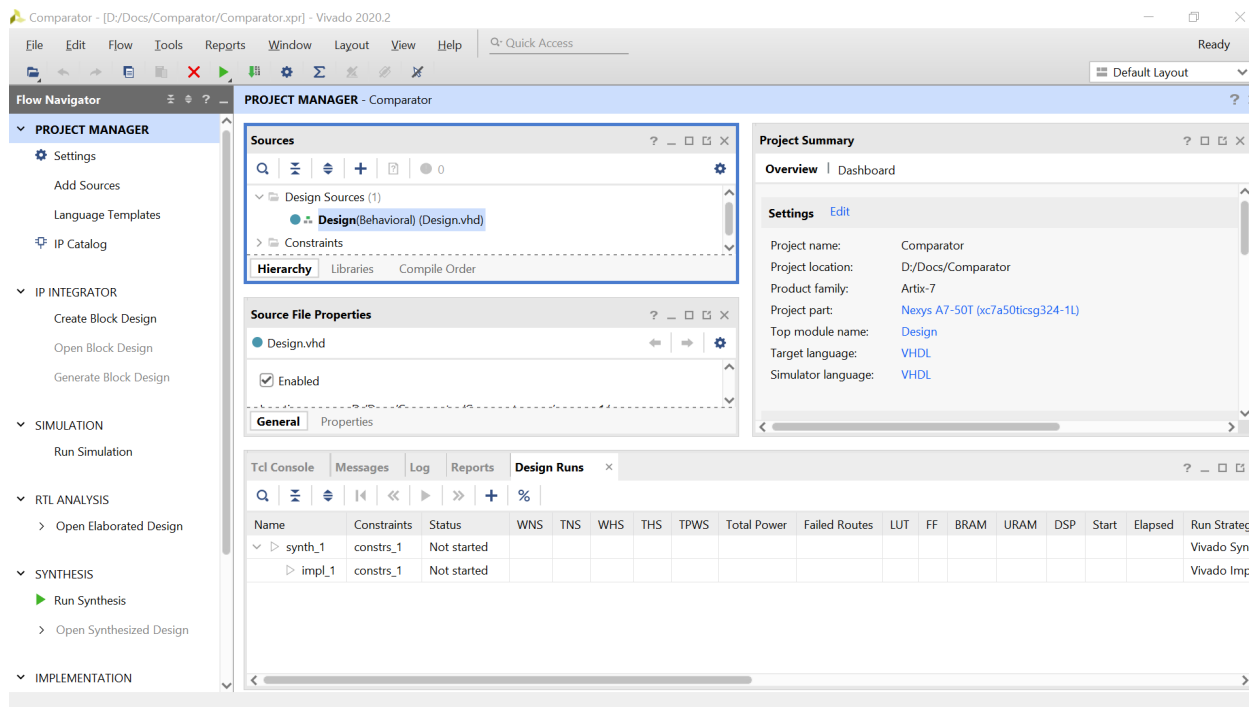
- A new RTL project named 'Comparator' will be created.
- 1 source file will be added.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:
 Default Board: Nexys A7-50T
 Default Part: xc7a50ticsg324-1L
 Product: Artix-7
 Family: Artix-7
 Package: csg324
 Speed Grade: -1L

VIVADO HLx Editions

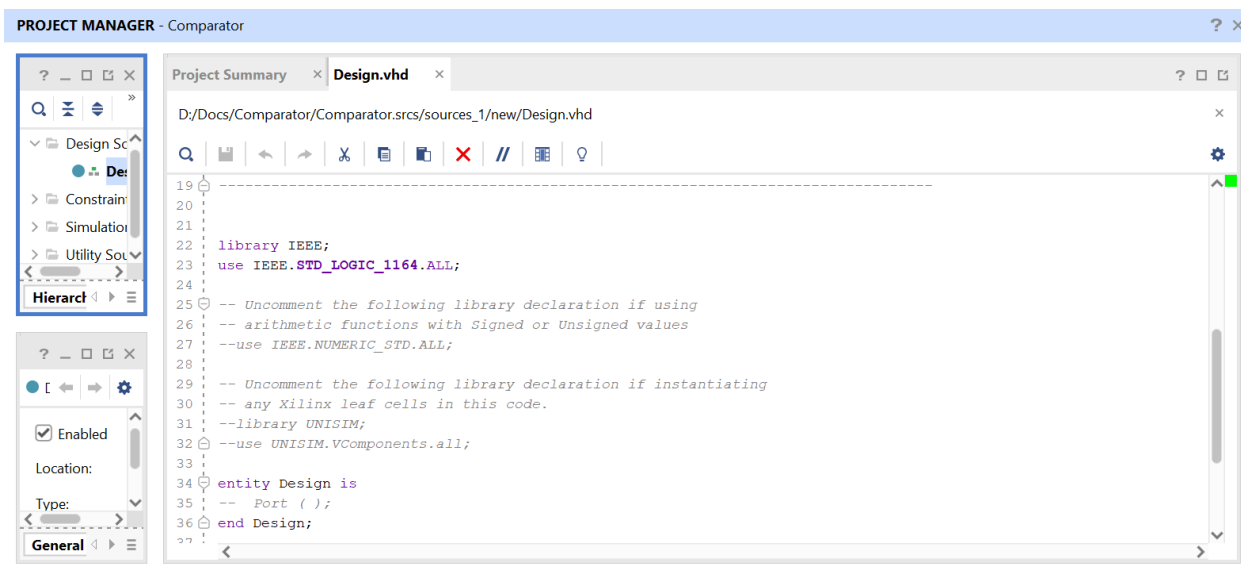
XILINX To create the project, click Finish

[? < Back Next > Finish Cancel](#)

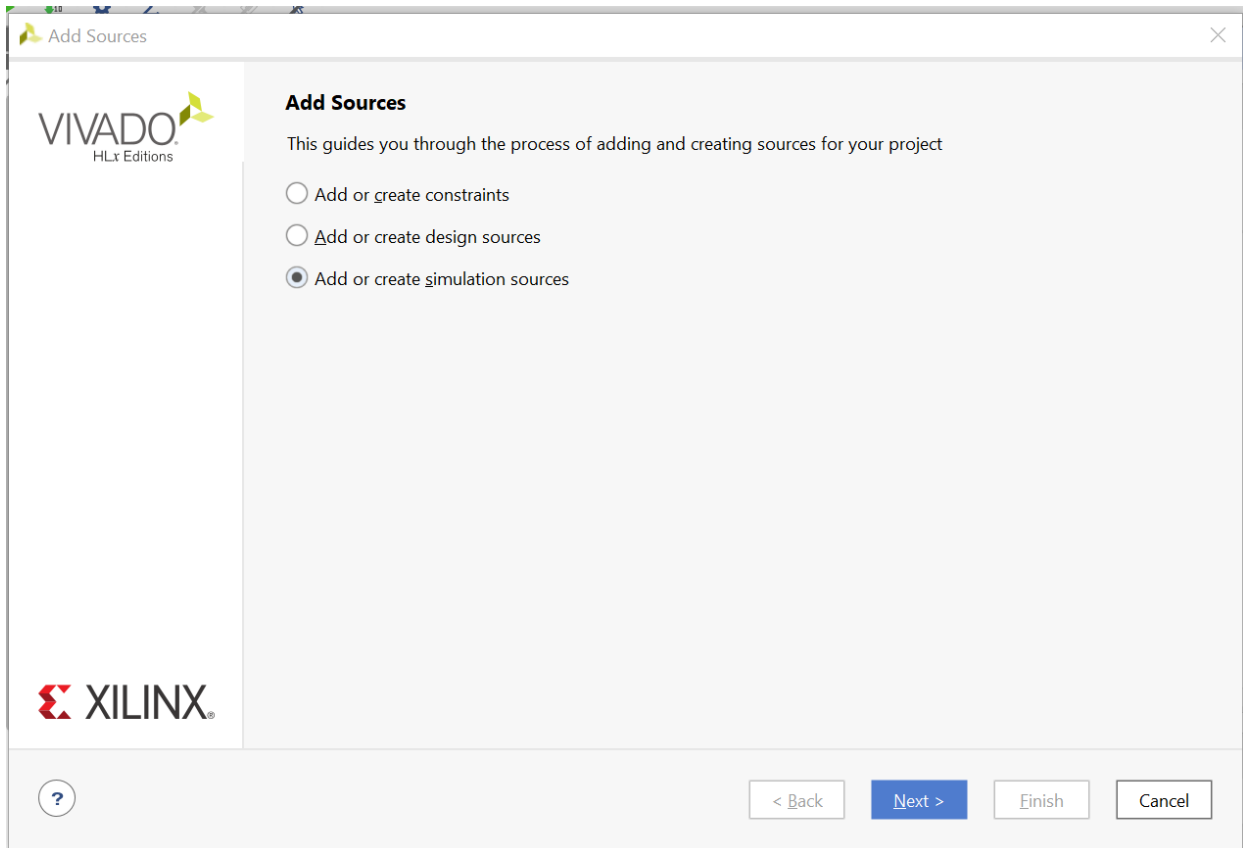
- Click **Finish** and the project will be made.



- In sources you can open your .vhd file and write your code.



- For creating a "testbench" file chose File/Add Sources or a shortcut Alt + A
- There you can create simulation sources (process is the same as when creating the Design.vhd earlier)



- Last thing you might be interested in is running the simulation.
- That is done via Flow/Run Simulation/Run Behavioral Simulation

