**NATIONAL RESEARCH UNIVERSITY HIGHER SCHOOL OF ECONOMICS**

**SCHOOL OF COMPUTER ENGINEERING**

**HSE TIKHONOV MOSCOW INSTITUTE OF ELECTRONICS AND MATHEMATICS**

**PROJECT PROPOSAL**

**Simulation of Macro - and Micro- Fusion Procedure in CPU Core**

Nikita Stepanov, BIV161

Advisor:

Elena Ivanova, Associate professor

Moscow

2020

***Abstract*—This proposal, prepared mostly for scientific researches and students of technical universities, will describe the processes of micro- and macro- fusion in CPU core and assess its impact on the performance of different computer systems. Working on program modeling of operation fusion, we have defined concepts of microprocessing technologies, its usage in AMD and Intel architectures, and its influence on processing rate. Users of the result program will have an opportunity to trace fusions of macro- and micro- operations with using application programming interface. Furthermore, they will be able to check the fusion impact on the entire system processing rate by changing appropriate parameters.  
*Keywords*—*CPU core; micro-operation; macro-operation; fusion***

INTRODUCTION

**Background**

One of significant problems of microprocessing technologies is the lack of bandwidth in CPU core blocks. Some of the solutions, such as quantum processor architecture, are not reachable in our times. Thus, there are several relevant ways of fixing this issue performed by leading companies. In this work we are observing the most valuable one. It refers to improving the bandwidth by decreasing the total amount of operations done in CPU core.

**Problem Statement**

This work is an attempt to illustrate the operation fusion by creating the programming model of such processes and to conduct the research of its influence on system performance. There is lack of information could be found in open sources and books. Consequently, in our work we will try to illuminate the following questions:

1. Which operations could be used in operation fusion?

2. How does the architecture of processor influence the operation fusion?

3. What is the difference between macro- and micro- fusion?

4.What results can be reached by using the benefits of operation fusion?

**Research stages**

Development stages could be divided into following steps:

1. Defining of the micro-operation fusion.

2. Defining of the macro-operation fusion.

3. Comprehension of the fusion algorithm work.

4. Development of the program back-end and algorithm realization.

5. Development of the graphical user interface.

**Professional Significance**

The findings of this study will redound to the benefit of microprocessing technologies development considering micro- and macro- fusion as implicated instrument which improves the entire system performance. Eventual programming model can be used in different cases. It may be useful while conducting science research in the sphere of information technologies or for students of different universities while studying.

LITERATURE REVIEW

Until recently, many researchers have shown interest in the field of operation fusion in CPU core. Using contemporary technologies, they have carried out a lot of experiments to observe this research field. Their papers had a great influence on the microprocessor’s development in modern world. The key aim of all performed researches is to find the way to improve CPU’s processing rate. Some of the achieved results and studies are reviewed here. The largest share of research information in the sphere of CPU’s operation fusions is provided by Agner’s Fog manual [1][2] and Intel company [3]. Besides these sources, a considerable contribution was made by Celio, Dabbelt, A. Patterson and Asanović, who’s work illustrates the ways to avoid ISA Bloat with macro-op fusion for RISC-V [4]. On the other hand, Taram, Venkat and Tullsen from University of California investigated micro-op fusions as method of increasing efficiency of RISC-V systems in their work[5].

One of the most significant research was done by Agner Fog. His manuals [1][2] contain information about experiments with different AMD and Intel processors. There are numerous code examples in them, which show processes of micro- and macro- fusions in CPU core. Also, Agner Fog also investigates whether different operations could be fused for each chosen processor. Based on the results he provides a thorough analysis of operation fusion influence on system efficiency, instruction timings and latency. Another important thing is that Agner’s Fog works are usually updated. All in all, his manuals illuminate the field of research. Therefore, they are used in different internet resources and scientific works.

The other equally important source of information is Intel 64 and IA-32 Architectures optimization Reference Manual [3]. It provides basic data about micro- and macro- fusions and its effect on improvement of front-end throughput. Furthermore, there is a detailed description of how operations are being fused in the CPU core with some code examples. Intel company is using their own investigations in the question of operation fusion to make their processors more efficient and innovative. As it can be seen, after each such investigation manual is being updated. Thus, Intel processors are rather more relevant for fusions in CPU core and are showing better rate increasing results, compared to AMD and ARM architectures, which can also be seen in Agner’s Fog manuals.

Next research discussed in this review was conducted by the group of people from University of California at Berkeley: Celio, Dabbelt, A. Patterson and Asanović [4]. Their paper mostly referred to the methods of avoiding ISA Bloat with using operation fusion in RISC-V architecture systems. The key point of the study is to reduce the effective instruction count by leveraging macro-op fusion. Researchers provide some charts, graphs, and histograms in their work to illustrate the impact of using macro-op fusion on RV64GC system. For better understanding of the theme, there are also idioms and rules of macro-op fusion. Furthermore, in the paper researchers share interesting experience of their failures and attempts to leverage macro-operation fusion while using different microprocessors and approaches.

The last but not the least source of information is the research made by Taram, Venkat and Tullsen from University of California, San Diego [5]. They consider micro- and macro- fusions as one of the front-end optimization instruments along with such thing as micro-op cache. The same as previous researchers, they have also used operation fusion for system efficiency and microprocessor rate. Moreover, in the results of the study there is some useful information about how implementing CSD (Circuit Switched Data) technology influences performance of micro-op cache hit rate while using operation fusion in CPU core.

METHODS

The main goal of this study is to create programming module which simulates micro- and macro- fusion in CPU core and to investigate its influence on system efficiency. To reach this aim, we will firstly provide definition of the fusion algorithm. This information could be reached by conducting several tests with different processor architectures and variations of executable programs. This work had been done by Agner Fog in his manuals [1][2] with huge number of examples and explanations. Consequently, by combining data from these sources and from Intel’s manual [3], we can receive a complete description of the fusion algorithm.

The next step of our work will be to bring the result algorithm to life by using modern technologies and programming tools. After a thorough analysis we have chosen Python as main program language for its wide specter of opportunities, high productivity and speed, extensive support libraries and high adaptability. Furthermore, Python has numerous modules which may come handy in the future development of the programming module. It can also be mentioned that we will use one of those modules for creating user interface for our eventual program.

The final step of our work includes investigation of fusion impact on system performance. To conduct the tests, we will use different contemporary processor architectures and will change parameters of the fusion for our needs. The conclusion about system efficiency will be based on the results of these tests.

RESULTS ANTICIPATED

The expected benefits of the research program will accrue for consumers, firms, scientists and other students through an improved understanding of the operations occurred in core and performance of CPU processes modeling. Areas of research main emphasis are the influence of micro- and macro- operations fusion in CPU core on the entire system efficiency, and model analysis of compiling concepts that affect improvement in processing speed and other quality attributes. The result model emphasizes understanding the ways of executing instructions in microprocessor, analysis of its performance, and assessment of operations fusion intended to influence that performance. An important organizing principle and end goal of this work is to provide relevant visible model, which simulates code compiling and gives information about the consequences of each micro- or macro- operation fusion.

The result product of the research will mostly be useful for students of technical Universities. It provides detailed information about CPU core processes and allows to trace the way of executing assembler instructions and commands from the beginning to the end. This innovative idea of modeling and analyzing of operations in microprocessor will also have impact on other scientific researches. Scientists can use the result program to emulate CPU core processes and find ways to improve its efficiency.

CONCLUSIONS

The primary goal of this study is to create autonomous programming model for simulating micro- and macro- fusion in CPU core. By collecting and analyzing data from previous investigations, we will completely define fusion algorithm. Working on creating modeling program and implementation of algorithm, we will use contemporary methods and tools of development. The result program can be useful for different people going to conduct the researches and studies in the sphere of microprocessors. It provides data about operation fusion and allows to do tests with changes in parameters of the fusion. All in all, we hope that our program will have an application in the world of processor development.

REFERENCES

[1] Agner Fog, "The microarchitecture of Intel, AMD and VIA CPUs", Technical University of Denmark, September 2018.

[2] Agner Fog, "Optimizing subroutines in assembly language", Technical University of Denmark, August 2019.

[3] Intel 64 and IA-32 architectures optimization reference manual, Intel Corporation, September 2019.

[4] C. Celio, D. Dabbelt, D. A. Patterson and K. Asanovic, "The Renewed Case for the Reduced Instruction Set Computer: Avoiding ISA Bloat with Macro-Op Fusion for RISC-V", Electrical Engineering and Computer Sciences University of California, Berkeley, July 2016.

[5] M. Taram, A. Venkat and D. M. Tullsen, "Mobilizing the Micro-Ops: Exploiting Context Sensitive Decoding for Security and Energy Efficiency", University of California, San Diego, June 2018.