* Finish the requirements document
  + SPI - Andrew  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
  + AXI  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
  + Async/FIFO - Devon  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
  + Registers  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
* Finish design/functionality documents
  + SPI - Eric  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
  + AXI - Devon  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
  + Async/FIFO - Devon/Eric  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
  + Registers - Andrew/Devon/Eric  
    –Expected Completion Date: 5/12/2020 EOD  
    --Current Status: Complete
* Cross-check requirements document(signoff) \*refine?
  + SPI
    - Andrew
    - Devon
    - Eric
  + AXI
    - Andrew
    - Devon
    - Eric
  + Async/FIFO
    - Andrew
    - Devon
    - Eric
  + Registers
    - Andrew
    - Devon
    - Eric
* Design Implementation
  + Stage 1: AXI and Registers
    - Address select / Chip select functionality - Andrew  
      –Expected Completion Date: 5/15/2020 EOD  
      --Current Status: Complete
    - FSM Setup for read/write - Eric  
      –Expected Completion Date: 5/15/2020 EOD  
      --Current Status: In progress
    - Read Routine – Eric  
      –Expected Completion Date: 5/15/2020 EOD  
      --Current Status: To Do
    - Write Routine – Andrew  
      –Expected Completion Date: 5/15/2020 EOD  
      --Current Status: In Progress
    - Register mapping/wrapper - Devon  
      –Expected Completion Date: 5/15/2020 EOD  
      --Current Status: In Progress
    - Register submodule functionality(write masks, TOW, etc.) - Devon  
      –Expected Completion Date: 5/15/2020 EOD  
      --Current Status: To Do
  + Stage 2: Async/FIFO and SPI
    - Parametrizable FIFO  
      –Expected Completion Date: 5/21/2020 EOD  
      --Current Status: To Do
    - Signal Synchronization across clock domains  
      –Expected Completion Date: 5/21/2020 EOD  
      --Current Status: To Do
    - Slave SPI  
      –Expected Completion Date: 5/21/2020 EOD  
      --Current Status: To Do
    - Master SPI  
      –Expected Completion Date: 5/21/2020 EOD  
      --Current Status: To Do
  + Stage 3: Submodule Assembly  
    –Expected Completion Date: 5/22/2020 EOD  
    --Current Status: To Do
  + Stage 4: Functional Verification / Synthesis
    - Testbench creation  
      –Expected Completion Date: 5/26/2020 EOD  
      --Current Status: To Do
    - Simulation  
      –Expected Completion Date: 5/27/2020 EOD  
      --Current Status: To Do
    - STA analysis/adjustments  
      –Expected Completion Date: 5/28/2020 EOD  
      --Current Status: To Do
    - FPGA testing  
      –Expected Completion Date: 5/29/2020 EOD  
      --Current Status: To Do

Note: Planning and scheduling documentation moved to designated excel sheet starting at stage 2.