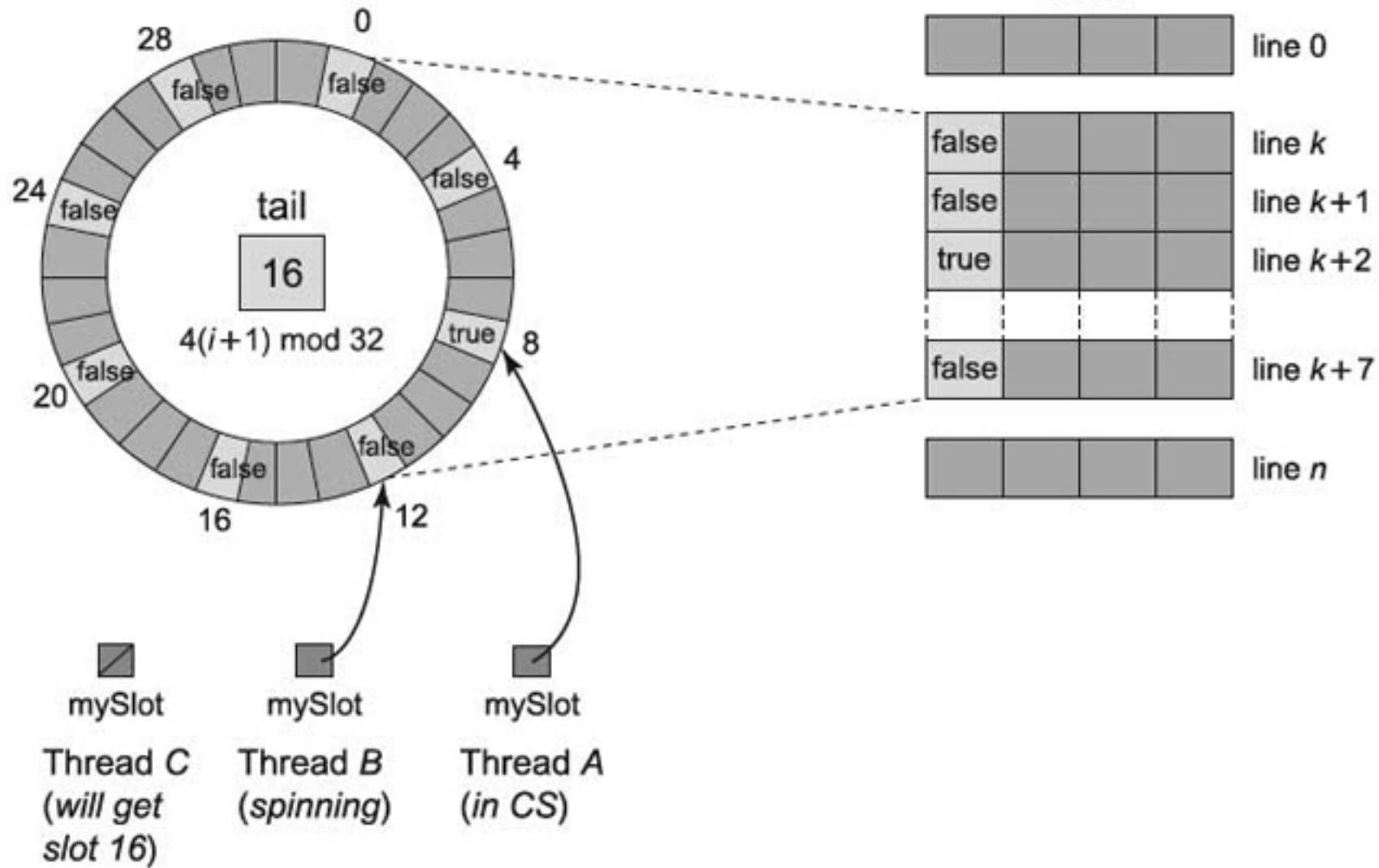**FIGURE 7.8B** The ALock with padding to avoid false sharing. In part (a), the ALock has eight slots which are accessed via a modulo 8 counter. Array entries are typically mapped into cache lines consecutively. As illustrated, when thread A changes the status of its entry, thread B, whose entry is mapped to the same cache line k, incurs a false invalidation. In part (b), each location is padded so it is 4 apart from the others with a modulo 32 counter. Even if array entries are mapped consecutively, the entry for B is mapped to a different cache line from that of A, so B's entry is not invalidated when A invalidates its entry.