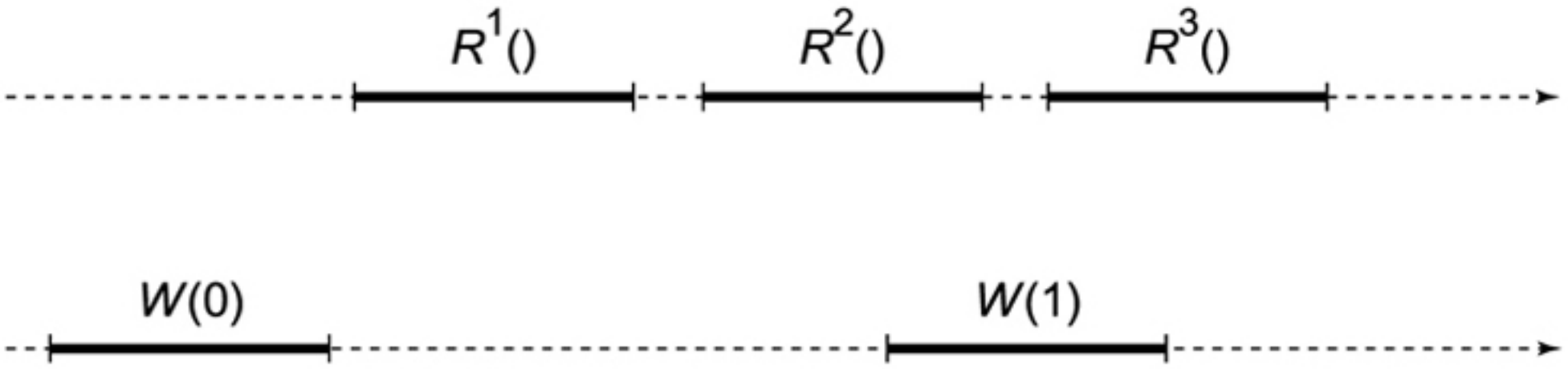


**FIGURE 4.3** An SRSW register execution: $R^i$ is the $i$-th read and $W(v)$ is a write of value $v$. Time flows from left to right. No matter whether the register is *safe*, *regular*, or *atomic*, $R^1$ must return 0, the most recently written value. If the register is *safe*, then because $R^2$ and $R^3$ are concurrent with $W(1)$, they may return any value in the range of the register. If the register is *regular*, $R^2$ and $R^3$ may each return either 0 or 1. If the register is *atomic*, then if $R^2$ returns 1, then $R^3$ must also return 1, and if $R^2$ returns 0, then $R^3$ may return 0 or 1.

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