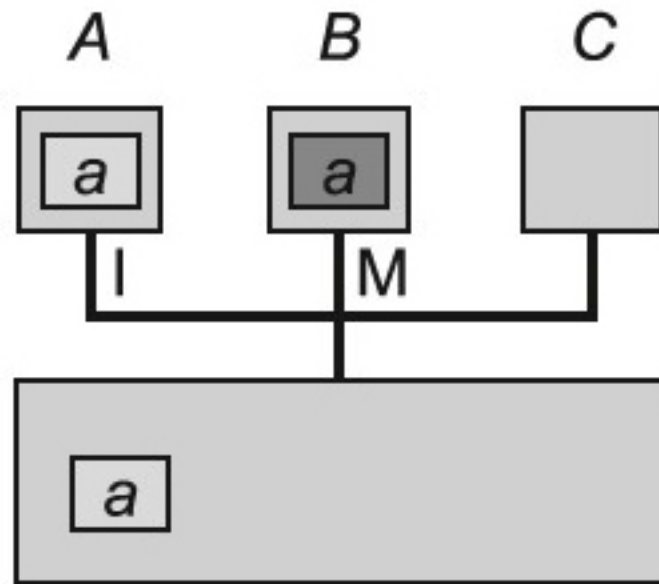


(c)



**FIGURE B.5C** Example of the MESI cache-coherence protocol's state transitions. (a) Processor A reads data from address *a*, and stores the data in its cache in the *exclusive* state. (b) When processor B attempts to read from the same address, A detects the address conflict, and responds with the associated data. Now *a* is cached at both A and B in the *shared* state. (c) If B writes to the shared address *a*, it changes its state to *modified*, and broadcasts a message warning A (and any other processor that might have those data cached) to set its cache line state to *invalid*. (d) If A then reads from *a*, it broadcasts a request, and B responds by sending the modified data both to A and to the main memory, leaving both copies in the *shared* state.