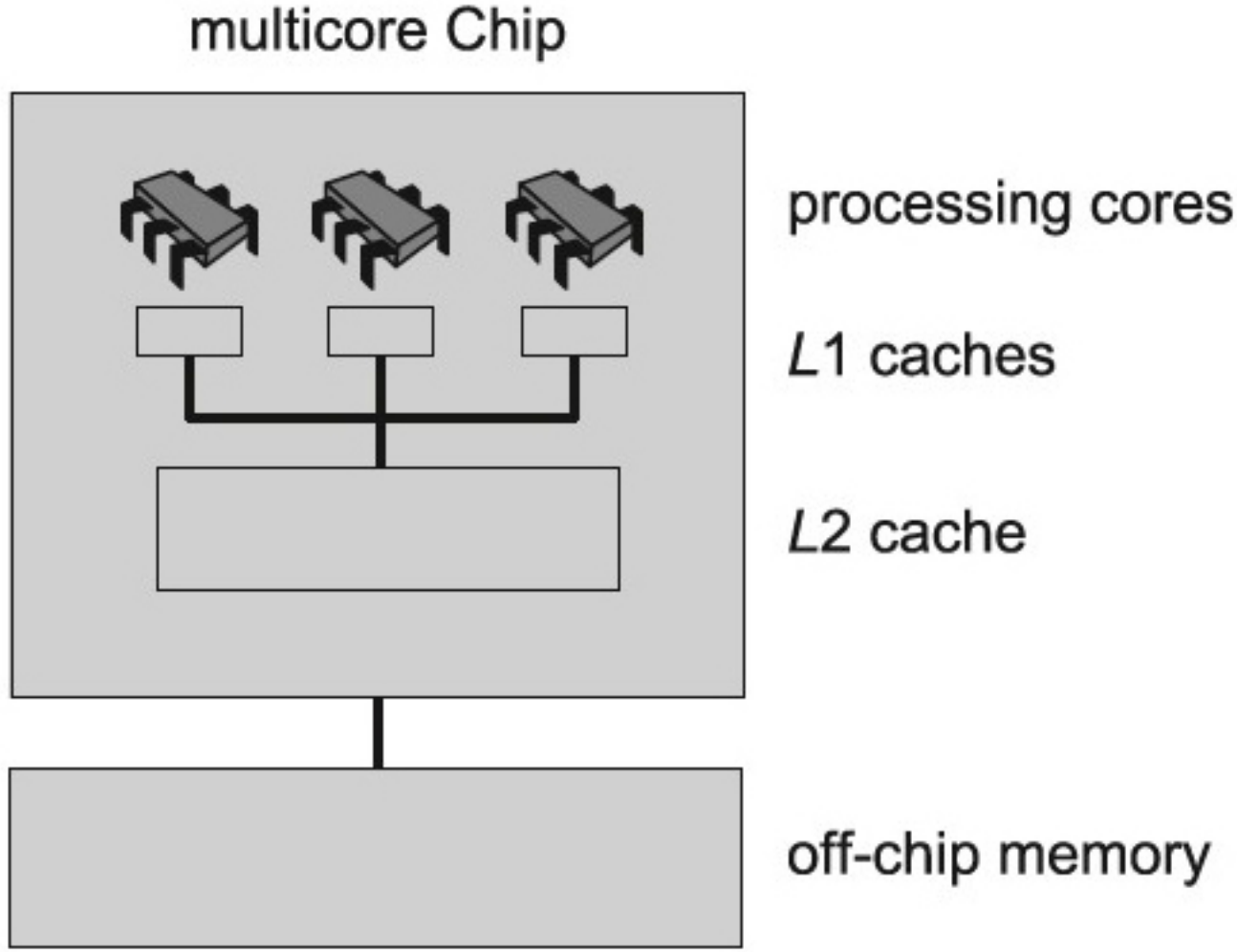

FIGURE B.6 A multicore SMP architecture. The *L2* cache is on chip and shared by all processors while the memory is off-chip.