CS2100 Final Exam (AY 2022-23, Sem1)

Question #: 1

Please answer this question as **Question 1** on the provided PAPER answer sheet. Please IGNORE the True/False choice for this question.

Part a (4 marks)

Implement the following function with at most two 3x8 decoders and a single 4x16 decoder, all with active high enables (En) and active high outputs, and as few OR gates as possible. OR gates may have a fan-in of at most 4. Assume that inverted inputs (e.g. A') are not available, though the values 0 and 1 are available. S2 is the most significant bit and S0 is the least significant bit.

(Note: The answer sheet provides two 3x8 decoders. Draw in a 4x16 decoder if you need it.)

(4 marks)

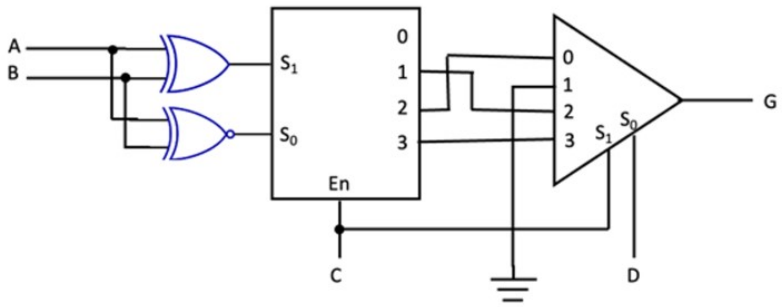
f(A, B, C, D, E, F, G) = $\sum m(22, 26, 28, 30, 58, 60, 90, 92)$

Part b (3 marks)

Implement the above function using a single 3x8 multiplexer with no enable line (i.e. always enabled) and as few gates as possible. Except for NOT gates, gates have a fan-in of at most 4. For simplicity this time you may assume that inverted inputs (e.g. A') and 0 and 1 are all available. S2 is the most significant bit and S0 is the least significant bit. (3 marks)

Part c (3 marks)

Write down the simplified sum-of-products expression for this circuit. S1 is the most significant bit, S0 is the least significant bit. (3 marks)



Item Weight: 1.0

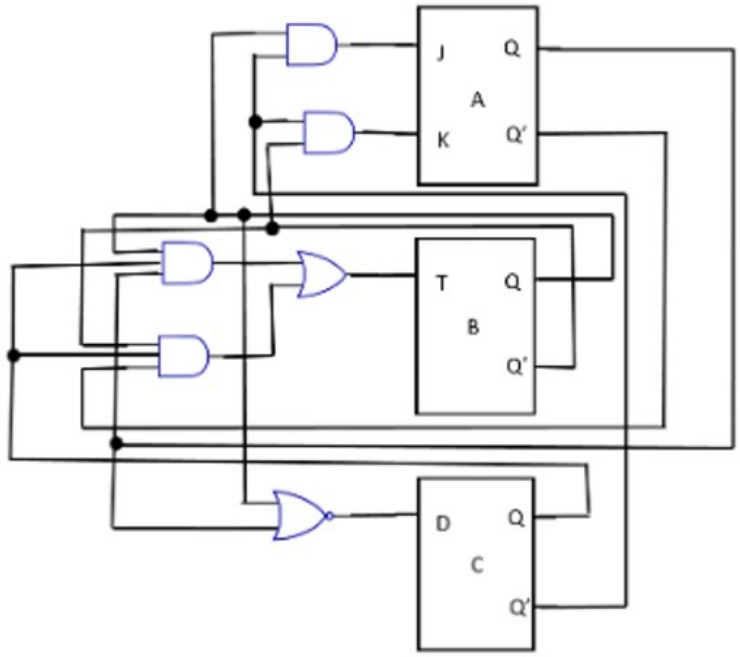
Question #: 2

Please answer this question as **Question 2** on the provided PAPER answer sheet. Please IGNORE the

True/False choice for this question.

Part a

Draw the state diagram for the following circuit (3 marks)



(The following parts are independent of part a)

We are building a lift controller for a building with four floors. A state machine keeps track of which floor a lift is now.

The state machine has two inputs X and Y which indicate the floor the lift should go to (00 =level 1, 01 =level 2, 10 =level 3 and 11 =level 4). It has one output D that controls the doors of the lift. When D =0, the doors are closed, and when D =1, the doors the open.

When the lift is at a floor indicated by XY, the state machine opens the door (D =1), and stays at that floor. When XY is changed to a different floor, the state machine closes the door (D =0), then the lift goes up or down until it reaches the floor indicated by XY, after which the state machine opens the door. The lift motor is controlled by a separate circuit that we do not need to concern ourselves with.

The clock inputs of the flip-flips are triggered by a circuit that produces a clock pulse whenever the lift passes a floor. Thus, on the rising edge of each pulse the floor number represented by the flip-flops either increases or decreases by one floor.

Part b

Draw the state diagram for our lift state machine. (2 marks)

Part c

Implement our state machine using only T flip-flops and as few logic gates as possible, and draw its circuit. You may use any logic gates (NOT, AND, OR, NAND, XOR, etc.) of any fan-in. Again, we assume that the clock input is connected to a circuit that generates a clock pulse each time the lift car passes a floor. You do not need to draw the clock input. (5 marks)

Item Weight: 1.0

Question #: 3

Let's say the instruction set of our MIPS processor is {lw, sw, beq, add, addi, sub, subi, and, andi, or, ori, slt}. If ALUsrc signal is stuck-at-0, then: (1 mark)

Item Weight: 1.0

Question #: 4

Let's say the instruction set of our MIPS processor is {lw, sw, beq, add, addi, sub, subi, and, andi, or, ori, slt}. If MemToReg signal is stuck-at-0, then: (1 mark)

Item Weight: 1.0

Question #: 5

Consider the following instruction group in MIPS: (4 marks)

R-type	I-type (except lw)	Load	Store	Branch	Jump
25%	29%	18%	13%	12%	3%

Fill in the following:

a. What percentage of all the instructions uses data memory? __1__%

b. What percentage of all the instructions uses instruction memory? __2__%

c. What percentage of all the instructions uses sign extension? __3__%

d. The sign extend unit produces an output for every instruction in the above group that is being executed. Say whether True or False: __4__

Item Weight: 4.0

Question #: 6

Consider an 8-way set associative mapped cache of size 512 KB with cache block size of 1 KB. There are 7 bits in the tag. For this cache setup, answer the following: (4 marks)

Fill in the following:

a.Each set has __1__ number of cache blocks

b.Number of bits for set index is __2__ bits

c.Number of bits for the address of main memory is __3__ bits

d.Size of main memory is __4__ MB

Item Weight: 4.0

Question #: 7

Let's say the given MIPS codes will be executed using a 5-stage pipeline processor. The target address of the jump instruction will be calculated at the same stage as beq instruction. You can assume the pipeline is implemented with data forwarding, branch prediction strategy as "NOT taken" and early branching technique is used. (3 marks)

```
# $s6 = 0x01001200
# $s3 = 0, $s4 = 2, $s5 = 502
L2: add $t1, $s3, $s3
    add $t1, $t1, $t1
    add $t1, $t1, $s6
    lw  $t0, 0($t1)
    slt $t2, $t0, $s5
    beq $t2, $0, L1
    add $s3, $s3, $s4
    j L2
L1:
```

Address	Memory
0x01001200	101
0x01001204	102
0x01001208	201
0x0100120C	202
0x01001210	301
0x01001214	302
0x01001218	401
0x0100121C	402
0x01001220	501
0x01001224	502
:	
:	

Fill in the following:

a. In the first iteration of the code, what is the number of stall(s)/delay(s) incurred before the execution stage of the bne instruction? Ans: __1__

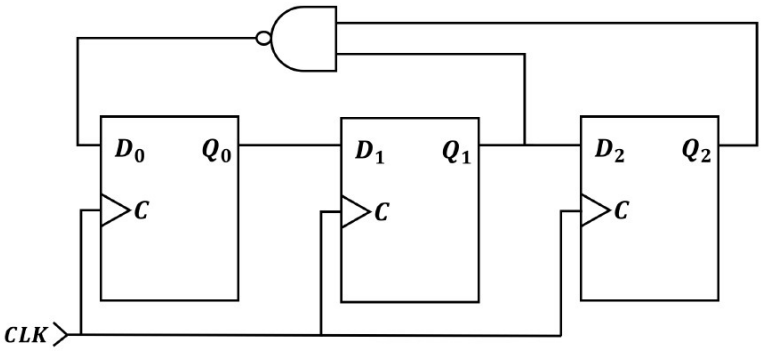
b. Calculate the number of clock cycles required to complete the execution (all the stages) of all the instructions in the first iteration. Ans: __2__

c. At what clock-cycle, does the first instruction (i.e., i1) in the second iteration of the loop will be fetched? Ans: __3__

Item Weight: 3.0

Question #: 8

Examine the following circuit design. The table shows the initial values of the system.



	Q_2	Q_1	Q_0	D_2	D_1	D_0
Initial State	**0**	**0**	**0**	**0**	**0**	**1**
CLK1						
CLK2						
CLK3						
CLK4						
CLK5						
CLK6						
CLK7						

*Hint: Fill in the table to help you solve the following questions.

What will be OUTPUT STATE $(Q_2Q_1Q_0)$ in **CLK6**?

(1 mark)

Item Weight: 1.0

Question #: 9

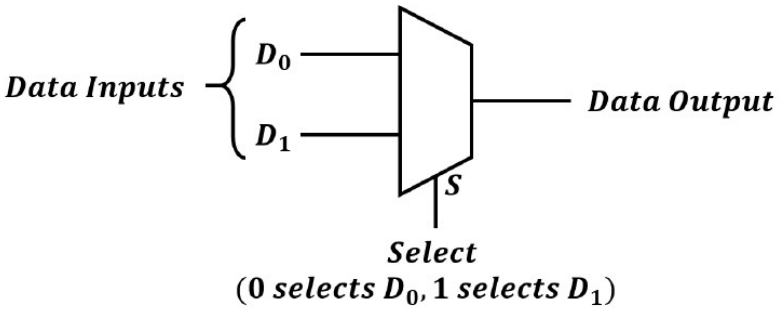
Excluding the Initial State $(Q_2Q_1Q_0 = 000)$, how many UNIQUE STATES $(Q_2Q_1Q_0)$ are there in the system?

(1 mark)

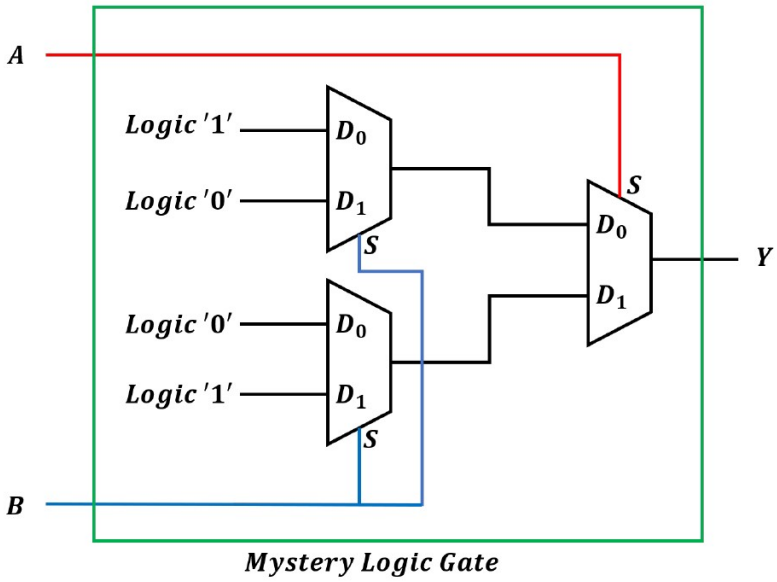
Item Weight: 1.0

Question #: 10

A 2:1 Multiplexor is as shown below.



The circuit below shows a “Mystery Logic Gate” implemented using the three 2:1 Multiplexers. For the Logic Gate, signals ‘A’ and ‘B’ are the inputs and signal ‘Y’ is the output.

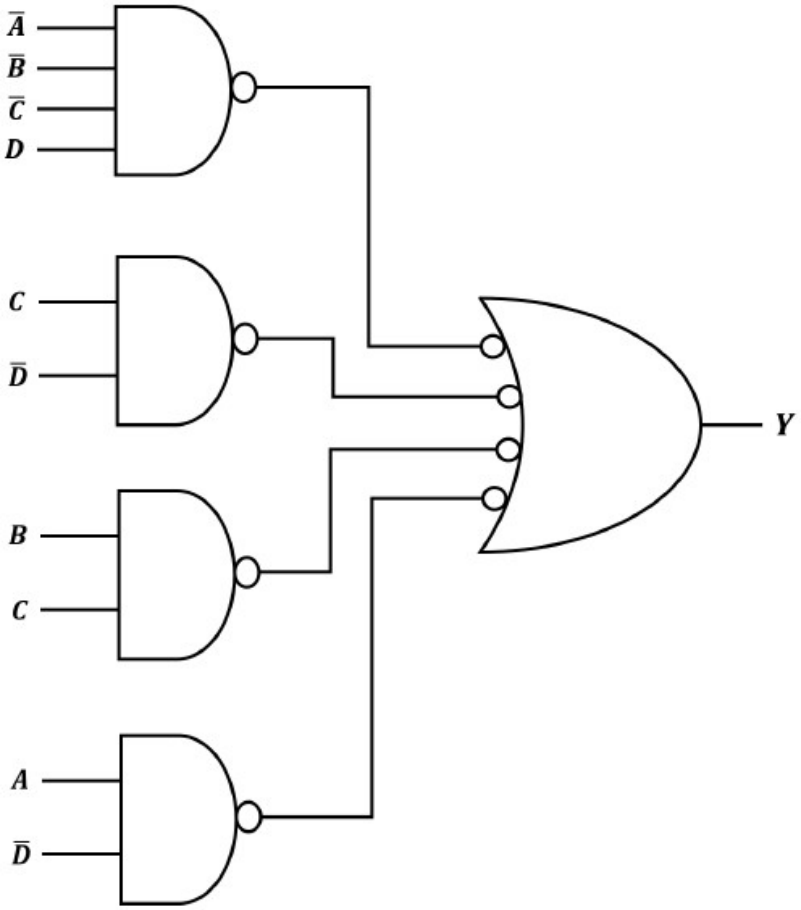


The mystery logic gate is _____ (1 mark)

Item Weight: 1.0

Question #: 11

Choose the correct Boolean expression for the given circuit design. (1 mark)



Item Weight: 1.0