Tutorial Week 8

Continuous Assessment

Cover Sheet

Student Name: Neo Sahadeo	**Student Number: D0026460**

Programme: Comp and Sys ops	**Stage:1**	**Complete Student Checklist:** Re-read brief ✅ References and Bibliography ✅ Proofread ✅
Module: Hardware		
Due Date: 26/11/2024	**No. Pages:**	
Lecturer(s) Name: Paula Duffy		
Assignment No. and/or Description/Topic: Tutorial Week 8		**Mode of Submission:** Softcopy Hardcopy

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Signature……Neo Sahadeo…..…… **Date**…25/11/2024……..

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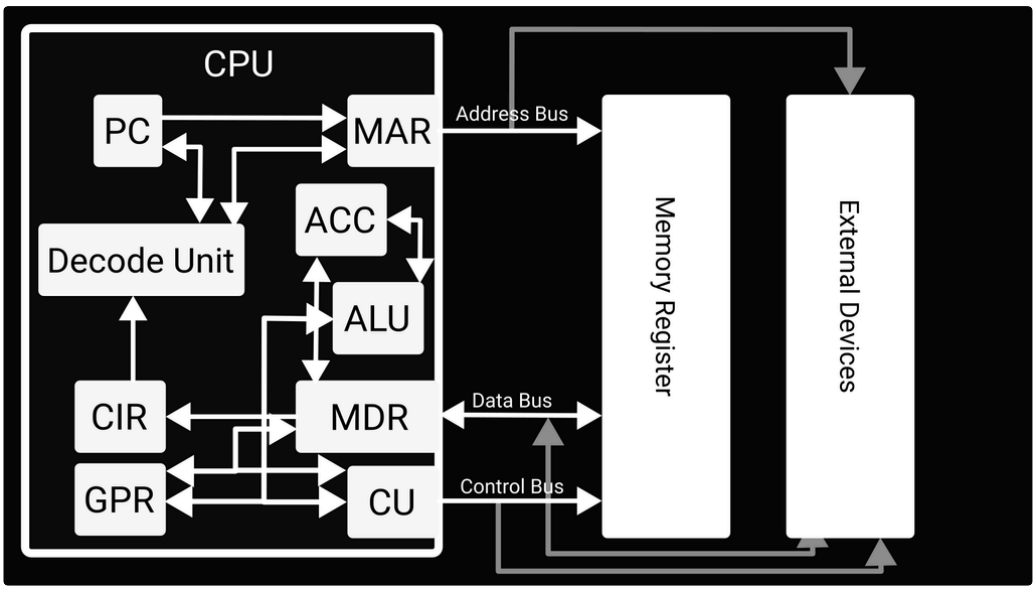
Introduction

This is my week 8 lab tutorial.

a)

CPU Architecture



The CPU connects to external components using busses. There are 3 busses.

The control and address busses are unidirectional and carry control and address signals respectively to RAM and external devices.

The data bus is bidirectional and carries data back and forth between RAM and external devices.

The internal architecture of the CPU consists of registers, a decode unit, and ALU.

Decode unit

This part of the CPU is responsible for understanding instructions sent to it. The instruction will be made up of two parts; the operation/opcode and the operand.

ALU

The arithmetic and logic unit performs operations on operands supplied, such as addition, subtration, and swaps.

Instruction Cycle:

1. Program counter is set to the next memory address (default is 0000)
2. The MAR then sends a signal to RAM and waits for the CU to send a signal on the address bus
3. The CU sends a signal to load the data at the memory location into the MDR and then CIR
4. The program counter increments by 1
5. The decode unit then processes the instruction
6. The instruction is then executed

During this process the instruction set can be used to send signal to external devices.

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b)

Registers

Registers are used to store information. They are an example of volatile memory, where if the computer were turned off, the information in the register will be lost.

Three examples of registers found in the CPU:

1. Accumulator Register
2. Program Counter
3. Instruction Register

Accumulator Register

The accumulator is used to do logical and arithmetic calculations. It is a temporary storage for operations carried out by the ALU. An example would be adding values from two different memory locations. The values at the locations should be fetched and put into the accumulator. The value is then placed into the ALU as the second value is loaded from memory. The result is then store in the ACC.

Current Instruction Register

The current instruction register holds the current instruction which the CPU can decode. The instruction value is made up of two parts. The first being the operation (opcode) and the second is the operands (What is Register in Digital Electronics ? 2023).

I wrote a small instruction set to demonstrate this in my Python 16-bit CPU emulator (Main (main.py) — A 16-bit CPU in Python 3 documentation n.d.).

INSTRUCTION SET	A	B	C	D
Logic or Arithmetic	0	1	0	1
operation code 1	0	0	0	0
operation code 2	0	0	0	0
zero replace	0	0	0	0
swap	0	0	0	0
less than	0	0	0	1
greater than	0	1	0	0
equal to	0	0	0	0
a register	0	0	0	0
b register	0	0	0	0
RAM	0	0	0	0
select register 'a' or RAM	0	0	0	0
	0	1	0	0
	0	0	0	0
	1	0	1	0
Direct write to register 'a' or use ALU	1	1	0	1

Program Counter

The program counter register keeps track of the address of the next instruction to be processed (What is Register in Digital Electronics? 2023).

The counter is incremented after an instruction is fetched, unless that instruction is a jump; such as a for loop in Python.

Other registers explained

GPR (General purpose registers) are registers than can be used various desired tasks.

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c)

How Data Moves Between Memory and Storage to the CPU

The CPU requests data from RAM first based on the MAR. It will send a signal on the control bus to load the data.

If there is no dataT in RAM (a miss) then a signal is sent to the i/o controller on the south bridge.

This then loads data from the respective storage device into RAM on the data bus where the CPU can send a control signal to read it.

Once the data is found the data is sent on the data bus to the MDR based on the instruction from the CIR and CU signalling.

Data cannot be directly read from the storage device as there is no direct connection and the south bridge devices run significantly slower the CPU which will drastically effect performance if it were possible for a CPU to read directly from storage devices.

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d)

SRAM and DRAM

Static RAM and Dynamic RAM (RAM stands for Random-Access-Memory) are two type of memory found in a computer.

Static RAM uses transistors to store information where as dynamic RAM uses capacitors to store information (DRAM does implement a transistor to control whether to read or write to it) (St. Michael 2019). This results in the price disparity between SRAM and DRAM where SRAM is more expensive and faster, and DRAM is cheaper and slower. When I mention faster and slower throughout my explanation I am referring to access times.

SRAM is used as caches by the CPU. There are 3 layers of cache. L3 cache is the slowest of the caches and L1 is the fastest of the caches. The sizes of the caches shrink from L3 being the largest to L1 being the smallest. L1 cache is often as fast or faster than the processing speed of the CPU. All caches are located on the CPU in modern CPUs (Ware 2023).

DRAM on the other hand is slower, cheaper and larger than SRAM. Generally many gigabytes of RAM are relatively inexpensive when compared with the cost of other hardware components and SRAM.

SRAM cannot be upgraded without upgrading the CPU. DRAM can be swapped out and upgraded as long as the motherboard supports that version. The current version available today of DRAM is DDR5 (DDR5 stands for Double Data Rate 5).

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c)

Memory vs Storage

Memory is a volatile storage type versus storage which is non-volatile. Volatility describes whether the information is preserved when the power supply is turned off.

Memory is more expensive than storage as the complexity and cost of materials is greater than that of storage. As of 2024, a stick of 32GB DDR4 memory will cost the equivalent of 2TB of HDD storage.

There is generally two types of memory that consumers purchase:

- DIMM
- SO-DIMM

DIMM (Dual Inline Memory Module) is memory found in desktop (“tower”) computers. SO-DIMM (Small Outline Inline Memory Module) is memory found in laptops.

The two main types of storage are:

- Hard Disk Drives (HDD)
- Solid State Drives (SSD)

A HDD is high-capacity-low-cost storage. It has slower access times than SSDs.

A SSD is high-capacity-medium-cost storage. SSDs have a faster access time than HDD with the tradeoff of being more limited in storage capacity and cost. As of 2024, SSDs are a very affordable alternative to HDDs. Some pre-built computers offer NVMe (Non-Volatile Memory express) SSDs which offer even higher transfer rates as it connects through an M.2 slot on the motherboard rather than over SATA.

There are hybrid storage devices known as SSHDs. These are not as popular as the previous two storage devices and I have seen few uses outside the general enthusiast.

A general rule of thumb is to build your computer with as much memory to increase the longevity of the machine. The more memory that a computer has the slower it tends to slow down as software demands increase.

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e) i)

All bits are 1 -> 11111111111111111111111111111111

$$2^{32}-1=4294967295$$

4 294 967 295 is the maximum location it can access where all bits are 1.

ii)

The total number of locations would be 4 294 967 296.

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f)

CPU Performance

The CPUs performance is affected by cache memory, clock speed, and amount of cores.

Cache memory as discussed above will affect the performance of CPU. SRAM speeds have to at minimum meet the clock cycle rate of the CPU else the CPU will have to wait for the SRAM to transfer in data; bottle-necking the computer performance. SRAM cache size allows more data to “sit“ closer to the CPU increasing the efficiency of the computer. SRAM hit and miss rates will also effect performance. If the data is not found at the memory location in SRAM then data has to be fetched from DRAM which will affect the processing speed of the CPU.

CPU clock speed will affect the performance as this is the processing speed. Modern CPUs can process roughly 4 billion operations per second. Slower clock speeds mean that the CPU will process that amount of operations per second.

The amount of cores the CPU has will also affect performance. If there are more cores more work can be done simultaneously but this is often with the trade-of with individual clock speed. There are two main competitors in the CPU space which are Intel and AMD. AMD is more focused on more cores at a lower clock frequency vs Intel who focus on high clock speeds with less cores.

References

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