Explain Interrupt structure of 8086 processor

Interrupt is the method of creating a temporary halt during program execution and allows peripheral devices to access the microprocessor. The microprocessor responds to that interrupt with an **ISR** (Interrupt Service Routine), which is a short program to instruct the microprocessor on how to handle the interrupt.

1. There are three sources of interrupts for 8086:

1. Hardware interrupt-

These interrupts occur as signals on the external pins of the microprocessor. 8086 has two pins to accept hardware interrupts, NMI and INTR.

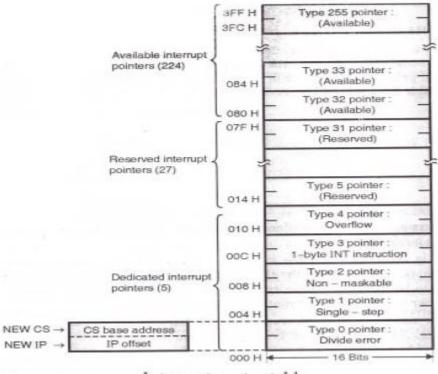
2. Software interrupt-

These interrupts are caused by writing the software interrupt instruction INT n where 'n' can be any value from 0 to 255 (00H to FFH). Hence all 256 interrupts can be invoked by software.

3. Error conditions (Exception or types)-

8086 is interrupted when some special conditions occur while executing certain instructions in the program. Example: An error in division automatically causes the INT 0 interrupt.

Interrupt Vector Table (IVT):



Interrupt vector table

The interrupt vector (or interrupt pointer) table is the link between an interrupt type code and the procedure that has been designated to service interrupts associated with that code.

→ 8000 supposets a total of 256 types of interoupt interoupt
its ISR. Thus a total of 1024 are mappined
for 256 interrupt types there, Interrupt vactor tole, setant at location 0000:0000 and ords at 0000 ores
> The interoupt type N is multiplied by 4 and
othe nexa decimal multiplication obtained gives the
affect address in the Renoth code degreet at which the IP and is addresses of the
intercept souvice mouths (ISA) are extended.
-> The execution automatically from new CS: IP.

- 1. The total interrupt vector table is divided into three groups namely,
 - A. Dedicated interrupts (INT 0.....INT 4)
 - B. Reserved interrupts (INT 5....INT 31)
 - C. Available interrupts (INT 32.....INT 225)

Dedicated interrupts (INT 0....INT 4):

INT 0 (Divide Error)-

- This interrupt occurs whenever there is division error i.e. when the result of a division is too large to be stored. This condition normally occurs when the divisor is very small as compared to the dividend or the divisor is zero.
- Its ISR address is stored at location 0 x 4 = 00000H in the IVT.

INT 1 (Single Step)-

- The microprocessor executes this interrupt after every instruction if the TF is set.
- It puts microprocessor in single stepping mode

INT 2 (Non mask-able Interrupt)-

The microprocessor executes this ISR in response to an interrupt on the NMI (Non mask-able Interrupt) line

INT 3 (Breakpoint Interrupt)-

• This interrupt is used to cause breakpoints in the program.

• It is useful in debugging large programs where single stepping is efficient.

INT 4 (Overflow Interrupt)-

• This interrupt occurs if the overflow flag is set and the microprocessor executes the INTO (Interrupt on Overflow) instruction.

. Reserved interrupts (INT 5.....INT 31):

1. These levels are reserved by Intel to be used in higher processors like 80386, Pentium etc. They are not available to the user.

Available interrupts (INT 32.....INT 225):

- 1. These are user defined, software interrupts.
- 2. ISRs for these interrupts are written by the users to service various user defined conditions.

Hardware Interrupts:

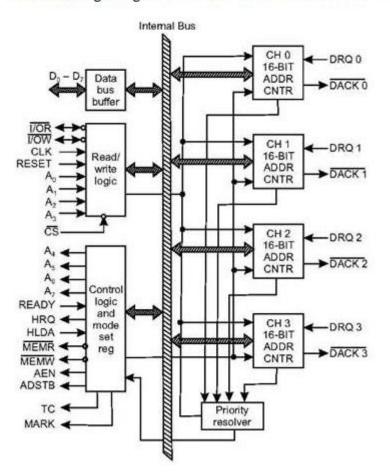
- 1. NMI (Non mask-able interrupt)
 - o This is a non-mask-able, edge triggered, high priority interrupt.
 - o On receiving an interrupt on NMI line, the microprocessor executes INT

INTR-

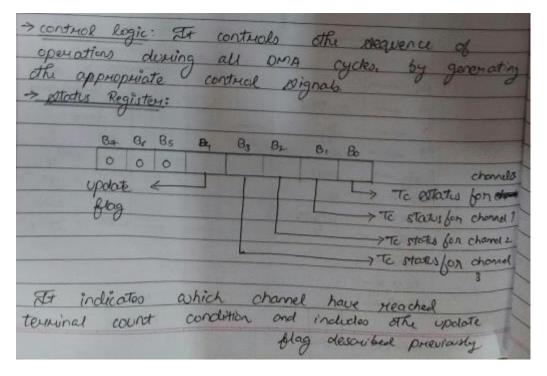
- This is a mask-able, level triggered, low priority interrupt.
- On receiving an interrupt on INTR line, the microprocessor executes 2 INTA——INTA pulses.
- 1st INTA——INTA pulse The interrupting device calculates (prepares to send) the vector number.
 - 2nd INTA——INTA pulse The interrupting device sends the vector number 'N' to the microprocessor.

8257 Architecture

The following image shows the architecture of 8257 -



→ Data bus Bullen: It is a thi-extate, bi-directional, eight bit bullen which interfaces offer #2 8257 to the system data bus. It is used to transfer data between you and internal negister of 8257. → Read/write Lagic: when other CRU is programming on meading one of the internal negisters of 8257 pin diagram, the Read/write accepts othe I/o Read on I/o write Dignal, decodes the least significant four addies bit and either writes othe contents of the data bus into othe addressed negister om places othe contents of the addressed negister on places othe data bus



-> Priority Resolven: It mesolves the previphenals

Hegrest at can be programmed to work in two

modes either in fixed mode on notating priority

mode

DRQ₀-DRQ**3**

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ_0 has the highest priority and DRQ_3 has the lowest priority among them.

DACK_o - DACK₃

the requesting peripheral about the status of their request by the CPU.

$$D_{o}-D_{7}$$

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

$A_0 - A_3$

These are the four least significant address lines.

CS

It is an active-low chip select line.

$A_4 - A_7$

These are the higher nibble of the lower byte address generated by DMA in the master mode.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRO

This signal is used to receive the hold request signal from the output device.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to 1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADST

This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for 'Terminal Count', which indicates the present DMA cycle to the present peripheral devices.

MARK

It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

DMA apperation perforated:
> The 8086 MICHOPHOCESSON MECEIVED bus meguests
through its he HOLD pin and issues greats from
othe hold acknowledge (HLDA) pin.
-> A neguest is made when a potential master
wends a 2 to the HOLD pin
> Nounally, after the connect bus cycle is complete the 8086 will nespond by putting a 2
complete the 8086 will respond by putting a 1
on the HILDA pin . When the Hequesting device
necess this great signal it becomes the morter.
7 It will Hemain master until it drops the
signal to the HOLD pin, at which time the
8886 will deep the quant on the HIDA pin.

(3)	esting Explain what is branch puediction logic
	in Pentium? Explain woulding of Branch puediction
1 31	with socitable example?
9	
Ans:	- why do we need buanch puediction?
	I The gain precduced by Pipelining can be to
1 250	I The gain produced by Pipelining can be fine Heduced by the presence of perogram transfer
	2. They change the exequence causing all the
	instruction othat entered the Bipeline often
1000	Program othersper instructions invalid
	3 This no work is done as the pipeline
	stages are related reloaded
150	
	To avoid othis problem, Pertilu uses a
1000	exchene called Dynamic branch mediction. In
- 100	and scheme, a prediction is mad. you have
100	THE COMMENTER IN THE PLANTING THE
-00	phillippin will either be token an not token
	THE DAY OF THE PARTY OF THE PAR
	aill not be flushed and no clock cycles will
	of the prediction is folse other the
	piperine will be flushed and estants over with
	be lost of the prediction is folse other only pipeline will be flushed and starts over with the current instruction.
	working of Branch prediction:
	TO BTB is a situation Contract
	with to othe wide of Decode instruction (DI)
	stage of two pipelines and instruction (DI)
	stage of two pipelines and monitors for buanch instruction.

The first time the beauth instruction enters other pipeline, the BTB USES HS BOUNCE MOMONY to penjourn a lookup in the cache -> since the instruction was never seen before it is BTB Miss. The predicts affect offer is unconditional gurp instruction. other other instruction reaches the EU, other branch will be either otaken on not taken. of taken, the next instruction to be executed will be fetched from the branch target address. I not taken, othere will be stagest organital fetch of instruction I when the bound is taken for the first time, the execution unit provides feedback to the breach prediction. The branch target address target address is ment back which is recorded in BTB A directory entry is made containing other some memory address and history bit & is set as sitrongly taken.

Movement when branch is not taken (WT) Weakly Not Taken (WT) Not Taken (SNT)

Movement when branch is taken

(103)Fig. 11.5.2: History bits

The history bits can indicate one of four possible states.

History Bits	Resulting Description	Prediction made	if actually taken	if actually not taken				
00	Strongly Not Taken	Branch Will Not Be Taken	Upgrades to Weakly Not Taken	Remains Strongly Not Taken				
01	Weakly Not Taken	Branch Will Not Be Taken	Upgrades to Weakly Taken	Downgrades to Strongly Not Taken				
10	Weakly Taken	Branch Will Be Taken	Upgrades to Strongly Taken	Downgrades to Weakly Not Taken				
11	Strongly Taken	Branch Will Be Taken	Remains Strongly Taken	Downgrades to Weakly Taken				

Q.4 Compare the 8086, 80386, Pentium Processor.

Product	8086	80386 1985				
Year introduced	1978					
Technology	NMOS	CMOS				
Clock rate (MHz)	3 - 10	16 - 33				
Number of pins	40	132				
Number of transistors	29,000	275,000				
Physical memory	1M	4G				
Virtual memory	None	64T				
Internal data bus	16	32				
External data bus	16	32				
Address bus	20	32				
Data type (bits)	8.16	8. 16. 32				

Pentium
1992
BICMOS
60, 66
273
3.1 million
4G
64T
32
64
32
8. 16. 32

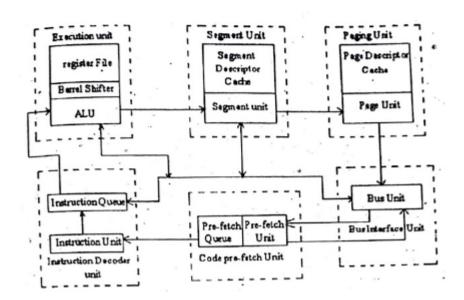
Draw and explain the internal architecture of 80386 microprocessor.

▲ MMRCSE ② 12/07/2018 04:38:00 PM 🔸 2

The internal architecture of the 80386 inch1des six functional units that operate in parallel. The parallel operation is called as pipeline processing. Moreover, Fetching, decoding execution, memory management, and bus access, for several instructions are performed simultaneously.

Also, the six functional units of the 80386 Architecture are

- · Bus Interface Unit
- · Code Pre-fetch Unit
- · Instruction Decoder Unit
- · Execution Unit
- · Segmentation Unit
- · Paging Unit



The Bus Interface Unit connects the 80386 with memory and I/O. Based on internal requests for fetching instructions and transferring data from the code pre-fetch unit, the 80386 Architecture generates the address, data and control signals for the current bus cycles.

Also, The code pre-fetch unit pre-fetches instructions when-the bus interface unit is not executing the bus cycles. It then stores them in a 16-byte instruction queue for decoding by the instruction decode unit.

Moreover, The instruction decode unit translates instructions from the prefetch queue into microcode. The decoded instructions then stored in an instruction queue (FIFO) for processing by the execution unit.

The execution unit processes the instructions from die instruction queue. It contains a control unit a data unit and a protection test unit.

The control unit contains microcode and parallel hardware for fast multiply, divide, and effective address calculation. The unit includes a 32-bit ALU, 8 general purpose registers and a 64-bit barrel shifter for performing multiple bit shifts in one clock. The data unit carries out data operations requested by the control unit.

Moreover, The protection test unit checks for segmentation violations under the control of microcode.

Also, The segmentation unit calculates and translates the logical address into linear addresses at the request of the execution unit.

The translated linear address sent to the paging unit. Upon enabling the paging mechanism, the 80386 translates these linear addresses into Physical addresses.

Also if paging not enabled, the physical address is identical to the linear address and no translation is necessary.

(8) Explain the operating modes at 90386? openating The processing made of the 80386 has three processing modes 1) Real-Address made is power on default made The tral nedvers made, 80396 acts as a Version OF 9086 which is fuster than original gold as solds operated on higher clock frequency Til) It offers memory addressability of IMB OF physical memory iv) segmented addressing : Total 6 segments 3) Protected Mode 1) It is the natural 32-bit envisonment at the \$0386 Processor II) In this mode all instructions and teamtures are available. iti) segment size & 1 to kink TO IF GOSAS IS WORKING IN Addressed Made I't can not Switch to Year Mode unless of the 801et 3) Vistual 1086 Made F) 486 made at berrund 8056 mode also conted as US6 made. It PS a dynamic in the sense that the processor can switch beleatedly and rappaly blw

mode to execute an 8086 program, then leaves

VEG mode and entery protected mode to

continue executing a native 80386 program.

iii) The reatures that are available to

applications programs in protected mode and

to all programs in VEG made continue

Same.

(7)	Explain internal auchitecture of 8086 typ ? Differentian
	the funtioning of Minimum mode and maximum modes
- 50	0 0
Ans:-	-> The auchitecture of 8086 provides a number of
	improvements over 8685 sp architecture
	> It supports 16-bit ALV, a met of 16-bit negisters,
	a mich Protocotion set, powerful intersept structure
	Letched instruction queve-
	4 The 8086 asschitecture is divided into two
-	parts (a) Bus Thterface Unit (BIU) and (b) Execution
	unit
	(D) Bus Interface unit (BIU):
	Is provides the interface of 80% to external
	performer various mothine cycles such as memory
	Head, I/O weed at to transfer data between
	MUNDEY WA TO DEVICES.
	BIV mainly contains 4 pregnent megisters instruction
-	pointer, prefetch quere and an address generation
	CHEWIT
_	The four segment negisters are,
	Code pregnent (CS) Data pregnent (OS)
	potack Begment (SS)
	EXTHO BEGHANT (ES)
	(B) Execution Unit (EU): The Main components of EU
	are General purpose register, the ALV, special purpose
	negister, Instruction negleter, and decoder, and flag
	Liegisteus.

There are 16 general purpose registers:
THE LIGHTION
It holds operands and most during multiplication
It holds operands and movet during multiplication and division operation. Place an accumulation during
string operation
-> BX Hegisten.
Holds memory address in indirect addressing
Mode
> CX megisten
The holds count for instruction like leop, notate,
whilt and setting opportunion
→ OX Megisten
Fit is used with Ax to hold 32 bit value
during multiplication and division
se especial purpose negistero
+ sotack pointer
-> Base pointer.
→ plounia index
-> Destination indu
a flago unglistore Flag neglisten consist of a flago.
a company to the contract of t
6 potatus flogo: 3 contince flogo
canny flaz ((4) Thap flag (TF) Frantly flag (OF) interrupt flag (TF)
Zeyo Glag (ZF) Dign Glag (S)
overflow biag (0)
1)

Minimum mode	Maximum mode
In minimum mode there can be only one processor i.e. 8086.	In maximum mode there can be multiple processors with 8086, like 8087 and 8089.
$\overline{MN}/\overline{MX}$ is 1 to indicate minimum mode.	MN/\overline{MX} is 0 to indicate maximum mode.
ALE for the latch is given by 8086 as it is the only processor in the circuit.	ALE for the latch is given by 8288 bus controller as there can be multiple processors in the circuit.
\overline{DEN} and DT/\overline{R} for the trans-receivers are given by 8086 itself.	and DT/\overline{R} for the trans-receivers are given by 8288 bus controller.
Direct control signals $M/\overline{IO}, \overline{RD}$ and \overline{WR} are given by 8086.	Instead of control signals, each processor generates status signals called $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$.
Control signals $M/\overline{IO},\overline{RD}$ and \overline{WR} are decoded by a 3:8 decoder like 74138.	Status signals $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$ are decoded by a bus controller like 8288 to produce control signals.
\overline{INTA} is given by 8086 in response to an interrupt on INTR line.	\overline{INTA} is given by 8288 bus controller in response to an interrupt on INTR line.
HOLD and HLDA signals are used for bus request with a DMA controller like 8237.	$\overline{RQ}/\overline{GT}$,lines are used for bus requests by other processors like 8087 or 8089.
The circuit is simpler.	The circuit is more complex.
Multiprocessing cannot be performed hence performance is lower.	As multiprocessing can be performed, it can give very high performance.

Sol ex	Input data -> Menciny address -> Cutput ox Menony add	10 by orenen in anny 1 04 20 2050 2051	evenents of annuy 1 A 55 2B 2052 8053 2054									
SOF. EXI	Input data -> Menciny address -> Cutput ox Menony add	no of otenen in corn-y 1 04 20 2050 2051	elements of annuay 1 A 55 2B 2052 8052 2054									
SOL: ex	Triput data -> I Menchy address -> Cutput ox Menony adal	00 Bl olement in corn-y 1 04 20 \$050 2051	1A 55 2B 2052 8052 2054									
	Input data -> Menchy address -> Cutput add	10 d 20 04 20 2050 2051 1	1A 55 2B 2052 8052 2054									
	Input data -> Menchy address -> Cutput add	10 d 20 04 20 2050 2051 1	1A 55 2B 2052 8052 2054									
ДН	Input data > Menchy address > Cutput ox Menony add	04 20 2050 2051 \ uta → 55	2052 8068 2054									
Он	nenchy addres of cutput oc menony add	2050 2051 \	amaia da de									
VR	Cutput OC Methony add	uta → 55	e laugest element									
рн	menony add	The second secon	e laugest elevens									
на	menony add	The second secon										
Он	-											
DH	ognan:											
7	0											
	DHOGHAM											
	memory address	MARHONICS	COMMENT									
	2000	LXT H ,2050	H + 20, L + 50									
	2003	mou cim	C←M C←C-01 HL← HL+0001									
	2004	DER C										
	₹005	TAX H										
	5000	MOU A, M	AEM									
	2007	TAX H										
constant of	2008	CMP M	HL € HL+0001									
	2009	JAK 2000	A-M Ta carring those of go to 2000									
1240	2006	MOV AM	90 to 2000									
	2000	DCR C	C+ C-1									
505	₹00€	JM 7 8007	To zero blog = 0, 900									
133 10 11	2011	STA 3050										
The said	2014	HLT	A → 3050									

Q. 2: Interface 32 K word of memory to the 8086 microprocessor system. Available memory chips are 16 K x 8 RAM. Use suitable decoder for generating chip select logic.

Step_1: Total memory = 32 K word = 32*2 K = 64 K
IC available = 16 K
hence,
number of RAM IC required = 64 K x 8/16 Kx8 = 4 ICs

EVEV Bank = 2 ICs of 16 Kx8 RAM

ODD Bank = 2 ICs of 16 Kx8 RAM

Even bank	Odd bank
RAM_1 (16K)	RAM _2 (16K)
RAM_3 (16K)	RAM_4 (16K)

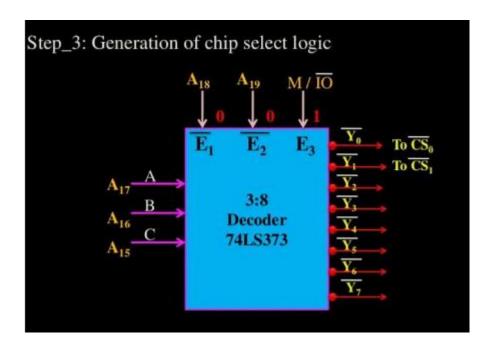
Step_2: Number of address lines required = 15 address lines

To decoder

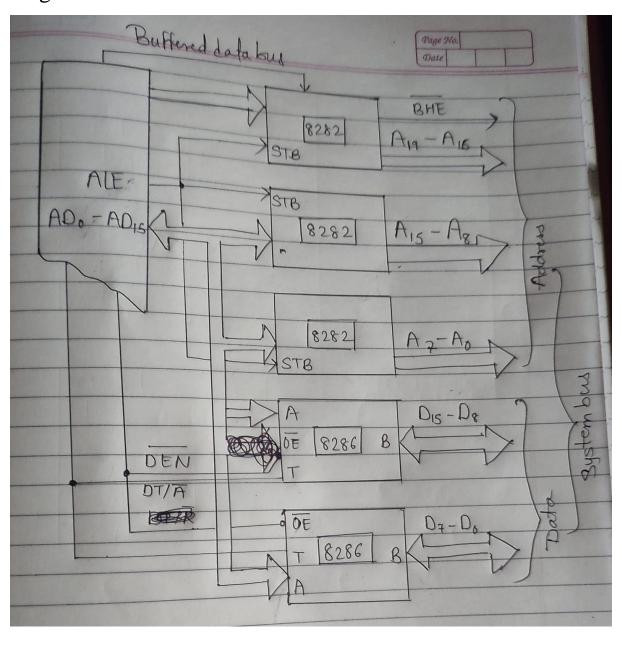
Step_3: Address decoding table

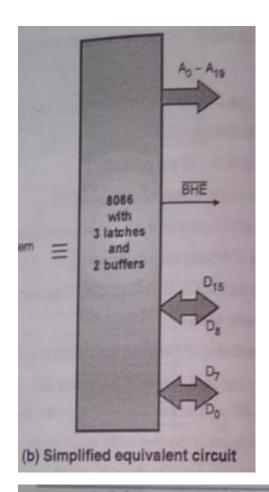
MEMORY IC	HEX ADDRESS						Bl	[N	AR	Y	ΑI	DD	R	ES	S						
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	An	A ₁₂	An	A ₁₀	A ₀	As	A ₇	A ₆	A ₅	A4	A ₃	A	Aı	A
16 K x 8 RAM-(1)	00000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FFE	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16 K x 8	8000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RAM-(3)	0FFFE	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

To 16 K IC



Explain address and data bus demultiplexing in 8086 with diagram.





We have discussed the use of 8282 latches address latching and 8286 as data bus buffer. If we use them simultaneously then we can demultiplex the address data bus as shown in Fig. 3.4.3(a). Thus we require three octal latch chips (8282) and two octal transceiver chips (8286) in order to completely demultiplex the address and data bus. The basic diagram of Fig. 3.4.3 is often required in the memory interfacing and I/O interfacing.

The simplified equivalent of Fig. 3.4.3(a) is shown in

Fig. 3.4.3(b).

(11)	Discuss need for Hencing banking in 8086
Anci-	-> The 8086 processor provides a 16-64 data
-	bus do it is capable of transferring 16 bit
	on cycle but each memory location is
	of a syle, Therefore are need two
	cycles to aces 16 bits from two different
	Mency locations. The polition to this problem
	The Memory banking
	parts (banks). One of the banks contains even
2555	addresses called Even bank and other contains
100	odd addresses called odd bank. Even bank
	always gives lower byte so even bank is
	called lower bank and opp bank to called
	Highen bank.
	aligned memory exaction from both banks simultan
	early and process 10-bit data transfer
	menony banking doesn't make it compulsioner
	to transfer 16-bit, it facilitates the 16-bit
	acus manifes
	-> The choice between 8-bit and 16-bit transfer
	depends on othe instructions given by othe
	рноднаммого.

dol: Mode-0: Atto This node is also known as bask the red This rode is also known as bask the red This rode is also known as bask the red To this rode provides simple input and atput applicing using sach of the others point. Data can be stimply need from and existen to input and output point respectivity, after neglicist featuring of this needs (i) taxe soft parts (part a and part a) and two 4-bit points (part a green and locus) are crailable. (ii) any point can be used as an injury con culput point. (iii) output points are lathed. Thout point are not latched. (iv) a reximum of four points are available as other overall is the configurations are pointly. Mode-2: This made of speciation of 5255 is also known as streeted bidinectional the nodificated device on an 5-bit data bus. The rede of operation provided 5255 with an additional feature for communicating with an pumphered device on an 5-bit data bus. The interpupt generation and other functions are sumilar to nacle a The interpupt generation and other functions are sumilar to nacle a Thus, in this rach and receiver. The interpupt generation and other functions are sumilar to nacle a Thus from with handstock signals. The solid service as an input cost on cutput point Balliert feature The solid service as an input cost on cutput point Balliert feature The solid service are available at point (vie sex-Ple Those the latine are available at point (vie sex-Ple Those and outputs are both lathered	(12)	end to the same of
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Explain interrupt procedure of 8086

Interrupt is the method of creating a temporary halt during program execution and allows peripheral devices to access the microprocessor. The microprocessor responds to that interrupt with an **ISR** (Interrupt Service Routine), which is a short program to instruct the microprocessor on how to handle the interrupt.

Hardware Interrupts

Hardware interrupt is caused by any peripheral device by sending a signal through a specified pin to the microprocessor.

The 8086 has two hardware interrupt pins, i.e. NMI and INTR. NMI is a non-maskable interrupt and INTR is a maskable interrupt having lower priority. One more interrupt pin associated is INTA called interrupt acknowledge.

NMI

When this interrupt is activated, these actions take place –

- Completes the current instruction that is in progress.
- Pushes the Flag register values on to the stack.
- Pushes the CS (code segment) value and IP (instruction pointer) value of the return address on to the stack.
- IP is loaded from the contents of the word location 00008H.
- CS is loaded from the contents of the next word location 0000AH.
- Interrupt flag and trap flag are reset to 0.

INTR

These actions are taken by the microprocessor –

- First completes the current instruction.
- Activates INTA output and receives the interrupt type, say X.
- Flag register value, CS value of the return address and IP value of the return address are pushed on to the stack.
- IP value is loaded from the contents of word location $X \times 4$
- CS is loaded from the contents of the next word location.
- Interrupt flag and trap flag is reset to 0

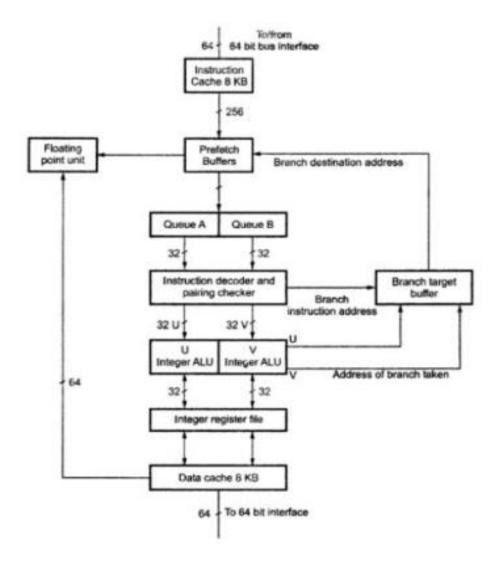
Its execution includes the following steps -

- Flag register value is pushed on to the stack.
- CS value of the return address and IP value of the return address are pushed on to the stack.
- IP is loaded from the contents of the word location 'type number' × 4
- CS is loaded from the contents of the next word location.
- Interrupt Flag and Trap Flag are reset to 0

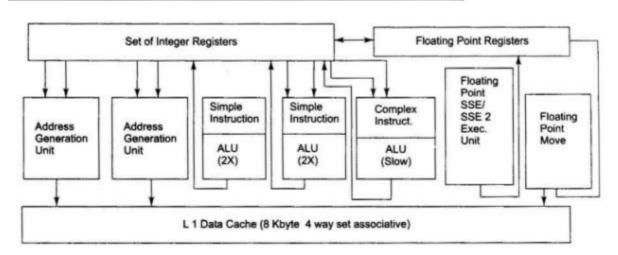
Explain integer pipeline of Pentium

Pentium uses a 5 stage pipeline with the following stages in the pipeline.

- 1.Prefetch stage Pentium instructions are variable length and are stored in a prefetch buffer. There is a 256 bit path from instruction cache to the prefetch buffer.
- 2.Decode 1 stage In this stage the processor decodes the instruction and finds the opcode and addressing information, check which instructions can be paired for simultaneous execution and participates in branch address prediction.
- 3.Decode 2 stage Addresses for memory reference are found in this stage.
- 4. Execute stage Data cache fetch or ALU or FPU operation is carried out. Two operations can be carried out at this stage.
- 5. Write back stage In this stage the registers and flags are updated on the basis of the results of execution.



(15)	white a note on Hyperthreading
Ans:	> thyperthreading used the concept of simultaneous multithreading and schools on improvement in the states microauchitecture development.
1	-> The major elegance of other auchitecture lies in devising appropriate mesource exhausing policy for
	each shared mesource several electrice sharing strategies have been investigated by the develope some of these are (a) partitioned mesources (b)
	of showing esthategy to be adopted depends on several factors, such as other traffic pattern,
	puopabilities and other considerations. To do other, other is one copy of the
	anchi testuru sotate for each logical proccessor, and othe logical proccusion stare a single set of physical execution repartees From a software
123	ou withtecture perspective, other means operating
	on conventioal physical processors as other and
	processor system From a micho anchitecture peuspective, othis mean othat instructions from sogical processors will pensist and execute
	Directoresurly on schooled execution resources



```
Program 3.5
A program to find out the number of even and odd numbers from a given series of 16-bit hex
Solution The simplest logic to decide whether a binary number is even or odd. is to ch
least significant bit of the number. If the bit is zero, the number is even, otherwise it is odd. Che
the LSB by rotating the number through carry flag, and increment even or odd number counter
        ASSUME CS:CODE. DS:DATA
        DATA SEGMENT
LIST DW 2357H, 0A579H, 0C322H, 0C91EH, 0C000H, 0957H
COUNT EDU 0D6H
        DATA ENDS
        CODE SEGMENT
        START:
                        XOR BX. BX
                        XOR DX. DX
                         MDV AX, DATA
                        MOV DS. AX
                        MOV CL. COUNT
MOV SI, OFFSET LIST
                        MOV AX. [SI]
ROR AX. DI
        AGAIN:
                         INC BX
                         JMP NEXT
                         INC DX
        NEXT:
                        ADD 51, 02
                         JNZ AGAIN
                         MOV AH. 4CH
                         INT 21H
                         CODE ENDS
                         END START
                                   Program 3.5 Listings
```

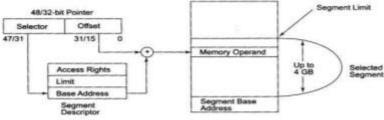
Q18.

80386: Protected Mode

All the capabilities of 80386 are available for utilization in its protected mode of operation. In this mode, the 80386 can address 4 Gigabytes of physical memory and 64 terrabytes of virtual memory per task. The 80386 in the protected mode supports all softwares written for 80286 and 8086 to be executed under the control of memory management and protection abilities of 80386. The protected mode allows the use of additional instructions, addressing modes and capabilities of 80386.

Addressing in Protected Mode 80386 support two methods a) Paging disabled b) Paging enabled

In this mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment. The effective address (offset) is added with segment base address to calculate linear address. This linear address is further used as physical address, if the paging unit is disabled. Otherwise, the paging unit converts the linear address into physical address.

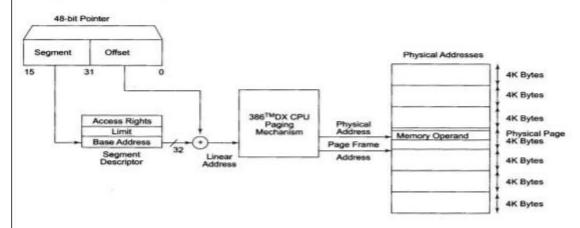


Protected Mode Addressing without Paging Unit (Intel Crop.)

80386: Protected Mode

b) Paging Enabled

The paging unit is a memory management unit enabled only in the protected mode. The paging mechanism allows handling of large segments of memory in terms of pages of 4 Kbyte size. The paging unit operates under the control of segmentation unit. The paging unit if enabled converts linear addresses into physical addresses, in protected mode.



Paging Unit Enabled in Protected Mode Addressing (Intel Corp.)

(19)	Explain memory segmentation in some with neat
Pos:	Beginentation is oth puccess in which oth main memory of othe computer is logically divided into different beginents and each degreed has the own base address. It is basically used to enchance othe speed of execution of the computer bystem. so that othe processor is able to fetch and execute othe data from othe memory easily and fast The Bus interface unit (BOS) contains the four 16-bit special pumpose megisters called as segment Registers.
	Registers. -> (ode segment Registers (CS): is used for addressing memory location in web segment of the memory location in web segment of the memory where the executable program is extended. -> Data segment Register (DS): points to the data segment of the memory where the skets is solved. -> Extra - segment Register (ES): also exfens to the segment in the memory which is another data segment in the memory which is another data segment in the memory which is another data segment in the segment of the memory addressing stack segment of the memory addressing stack segment of the memory.

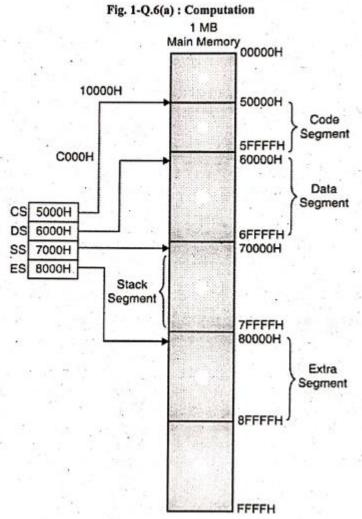
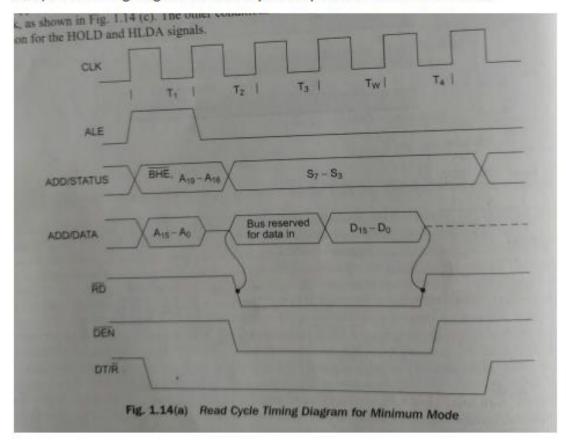


Fig. 2-Q. 6(a) : Segments in 8086

Q20) Draw timing diagram of memory read operation in minimum mode.



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		0	4	0	0	- 80

In the programing nodel others one: - 4 general purpose neglitous - 4 organist westerns - 2 pointer negisters - 2 Trodex neglitars - 2 instruction pointies sugirter - 1 flag megister -> General purpose megisters (2) Ax register: This is accomplation to its is used in another; legic and data triangler trictivetiens (6) 8x negistor It is a base register. It is usually continue data pointers used for band, band indone of projection indirect addresing (3) ex megisters: This is count megisten Purguent loop constructions are facilitated by it. post number in 1/0 operations. -> Degment megistern (3) aide Organis FIF PI used for addressing a warray leaster in the ade segment of the menony a) Data suggest: It points to the data object of the (3) sotech Degrent to is used for addressing others organic of the newly to so another refers to it the Beynest which essentially to another data pregnent of othe monory

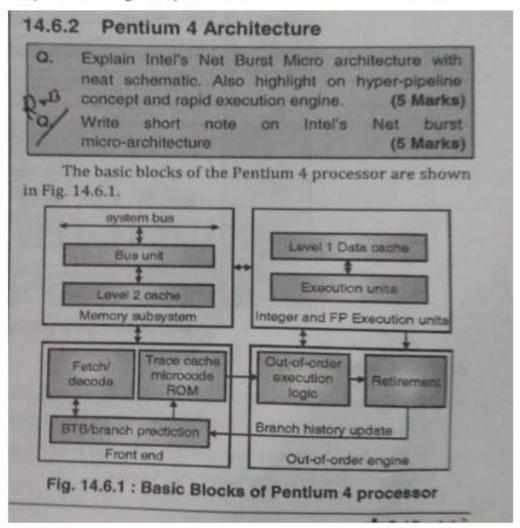
> Pointen negisters (2) SP Register: This is stack pointed register pointing . рисдиан власк (6) Br Register: This is Base pointen exegition pointing + data in sotale pregnent - Inder Registers: (2) ST Register (Mounce Andre): This is used to point , Memory Locations in the data suggest addressed by (2) DI Register (Destination students This megister performs the Name function as ST There is a obsi of instructcalled 19thing instruction that UK DI to access the Merony locations activismed by Es. -> Instruction pointer The Instruction pointer points to the post address of the next instruction to be executed -> Flag ingister. The sens flag register contents include the result of computation in the PLU

Q.22 Explain BSR mode of 8255.

The **BSR mode** stands for "**Bit Set Reset Mode**". The first bit, i.e. the Most Significant Bit (MSB) of the Control word decides the mode in which the 8255 IC will be. For the IC to be in the BSR mode, the MSB must be reset, i.e. it must be 0. The BSR mode works only for port C. In this mode, we can select any bit of the port C and then assign it any value: either 0 or 1.

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Sar Be			82 B	6, 8 ₀		
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7			1 1	1 1 0-Reset		
0	Box mode		Bi+ dela	ect flag 2 - set		

Q.23 Same as Q.3



The basic blocks of Pentium 4, as shown in Fig. 14-5.3, consists of Mamory subsystem. Front and Dut-of-order Engine and the integer and Florting point execution units.

1. Memory Subsystem

- This unit bandles the memory accesses and also commute of the L2 cache.
- The L2 cache is an Advanced Trace Cache as discussed in the features of the processor.

2. Front End

 This block cunstits of a Fesch / Decode unit. Trace cache along with microcode ROM and BTB along with branch prediction logic.

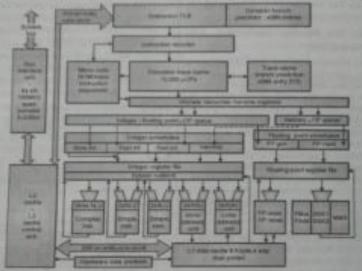
- The firtch decode unit letches the instructions and decodes them.
- The trace cache, as discussed already, stores the decoded instructions and hence reduces the time for decoding in loops.
- The branch prediction logic predicts the sequence of matricitions during a branch instruction with the help of branch history stored in Branch Turget Buffer (BTE).

3. Out-of-order Engine

- The out-of-order engine executes the instructions outof order in case of their dependencies and hence keeps the execution units continuously busy.
- But the retirement of the instructions are in order.

4. Execution units

There are imager execution staffs to concurs images instructions. Starting profit must be Shorting point statement and MNN unit to execute 1980 years investigation. The detailed bit-in diagram of Fernium 4 to shown in Fig. 14.6.2.



Pig. 14.6.2 : Detailed Block Diagram of Pentium 4

[4] AdvancedL2Cache

- The L2-cache also called as "Advanced Transfer Cache" is 236 KB (or S12KB or 1 MB) and is 8-very assistation France.
 6's L2-cache uses 128 byte cache lines, which are divided in two 64-byte pieces.
- The L1 data cache was reduced from to only 0 KB, to enable its extremely low latency of only 2 check system and hour
 results in an overall improved read latency.

Q.25 Same as Q.5

Q27) Write an 8086 assembly language program to print content of flag register.

```
mov ax, Data
mov DS, ax
 mov dx,offset msg
mov sh,09h
int 21h
 mov dx.offset newl
mov ah.09h
int 21h
  eli
 atc
atd
 pushf
 pop bx
 mov flag,bx
 mov cx,16
mov bx,8000h
Loops:
 mov ax, flag
and ax, bx
jz zero
mov dl, 31h
mov ah, 02h
int 21h
 jmp space
zero: mow dl,30h
 mov ah, 02h
int 21h
space: mov dl, ' '
mov ah, 02h
int 21h
 mov ah, 02h
int 21h
 ror bx, 1
 loop loops
mov ah, 4ch
int 21h
Code ends
end start
```