addresses allotted to initiate various operations are listed in Table 9.38.

TABLE - 9.38 : ADDRESS ALLOTED TO ADC0809 INTERFACED TO 8031/8051 AS SHOWN IN FIG. 9.96

Operation performed	Decoder Input	Binary address														Hexa address	Comment
		Address input to ADC															
	A_{15} A_{14} A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
SOC channel-0	1 1 0	x	x	x	x	x	x	x	x	x	0	0	0	0		C000	External data memory address space
SOC channel-1	1 1 0	x	x	x	x	x	x	x	x	x	0	0	0	1		C001	
SOC channel-2	1 1 0	x	x	x	x	x	x	x	x	x	0	0	1	0		C002	
SOC channel-3	1 1 0	x	x	x	x	x	x	x	x	x	0	0	1	1		C003	
SOC channel-4	1 1 0	x	x	x	x	x	x	x	x	x	0	1	0	0		C004	
SOC channel-5	1 1 0	x	x	x	x	x	x	x	x	x	0	1	0	1		C005	
SOC channel-6	1 1 0	x	x	x	x	x	x	x	x	x	0	1	1	0		C006	
SOC channel-7	1 1 0	x	x	x	x	x	x	x	x	x	0	1	1	1		C007	
Read EOC	1 0 1	x	x	x	x	x	x	x	x	x	x	x	x	x		A000	
Read ADC output	1 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x		E000	

Note : Don't care "x" is considered as zero.

9.8 SHORT QUESTIONS AND ANSWERS

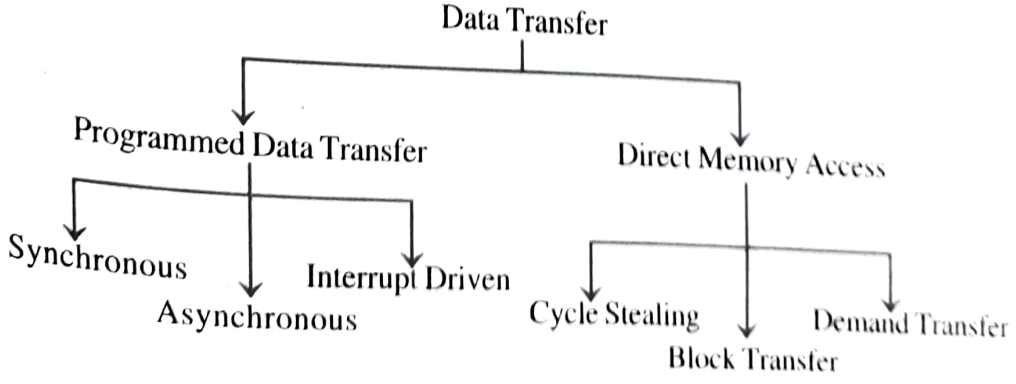
9.1 ***What is a programmable peripheral device?***

If the functions performed by a peripheral device can be altered or changed by a program instruction then the peripheral device is a called programmable device. Usually programmable devices will have control registers. The device can be programmed by sending control word in the prescribed format to the control register.

9.2 ***What is data transfer scheme and what are its types ?***

The data transfer scheme refers to the method of data transfer between the processor and the peripheral devices.

The different types of data transfer schemes are shown below:



9.3 What is a synchronous data transfer scheme?

In synchronous data transfer scheme, the processor does not check the readiness of the device after a command have been issued for read/write operation. In this scheme, the processor will request the device to get ready and then read/write to the device immediately after the request. In some synchronous schemes a small delay is allowed after the request.

9.4 What is an asynchronous data transfer scheme ?

In asynchronous data transfer scheme, first the processor sends a request to the device for read/write operation. Then the processor keeps on polling the status of the device. Once the device is ready, the processor executes a data transfer instruction to complete the process.

9.5 What are the operating modes of an 8212 ?

The 8212 can be hardwired to work either as a latch or tristate buffer. If mode (MD) pin is tied **high**, then it will work as a latch and so it can be used as an output port. If mode (MD) pin is tied **low**, then it work as tristate buffer and so it can be used as an input port.

9.6 What are the various internal devices of INTEL 8155?

The INTEL 8155 is an IC consisting of static RAM, IO ports and a timer. The internal devices of 8155 are 256 bytes of static RAM, three numbers of programmable IO ports and a 14-bit programmable timer.

9.7 What are the internal devices of an 8255 ?

The internal devices of an 8255 are port-A, port-B and port-C. The ports can be programmed for either input or output function in different operating modes.

9.8 What are the operating modes of port-A of an 8255?

The port-A of an 8255 can be programmed to work in any one of the following operating modes as input or output port:

Mode-0 : Simple IO port

Mode-1 : Handshake IO port

Mode-2 : Bidirectional IO port

9.9 What are the functions performed by port-C of an 8255?

1. The port-C pins are used for handshake signals.
2. Port-C can be used as an 8-bit parallel IO port in mode-0.
3. It can be used as two numbers of 4-bit parallel port in mode-0.
4. The individual pins of port-C can be set or reset for various control applications.

9.10 What is a handshake port ?

In a handshake port, signals are exchanged between the IO device and the port or between the port and the processor for checking/informing various condition of the device.

9.11 Explain the working of a handshake input port.

In handshake input operation, the input device will check whether the port is empty or not. If the port is empty, then it will load the data to the port. When the port receives the data, it will inform the processor for read operation. Once the data has been read by the processor, the port will signal the input device that it is empty. Now the input device can load another data to the port and the above process is repeated.

9.12 Explain the working of a handshake output port.

In handshake output operation, the processor will load a data to the port. When the port receives the data, it will inform the output device to collect the data. Once the output device accepts the data, the port will inform the processor that it is empty. Now the processor can load another data to the port and the above process is repeated.

9.13 How is DMA initiated?

When the IO device needs a DMA transfer, it will send a DMA request signal to the DMA controller. The DMA controller in turn send a HOLD request to the processor. When the processor receives a **HOLD request**, it will drive its tristated pins to **high impedance** state at the end of current instruction execution and send an acknowledge signal to the DMA controller. Now the DMA controller will perform DMA transfer.

9.14 What are the different types of DMA?

The different types of DMA data transfer are cycle stealing (or single transfer) DMA, Block transfer (or Burst mode) DMA and Demand transfer DMA.

9.15 What is cycle stealing DMA?

In cycle stealing DMA (or single transfer mode), the DMA controller will perform one DMA transfer in between instruction cycles (i.e, in this mode the execution of one processor instruction and one DMA data transfer will take place alternatively.)

9.16 What is block and demand transfer mode DMA?

In block transfer mode, the DMA controller will transfer a block of data and relieve the bus to processor. After sometime another block of data is transferred by the DMA and so on.

In demand transfer mode, the DMA controller will complete the entire data transfer at a stretch and then relieve the bus to the processor.

9.17 What are the programmable registers of 8237?

The programmable registers of 8237 are Base address registers, Base word count registers, Command register, Request register, Mode registers end Mask register.

9.18 What is the first-last flip-flop?

The 8237 has an internal flip-flop called first-last flip-flop which takes care of reading/writing 16-bit information through 8-data lines.

The first-last flip-flop selects the low or high byte during read/write operation of the address and count registers of channels. If first-last flip-flop is zero (i.e. reset),then the low byte can be read/write. If it is one (i.e., set), then the high byte can be read/write. After every read/write operation the first-last flip-flop automatically toggles.

9.19 What is the bit format used for sending asynchronous serial data?

In asynchronous transmission, each data character has a bit which identifies its start and 1 or 2 bits which identifies its end. A typical bit format is shown in Fig. Q9.19.

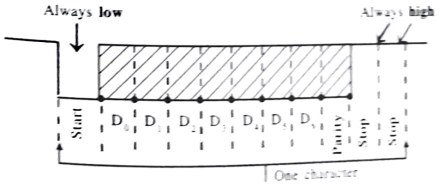


Fig. Q9.19 : Bit format used for sending asynchronous serial data.

9.20 What is baud rate ?

The baud rate is the rate at which the serial data are transmitted. Baud rate is defined as $\frac{1}{\text{(The time for a bit cell)}}$. In some systems one bit cell has one data bit, then the baud rate and bits per second are same.