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DLCOA / Experiment 2

Aim: To design & verify a Half-adder circuit.

Software Used: DLCOA virtual Lab Simulator.

Theory: Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bits (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B.

From this, it is clear that a half adder circuit can be easily constructed using one X-OR gate and one OR gate

Half-adder is the simplest of all circuits but it has a major disadvantage.

So, if the input to a half adder ~~can~~ has a carry, then it will be neglected & adds only the A & B bits

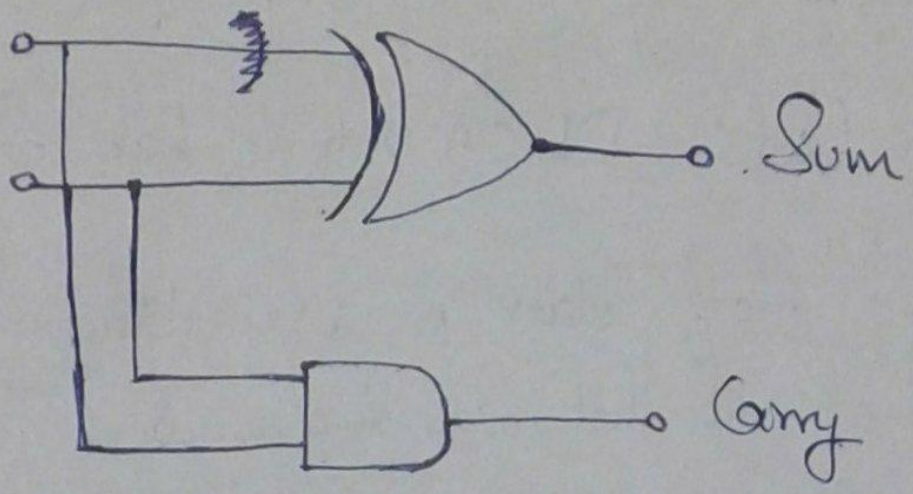
That means the binary addition process, is not complete and thats why it is called a halfadder.

$$\text{Sum } S = A \text{ Xor } B = A\bar{B} + \bar{A}B$$

$$\text{Carry } C = A.B$$

Objective: To design, realize & verify the characteristics of half-adder circuit using basic gates and univ gates.

Conclusion



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Therefore, we have designed and verified the Half-adder circuit using the Virtual lab Simulator.

Carry and Sum of different Inputs in Half Adder: