The 16 kb RAM memory can be implemented by using two numbers of 8 kb RAM 6264. The RAM memories 8255 and 8279 can be interfaced to the 8051 controller as data memory. The 8 kb RAM requires 13 address lines and so the address lines A_0-A_{12} are connected to the address pins of the RAM to select its internal locations. The address lines A_0 and A_1 are connected to 8255 and the address line A_0 is connected to 8279 to select their internal devices.

A 2-to-4 decoder is employed in the system to generate the chip select signals required for RAM, 8255 and 8279. The address lines A_{13} and A_{14} are connected to the input of the decoder to generate four chip select signals. The address line A_{15} is used as logic low chip enable for the decoder.

Since the internal ROM is used in the system, the pin $\overline{EA}$ should be tied to V_{cc} or +5-V. The 8051 provides separate read and write control signals $\overline{RD}$ and $\overline{WR}$ for reading and writing with devices interfaced as data memory. The memory and IO interface diagram is shown in Fig. 51.2. The addresses allotted to the various devices are listed in Table-51.2. The 8051 has separate 256 bytes internal data memory address space allotted to internal RAM and SFR.

6.13 SHORT QUESTIONS AND ANSWERS

6.1 *What is memory ?*

A memory is a storage device in a microprocessor-based system and its primary function is to store programs and data.

6.2 *Why are semiconductor memories used as the main memory in a microprocessor system ?*

The semiconductor memories alone have a processor compatible access time for read and write operations. Therefore, semiconductor memories are used as the main memories.

6.3 *What are the different types of semiconductor memory?*

The different types of semiconductor memory are RAM, PROM, EPROM, static RAM, DRAM and NVROM.

6.4 *List the features of semiconductor memories ?*

1. The semiconductor memories are random access memories.
2. In semiconductor memories, a read operation by the processor will not destroy the stored information.
3. The read and write time of the semiconductor memory are compatible for the microprocessor.

6.5 *What is meant by volatile and non-volatile ?*

If the information stored in the memory is lost when the power supply is switched OFF, then the memory is called volatile.

If the content of memory is preserved even after switching OFF the power supply, then the memory is called non-volatile.

6.6 *List the volatile and non-volatile semiconductor memories.*

The volatile semiconductor memories include the static RAM and DRAM. The non-volatile semiconductor memories are ROM, PROM, EPROM and NVROM.

6.7 *What are the characteristics of ROM memory ?*

1. It is non-volatile memory.
2. The contents of ROM memory can be read by the processor, but it cannot write into it.
3. The ROM memory has the feature of random access.
4. The memory cell has a MOS transistor either with open gate or closed gate.

6.8 *How the ROM memories are classified?*

The ROM memories can be classified into the following three categories based on the method of programming :

1. Custom programmed or Mask programmed ROM
2. Programmable or Field programmable ROM
3. Reprogrammable or Erasable - programmable ROM.

6.9 *List the characteristics of EPROM.*

1. The EPROM is non-volatile.
2. It has random-access feature.
3. The contents of EPROM can be erased by passing UV light and then the device can be programmed.
4. The EPROM is a read only memory and for writing into EPROM, a separate hardware set up is required.

6.10 *Write a short note on the memory cell of EPROM.*

The memory cell of EPROM contains a MOS transistor with isolated gate. The isolated gate is located between the normal control gate and the source/drain region of transistor. The information is stored as a charge or no charge in the floating gate.

6.11 *What is NVRAM?*

The non-volatile read/write memories are called NVRAM. The various types of NVRAMs are flash memory, EEPROM and Shadow RAM.

6.12 *List the features of static RAM?*

1. The static RAMs are read/write memories.
2. They are volatile and have random access feature.
3. The memory cell is a flip-flop constructed using 6 to 8 MOS transistors.

6.13 *What is DRAM ?*

DRAMs are read/write semiconductor memories in which the information is stored in the form of electric charge on the gate to substrate capacitance of a MOS transistor.

6.14 *List the characteristics of DRAM?*

1. DRAMs are volatile and have random access feature.
2. They are read/write memories.
3. The contents of DRAM have to be refreshed periodically using refreshing circuits.
4. The memory cell of DRAM will have 3 to 4 MOS transistor.

6.15 *Compare Static RAM and DRAM?*

Static RAM	DRAM
1. Information is stored as voltage level in a flip-flop.	1. Information is stored as a charge in the gate to substrate capacitance.
2. Six to eight transistors are required to form one memory cell.	2. Three to four transistors are required to form one memory cell.
3. Packing density is low.	3. Packing density is high.
4. Contents of memory need not be refreshed.	4. Contents of the memory has to be refreshed periodically.

6.16 *What is physical memory space?*

The memory locations that are directly addressed by the microprocessor is called physical memory space.

6.17 *What is memory word size?*

The size of data that can be stored in the memory location is called memory word size.

6.18 *What is meant by memory mapping?*

Memory mapping is the process of interfacing memories to a microprocessor and allocating addresses to each memory locations.

6.19 *What is memory access time?*

The memory access time is the time taken by the processor to read or write a memory location. During read operation, it is the time between a valid address on the bus and end of read control signal. During write operation, it is the time between a valid address on the bus and the end of write control signal.

6.20 *What are the factors to be considered while selecting a semiconductor memory for microprocessor system ?*

The following factors are to be considered while selecting a semiconductor memory IC:

- Capacity and organization (Memory word size).
- Timings of various signals.
- Power consumption and bus loading (Current levels).
- Physical dimensions and packaging.
- Cost, reliability and availability.

6.21 *What is bus contention?*

If two devices drive the data bus simultaneously, then it is called bus contention. It may lead to the following undesirable events.

1. Damaging one or both the IC chip.
2. The high current may cause a voltage spike in the supply system leading to data loss.

6.22 *Why is EPROM mapped at the beginning of memory space in an 8085 ?*

When EPROM is mapped at the beginning of memory space, then 0000_H address will be allotted to EPROM. The monitor program can be stored from 0000_H address. Whenever the processor is resetted, the program counter will be cleared (i.e, it will have 0000_H address) and so the monitor program will be executed automatically.

6.23 *Why is EPROM mapped at the end of memory space in an 8086 ?*

The mapping of EPROM at the end of memory space will facilitate automatic execution of the monitor program upon reset. Whenever the processor is resetted, the IP is cleared and CS is initialized with $FFFF_H$, and so after a reset the processor will start executing the instructions from $FFFF0_H$ after a reset. The system designer has to permanently store the monitor/boot program starting from this address, which is possible only if EPROM is mapped at the end of memory space.

6.24 *What is chip select and how is it generated ?*

Chip select is the control signal that has to be asserted TRUE to bring an IC from high impedance state to normal state. Generally, the chip select signals are generated in a system by decoding the unused address lines with the help of decoders.

6.25 *Write the typical control signals involved in EPROM interfacing ?*

The control signals needed for EPROM are chip select and output enable.

6.26 *Write the typical control signals involved in RAM interfacing ?*

The control signals needed for RAM interfacing are chip enable, output enable and write enable.

6.27 *What is the relation between memory capacity and address and data pins of memory IC?*

If a memory IC has "m" data pins and "n" address pins, then the memory IC will have a capacity of $2^n \times m$ bits. When m = 8, the memory capacity is 2^n bytes.

6.28 *How memory space is organized in an 8086?*

In 8086, the one mega-byte (1 Mb) of addressable memory space is divided into two banks: Even (or lower) memory bank and Odd (or upper) memory bank. Each bank will have an addressable space of 512 kb.

6.29 *How are the data lines connected to memory banks in an 8086?*

In an 8086-based system, the lower eight lines of the data bus, D_0 - D_7 are connected to the even bank memory ICs and the upper eight lines of data bus, D_8-D_{15} are connected to the odd bank memory ICs.

6.30 *What are the signals involved in memory bank selection?*

In 8086-based system, the even bank is selected by the address line A_0 and the odd bank is selected by the control signal BHE.

6.31 *What is the available address space in an 8031/8051-based system ?*

The 8031/8051-based system has 64 kb program memory address space, 64 kb external data memory address space and 256 bytes internal data memory address space.

6.32 *How is the program memory organized in an 8051 based system ?*

In an 8051-based system the entire 64 kb program memory can be external or 4 kb is internal and the remaining 60 kb is external. This is decided by the logic level of the signal at $\overline{EA}$ pin. When $\overline{EA}$ pin is tied **high** (+ V_{cc} or 5-V) the first 4 kb of program memory is internal and the remaining 60 kb is external. When $\overline{EA}$ pin is tied **low** (GND or 0-V) the internal ROM is ignored and the entire 64 kb is external.

6.33 *What is programmed IO ?*

If the data transfer between an IO device and the processor is accomplished through an IO port and controlled by a program, then the IO device is called programmed IO.

6.34 *What is interrupt IO?*

If the IO device initiates the data transfer through the interrupt, then the IO is called interrupt driven IO.

6.35 *What is DMA?*

The direct data transfer between an IO device and memory is called DMA.

6.36 *What is the need for ports?*

The IO devices are generally slow devices and their timing characteristics do not match with the processor timings. Hence, the IO devices are connected to the system bus through the ports.

6.37 *What is a port?*

Port is a buffered IC which is used to hold the data transmitted from the microprocessor to the IO device or vice versa.

6.38 *Give some examples of the port devices used in an 8085/8086 microprocessor-based system ?*

The various INTEL IO port devices used in 8085/8086 microprocessor-based system are 8212, 8155, 8156, 8255, 8355 and 8755.

6.39 *Write a short note on INTEL 8255?*

The INTEL 8255 is a IO port device consisting of 3 numbers of 8-bit parallel IO ports. The ports can be programmed to function either as an input port or as an output port in different operating modes. It requires 4 internal addresses and has one logic **low** chip select pin.

6.40 *What are the different methods of interfacing IO devices to 8085 and 8086-based systems ?*

There are two methods of interfacing IO devices to 8085 and 8086-based systems. They are memory mapping of IO devices and standard IO mapping.

6.41 *Draw a simple circuit to decode three control signals $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ and to produce separate read/write control signals for memory and IO devices in 8085-based system.*

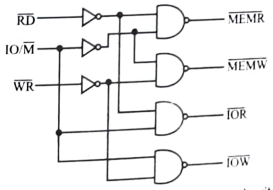

Fig. Q6.41 : Circuit to generate separate read and write signals for memory and IO devices in an 8085-based system.

6.42 ***Compare the memory-mapped IO and standard IO-mapped IO in an 8085-based system.***

Memory-Mapped IO	Standard IO-mapped IO
1. Sixteen bit address is allotted to an IO device.	1. Eight bit address is allotted to an IO device.
2. The devices are accessed by memory read/write cycle.	2. The devices are accessed by IO read/write cycle.
3. All instructions related to memory can be used for data.	3. Only IN and OUT instructions can be used for data transfer.
4. A large number of IO ports can be interfaced.	4. Only 256 ports can be interfaced.

6.43 ***Draw a simple circuit to decode three control signals $\overline{RD}$, $\overline{WR}$ and $M/\overline{IO}$ and to produce separate read/write control signals for memory and IO devices in 8086-based system.***

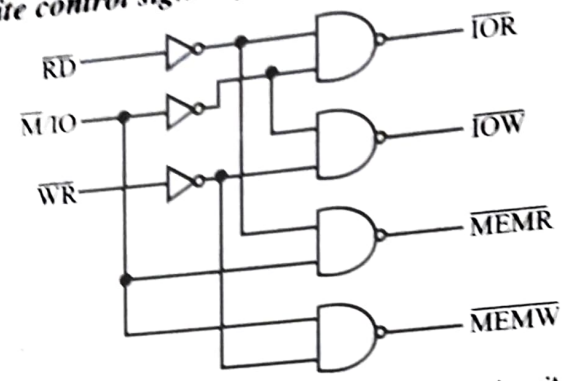

Fig. Q6.43 : Circuit to generate separate read and write signals for memory and IO devices in an 8086-based system.

6.44 ***Compare the memory-mapped IO and standard IO-mapped IO in an 8086-based system.***

Memory mapping of IO device	IO mapping of IO device
1. 20-bit addresses are provided for IO devices.	1. 8-bit or 16-bit addresses are provided for IO devices.
2. The IO ports or peripherals can be treated like memory locations and so all instructions related to memory can be used for data transfer between the IO device and the processor.	2. Only IN and OUT instructions can be used for data transfer between IO device and the processor.
3. In memory-mapped ports, the data can be moved from any register to the ports and vice versa.	3. In IO-mapped ports, the data transfer can take place only between the accumulator and ports.
4. When memory mapping is used for IO devices, the full memory address space cannot be used for addressing memory. Hence memory mapping is useful only for small systems, where the memory requirement is less.	4. When IO mapping is used for IO devices, then the full memory address space can be used for addressing memory. Hence it is suitable for systems which requires large memory capacity.
5. For accessing the memory-mapped devices, the processor executes memory read or write cycle. During this cycle $M/\overline{IO}$ is asserted high.	5. For accessing the IO-mapped devices, the processor executes IO read or write cycle. During this cycle $M/\overline{IO}$ is asserted low.

6.45 ***What is the drawback in memory-mapped IO?***

When IO devices are memory-mapped, some of the addresses are allotted to the IO devices and so the full address space cannot be used for the addressing memory (i.e., physical memory address space will be reduced). Hence memory mapping is useful only for small systems, where the memory requirement is less.