Experiment - 3

YASH SARANG

DGAD - 47

DOP : 29/9/2021

DOS : 5/10/2021

Experiment 3

Aim: Realization of full-adder circuit.

Software used: DLCOA virtual simulator.

Theory: A full-adder is a logic circuit having 3 inputs A, B & C (which is the carry from from the previous stage) and 2 outputs (Sum & carry), which will perform according to table 3. The full-adder can handle three binary digits at a time & can therefore be used to add binary number in general. The simplest way to construct a full adder is to connect two half-adder & an OR gate as shown in figure. The full adder is then the fundamental logic circuit incorporated in digital computers to perform arithmetic functions.

From the truth table, the expressions from sum & carry bits of the output can be obtained as

$$\text{Sum} = A \text{ XOR } B \text{ XOR } C$$

$$\text{Carry} = AB + BC + AC.$$

- Truth table :

Input			Output	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- Design using K-map

Sum

A \ BC	$B'C'$	$B'C$	BC'	BC
A'	0	(1)	0	(1)
A	(1)	0	(1)	0

Sum = A XOR B XOR C.

Carry

A \ BC	$B'C'$	$B'C$	BC'	BC
A'	0	0	1	0
A	0	1	1	1

Carry = $AB + BC + AC$

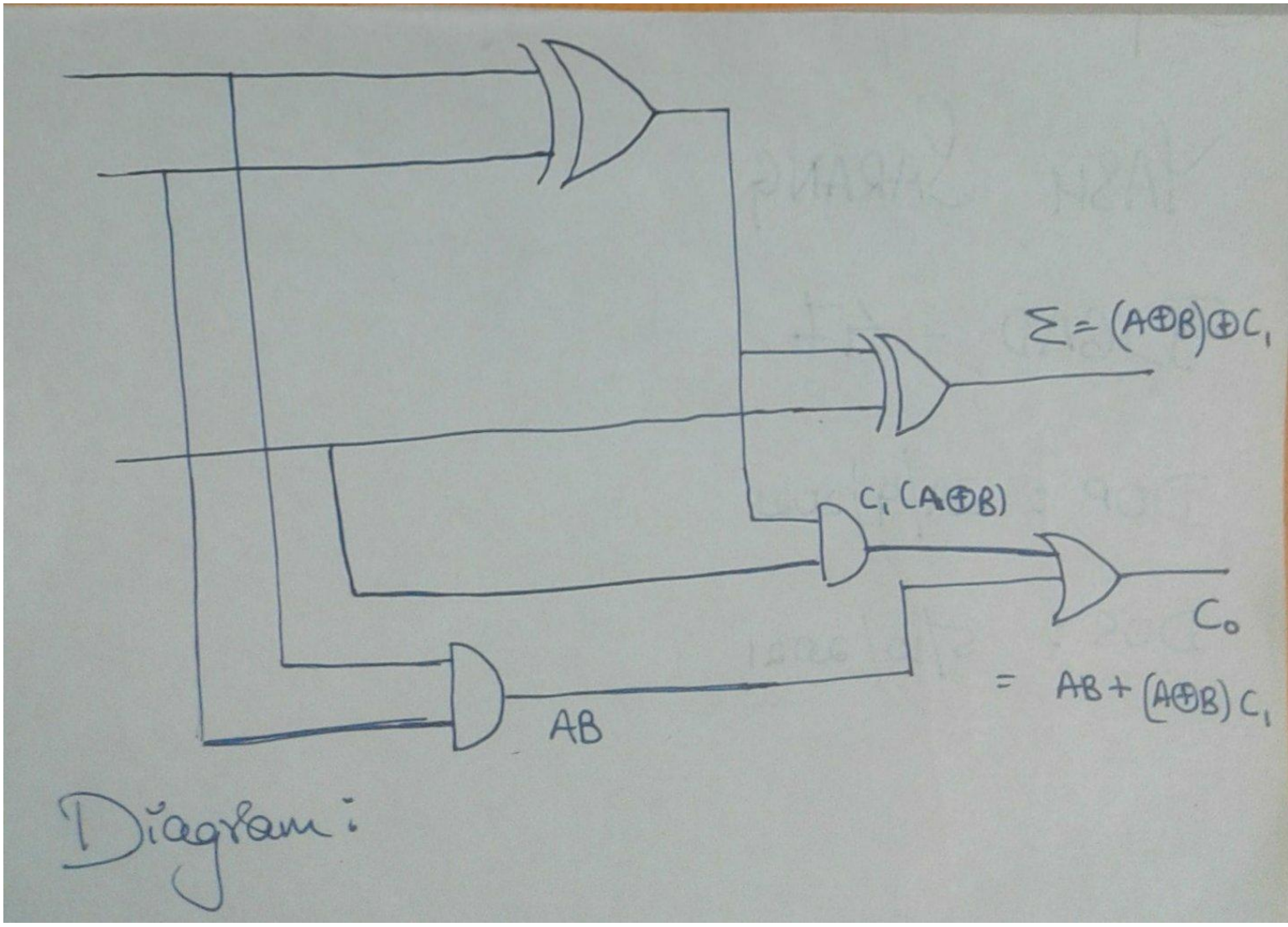
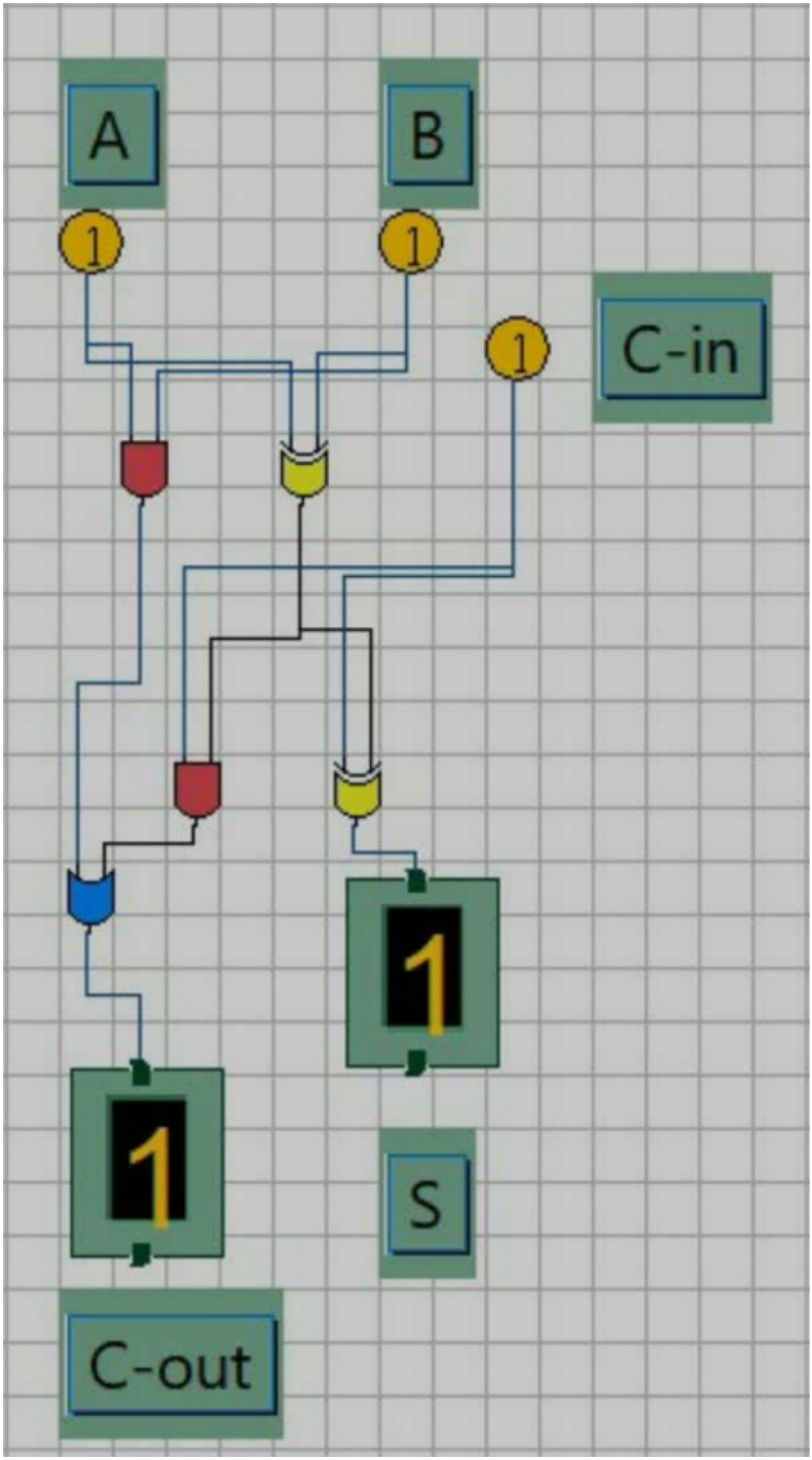
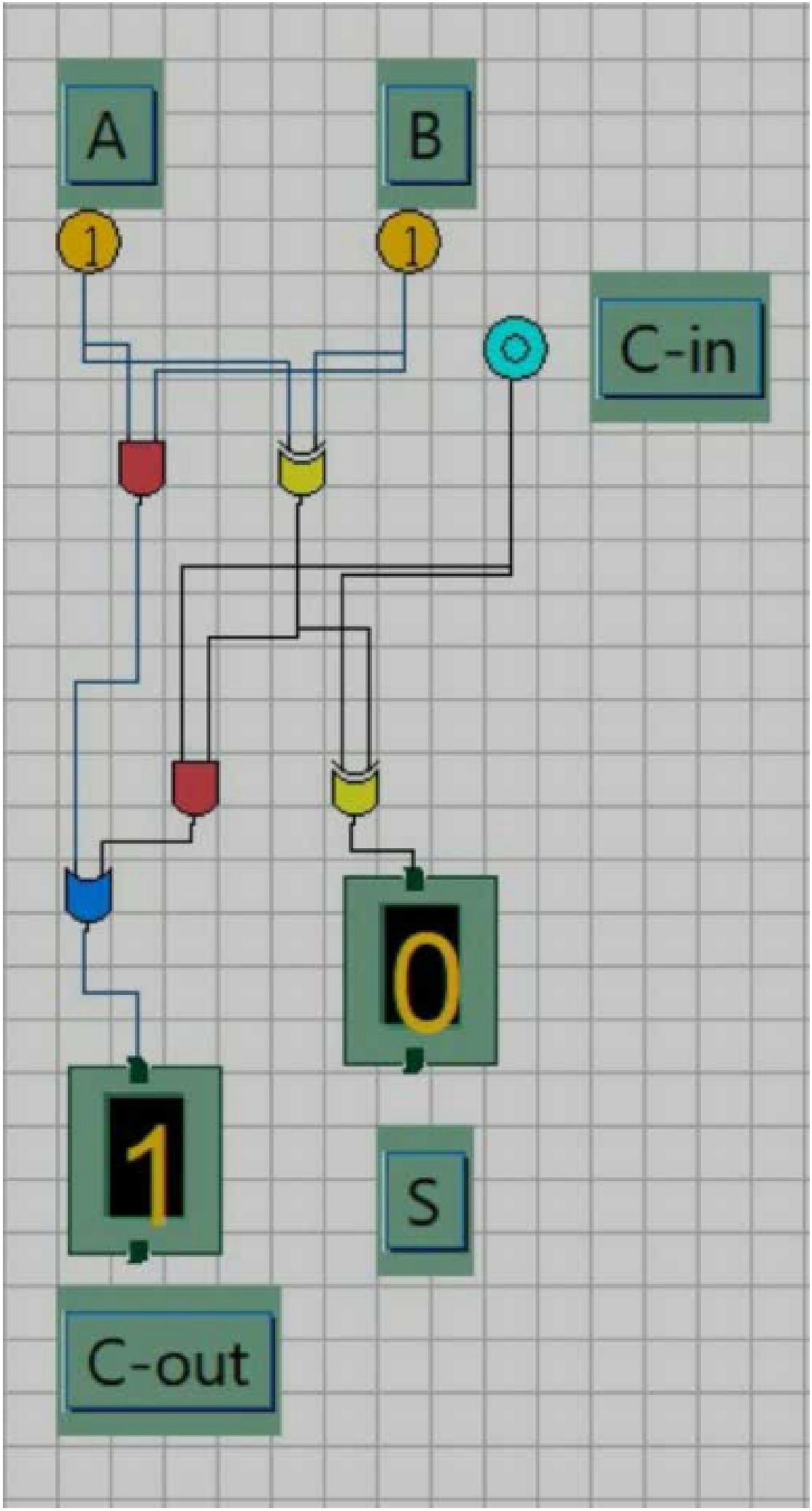


Diagram:

Conclusion: We have successfully constructed and implemented full adder using two half adders and one OR gate.

OUTPUTS :




A
B
1
1
C-in
0
1
S
C-out