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DLCOA / Experiment 7

DLCOA Experiment No. 7

Aim: Synthesis of flip flops.

Software: Virtual lab simulator.

Theory:

Most of the components of digital logic circuit consists of combinational circuits, but they are likely to have memory elements too. Those types of circuits are known as sequential circuits.

In a sequential circuit, the present output is not only determined by the present input but also depends on the past outputs.

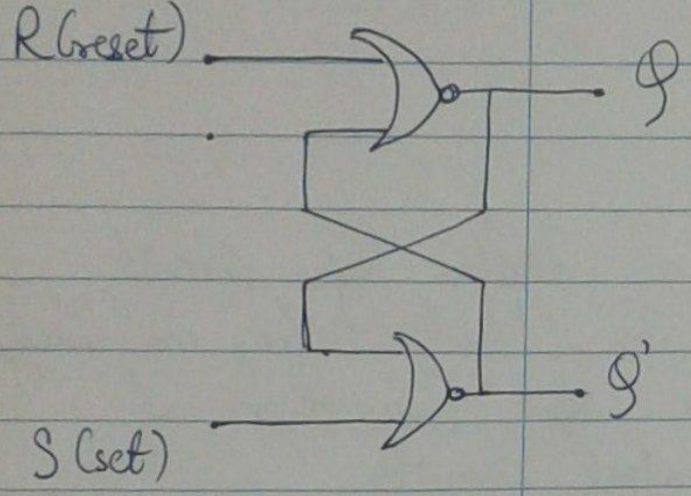
Flip flops are the simplest kind of sequential circuits. A flip flop can maintain a binary state identity which means it can act as 1 bit memory cell. There are different kinds of flip flops depending on the number of inputs or the way the input affects the state.

Basic flip flop.

A basic flip flop can be constructed using two cross coupled NAND/NOR gates.

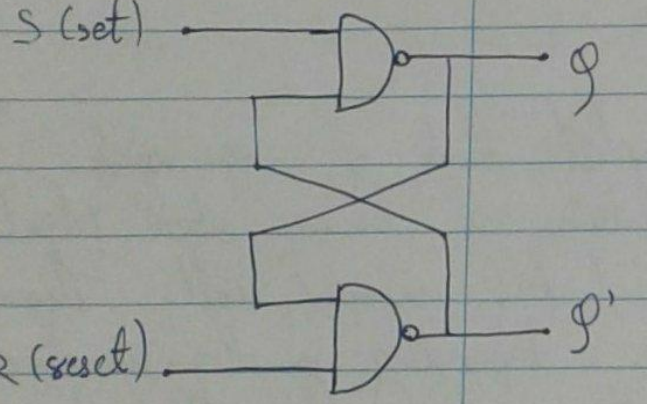
In basic flip flop circuit with NAND gates, when both inputs goes to 0, both outputs go to 0, violating the fact that the outputs of the flip flop have to be complements of each other.

Logic diagram



Truth table

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0



S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

There are various different kinds of flips flops. Some of them are RS flipflop, D-flipflop, J-K flipflop, T-flipflop, etc.

① RS flip flop (Clocked): The basic flip flop is modified by adding some gates to the inputs. So that the flip flops change states.

Truth table:

Q	S	R	Q (t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate.

② JK flip flop.

JK flip flop is a refinement of RS flipflop where the indeterminate state of RS type is defined.

Truth table

Q	J	K	Q (t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

③ D flipflop. - It is used to transfer data to the flip flop. It is basically the JK flipflop where K is inverted.

Truth table

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

(4) T - flip flop. - The T or toggle flip flop, changes its output on each clock edge.

Truth table

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Objective:

i) To understand the basic concepts of flip flops.
ii) To understand race around condition and why does it occur in JK flip flop.
iii) To know how to avoid the race around condition.
iv) To understand what kind of problems may occur in master slave JK flip flop.
v) To know the need for master slave JK flip flop with asynchronous preset and clear.

Procedure:

① Start the simulation. The simulator supports 5 valued logic.

② The experiment is needed to be performed on the given structural ~~wo~~ working modules of all kinds of flip flops.

③ The flip flop components are in the sequential circuit drawer in the pallet.

④ Click on the flip flop component in the pallet and then click on the position of the editor window where you want to add the component, likewise add free running clock, bit switches and bit ~~dist~~ displays.

⑤ To connect any two components select the connection menu of pallette.

⑥ To see the ~~co~~ circuit working, click on the selection tool in the pallet then give input by double clicking on the bit switch, turn on the case analysis feature in the simulator if the pin configuration of the flip flop mentions the case analysis are required then start the clock, now check behaviour of the flip flop according to the ~~guideling~~ guideling given in the objective.

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