JASH SARANIG 47/ DGAD DLCOA Experiment 8.

Experiment 8 Strie Study of this flops using 10's. Components

JK Flip flop.

D Flip flop

SR Flip flop. Apparlatus: Sr no. Theory:

The JK Flip Flop. Characteristic egn of JK flip flop is:

R. Preset (PRE) and clear CELR) are as anynchroners
entire low inputs and operate immediately of the
clock input. clock input. D Flip Flop. Characteristic equ of D flip flop is Quent = D. Tollowing the hold time toll interval, data at the D inputs may be changed without affecting levels of output.

Futh Tables:		Hip	Hop		
	QK	J	X	Qu	
	1	0	0	Qu	
	1	1	0	Qu	
SR Hip Flop	QK 0	8 x 0	R X O _	Que Qu Qu Qu	Memory Hold state Reset
	1	(0	Inval	Set id Unused
D Flip Flop	QKOII	Dxol	QU C		lemony Her.
7 Hip Hops	Qx 0	TXOI		Qu Qu Qu	Memory Hold Taggle.

SR Flep Flop. device having two inputs i.e SET & RESET.

The SR flip flop stands for "Set Reset" Stop stop to its original state from the current state with an output Q. Block digglam: Circuit dia diagram.

loggle Hip Flop. In T- Hip Hop, "T' defines the torm
"Taggle". In SR Hip Hop, we provide only a
single input called "Taggle" or "Trigger" to input
to avoid on intermediate state a occurrence.
Now, Hip Hop work as a Taggle switcher. Block diagsam! Togle input - Output T Q Toggle Hip Hop o Invoded output. Circuit diagram: The T flip flop is toggled when the set to resets inputs alternatively changed by the incoming brigger.

Procedure:	
1 Mount the required 16's &	on the bread board
Procedure: De Mount the required 10's and make the connections as pe	r the diagram.
Dire the +5 vcc & Gird to connecting wires.	IC with the help of
connecting wires.	
(3) With the connecting wires, give to the required pins	the logical inputs
901100 7.119	
(9) Connect the outputs per pin act terminals (Q, Quar)	ross the logical output
3 Apply different inputs and	verify the fruth table.
Conclusion:	1 1/21 1107 00 103
and their buth tables were verifie	ed.
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