Powering ARM MCUs

Case Study:

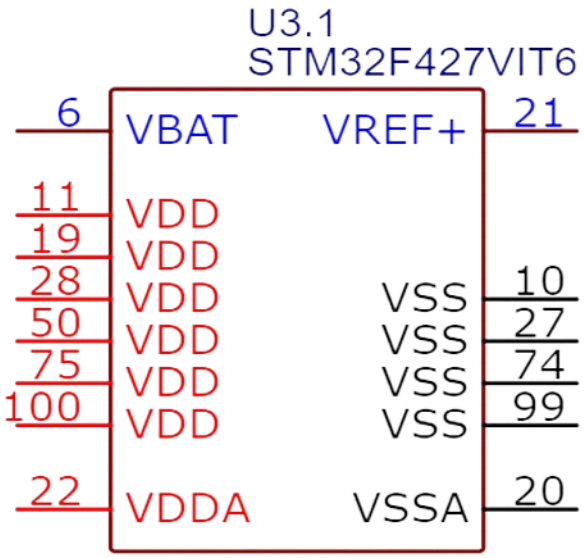
STM32F4XX

STM32F4XX Overview

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU Adaptive real-time Accelerator (ART Accelerator™).
- Up to 2MB Flash/256+4KB RAM.
- Operates from 1.8 V to 3.6 V, with minimum 1.7 V in reduced conditions.
- USB OTG HS/FS, Ethernet.
- 17 TIMs, 3 ADCs, 20 com. interfaces, camera & LCD-TFT.

Power Domains & Pins

- VBAT: RTC / backup registers
- VDD: Digital core & I/O
- VDDA: Analog supply for ADC, DAC
- VCAP1/2: Internal regulator caps (2.2 µF each)
- VREF+/-: External reference (in larger packages)



Supply Voltage Requirements

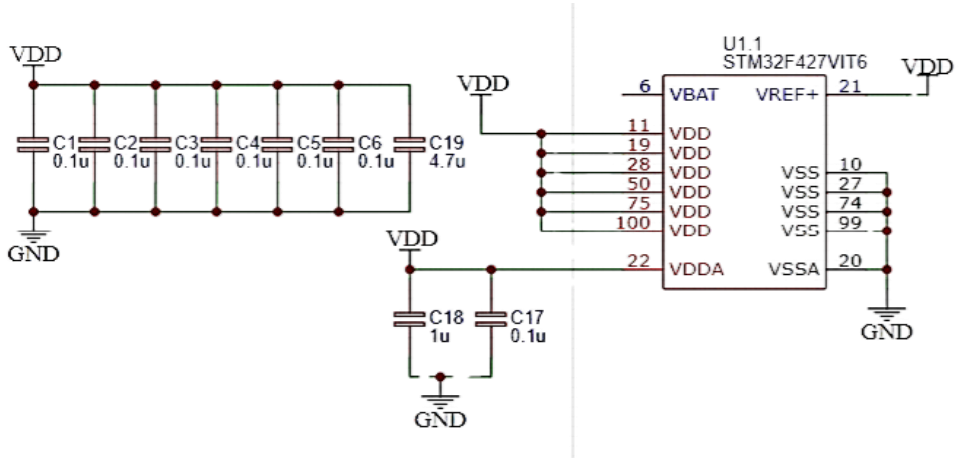
- VDD = 1.7 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through VDD pins.

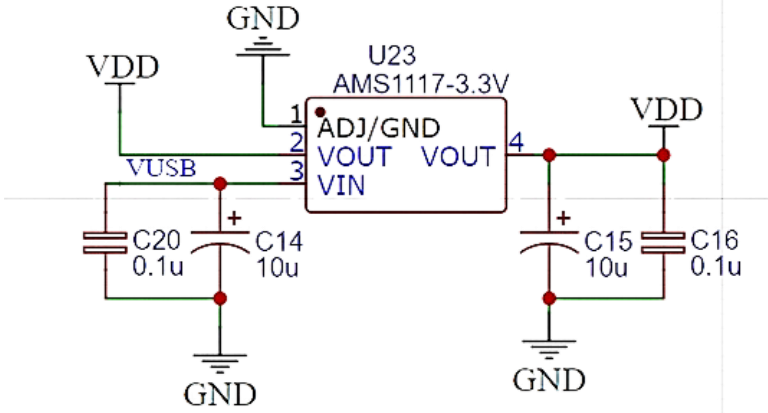
- VSSA, VDDA = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs, and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.

- VBAT = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

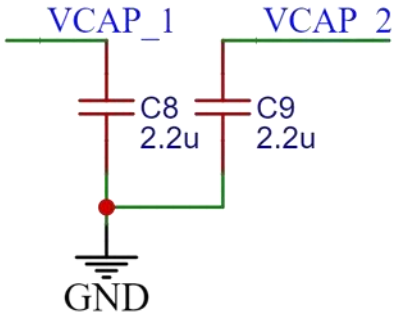
Power-Supply Circuit Essentials

- Clean 3.3 V regulator required if powering via 5V(e.g.,USB) with [2*100nF] and [2*10µF] for filtering

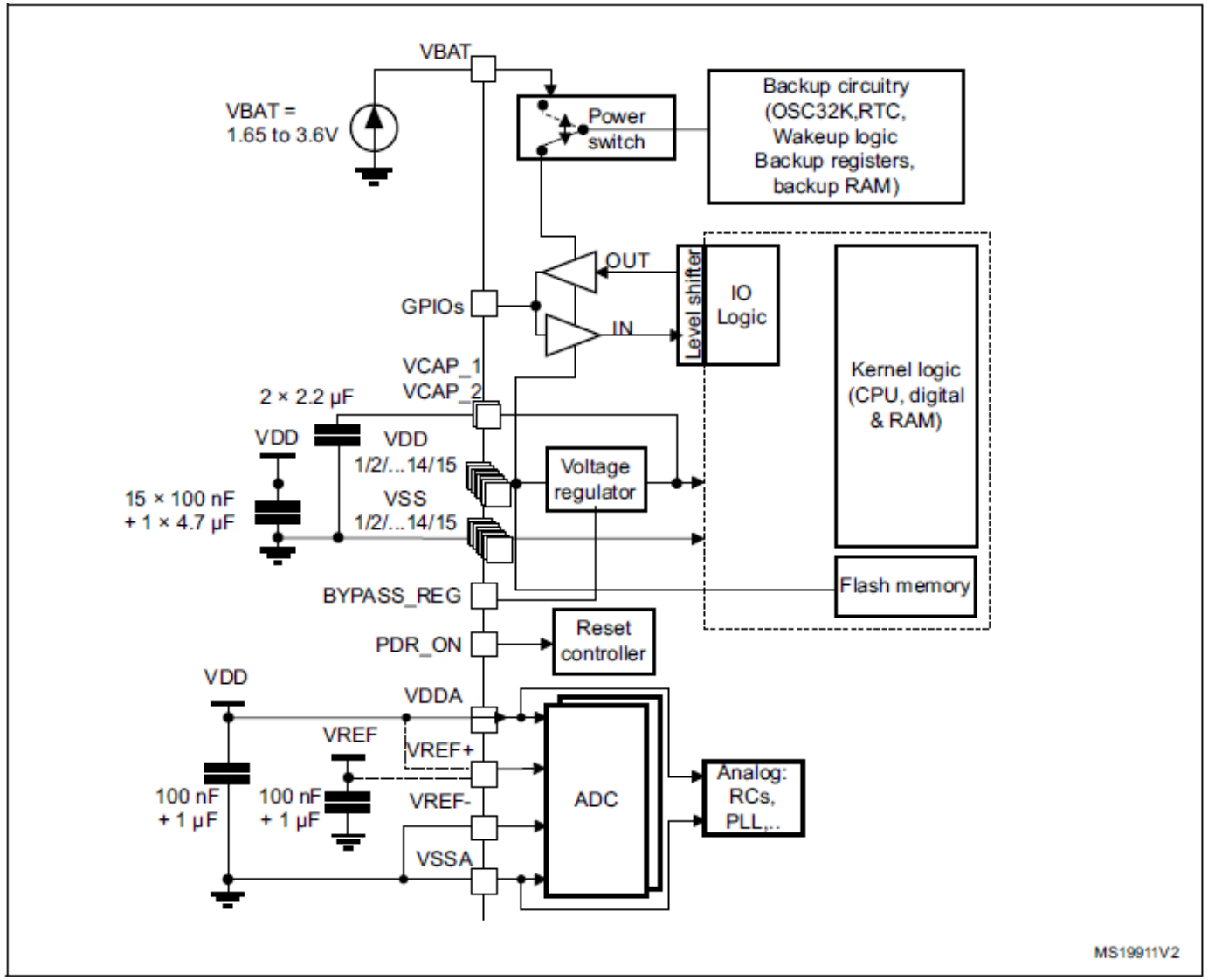




- Recommended decoupling :
  - ❑ VDD: 4.7 µF + 100 nF per pin
  - ❑ VDDA: 1 µF + 100 nF; optional ferrite bead to VDD
  - ❑ VREF+: 1 µF + 100 nF if used
  - ❑ VCAP1/VCAP2: 2.2 µF ceramic, low ESR



Power-Supply Circuit Essentials



Layout recommendations for placing filtering and decoupling capacitors

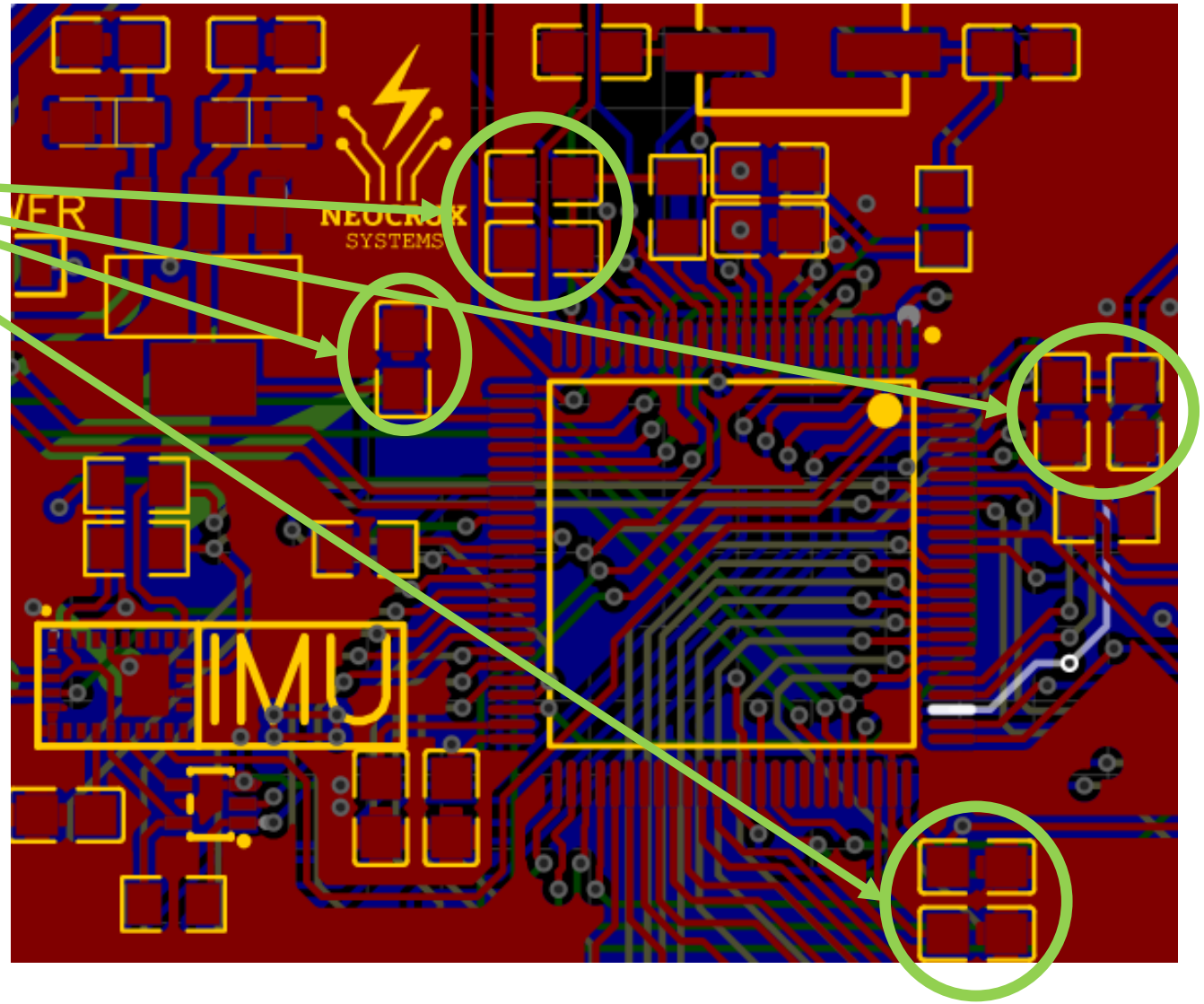
- Place caps as close to each VDD/VSSA/VREF pin as possible.

- Optimize via placement:
  - For each cap, route short, wide traces to separate power and ground vias.
  - Keep these vias close-directly adjacent to the capacitor pads.
  - Avoid long via-to-pad-to-via loops.

- Use both high-frequency and bulk capacitors:
  - Place 0.1 µF MLCC caps right at each power pin for high-frequency noise.
  - Add bulk 4.7–10 µF caps nearby for low-frequency stabilization.

Layout recommendations for placing filtering and decoupling capacitors

Caps placing Example



Low-Power Design Techniques

- **Clock scaling**: Reduce frequency during idle
- **Voltage scaling:** Lower core voltage saves leakage power
- **Use sleep/deep-sleep:** Leverage Stop/Standby modes
- **Disable unused peripherals & GPIOs**
- **Power gating:** Only power necessary blocks

- **STM32-Specific Optimization (AN4635) :**
  - **Best low-power** achieved using MSI at 4 MHz, LPRUN regulator
  - **Typical Stop mode current**: ≈ 44 µA
  - **Lower clock** & **AHB divider** improve efficiency