

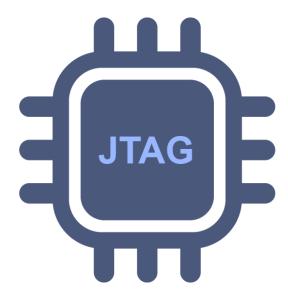


Understanding JTAG Interface in Embedded Systems





JTAG = Joint Test Action Group, standardized as IEEE 1149.1



- Interface primarily used for:
 - Debugging embedded systems
 - oIn-system programming (ISP)
 - Boundary scan testing



- ☐ 1985: JTAG group formed to simplify PCB testing
- ☐ 1990: IEEE 1149.1 standard published

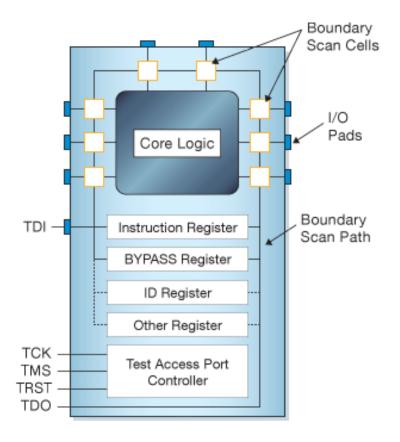
- ☐ 1999: Adopted widely by ARM, MIPS, and DSP processors
- ☐ **Present**: Standard debug method for FPGAs, SoCs, MCUs (e.g. STM32)

JTAG Pinout (ARM Example)

Signal	Description	
TDI	Test Data In	
TDO	Test Data Out	
ТСК	Test Clock	
TMS	Test Mode Select	
TRST	Optional: Test Reset	
GND	Common Ground	



- TAP (Test Access Port)
- Instruction Register
- Boundary Scan Chain
- Core Debug Module
- Connections to MCU/FPGA pins





- ■In-System Programming (flash MCUs, FPGAs)
- Debugging (halt/run, breakpoints, register inspection)
 - ✓ Boundary Scan Testing
 - √ Check soldering issues
 - ✓ Pin-level access even without firmware
- ■Chain Devices Together: Debug multiple chips via shared TDI/TDO

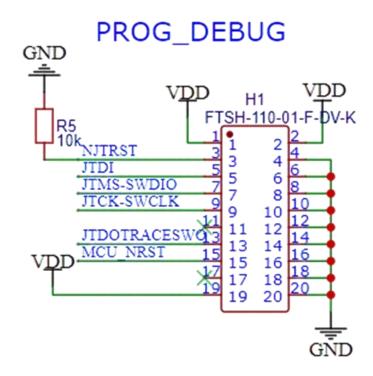
JTAG vs SWD (Serial Wire Debug)

Feature	JTAG	SWD
Pins used	4–5	2
Speed	Slower	Faster
Debug chains	Multi-chip	Single
ARM support	Yes	Yes
Complexity	Medium	Simple

! STM32F4 MCUs support both via SWJ-DP (Serial Wire JTAG Debug Port)

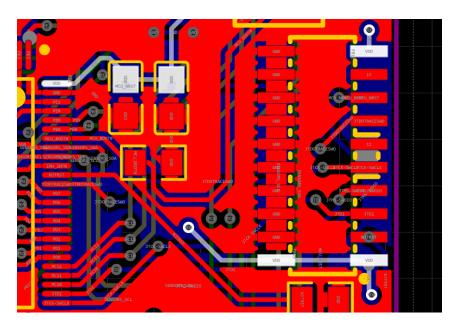
☐ JTAG in STM32

- ■ARM Cortex-M Debug Access Port (DAP):
 - → Supports both SWD and JTAG
 - →Use ST-Link, J-Link, OpenOCD, etc...

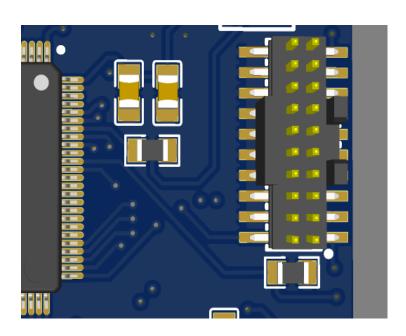


■SWJ-DP Mode: Select between JTAG/SWD via CubeMX or reset sequence

☐ JTAG in STM32 : implementation



PCB layout



3D View



Software

■STM32CubeIDE, OpenOCD, Keil μVision, GDB



Hardware:

■ST-Link V2, SEGGER J-Link, Olimex ARM-USB-TINY



Connector Standards

- ■20-pin ARM JTAG
- ■10-pin Cortex Debug
- ■Tag-Connect (no header)







- ■ETM Trace Port (External trace with TPIU)
- ■Flash breakpoints without RAM usage
- Power debugging (current profiling via tools)
- ■Secure JTAG: Fuse lock, authentication-based access